Results with the ALICE CMOS investigator chip

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CLICdp collaboration meeting

March 9th 2017

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Outline

- Motivation of monolithic technology for the CLIC tracker
- The ALICE Investigator Chip
- Test-beam:
  - Setup
  - Analysis
  - Results
- Simulation
- Summary & outlook

Motivation of monolithic technology for the CLIC tracker

Large surface silicon tracker planned for CLIC (~ 100m²):

➞ Need of large scale production

Benefit from monolithic technologies:

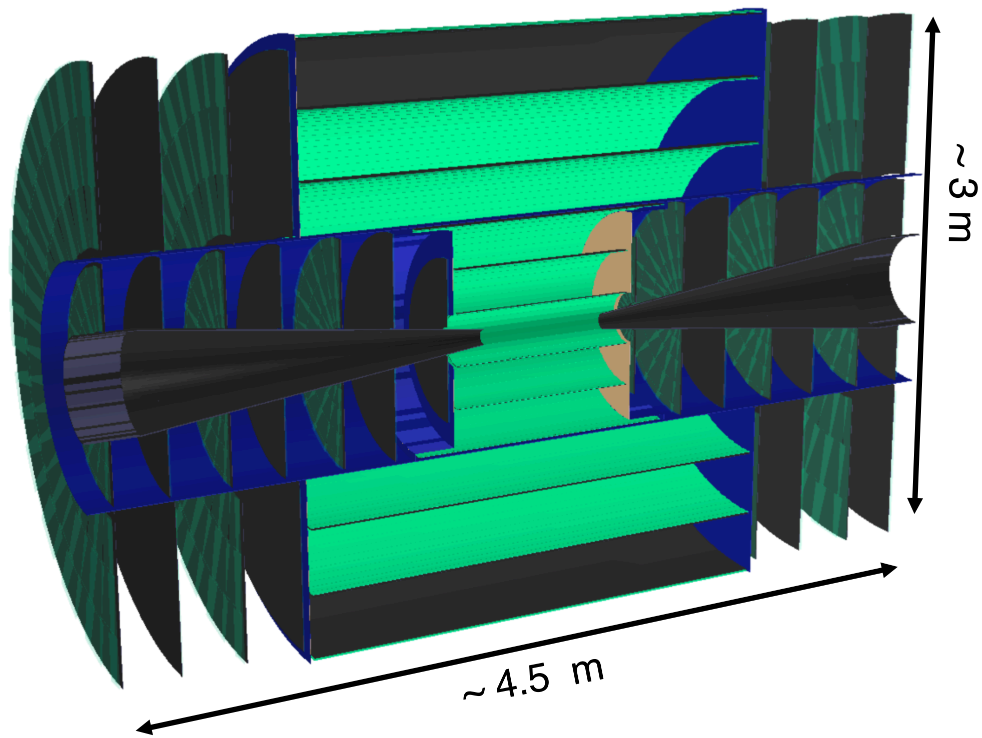
➞ Electronics integrated in sensor
➞ No separate readout chip
➞ No need of bump bonding
➞ Reduced material budget

Benefit from synergies with ALICE collaboration:

➞ Test-chip developed within ALICE collaboration to investigate full analogue performance of monolithic technology chosen by ALICE

➞ Interesting to study feasibility of technology chosen by ALICE with respect to CLIC tracker requirements
(time slicing of 10 ns, single point resolution of ~ 7 μm)

CLIC tracker layout:

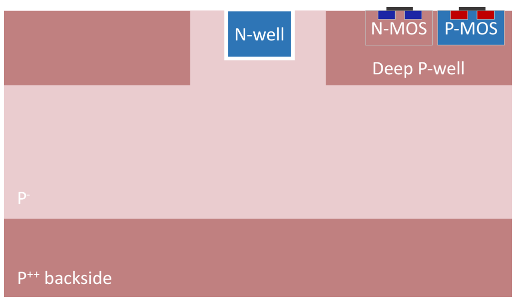


The ALICE Investigator chip (*W. Snoeys, J.W. van Hoorne et. al.*)

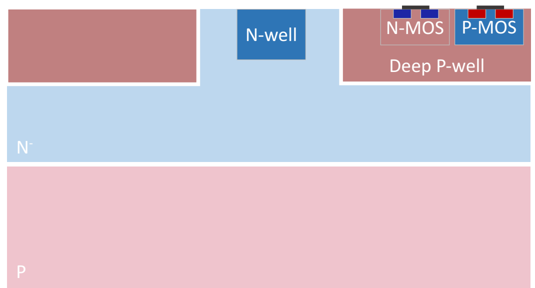
Monolithic HR-CMOS process:

- Developed as part of ALPIDE development for ALICE ITS upgrade
- 180 nm High Resistivity (HR) CMOS process, 15-40 µm thick epitaxial layer (1-8 kΩcm)
- Two different submissions, changes in 2^{nd} submission to achieve full depletion of epitaxial layer:

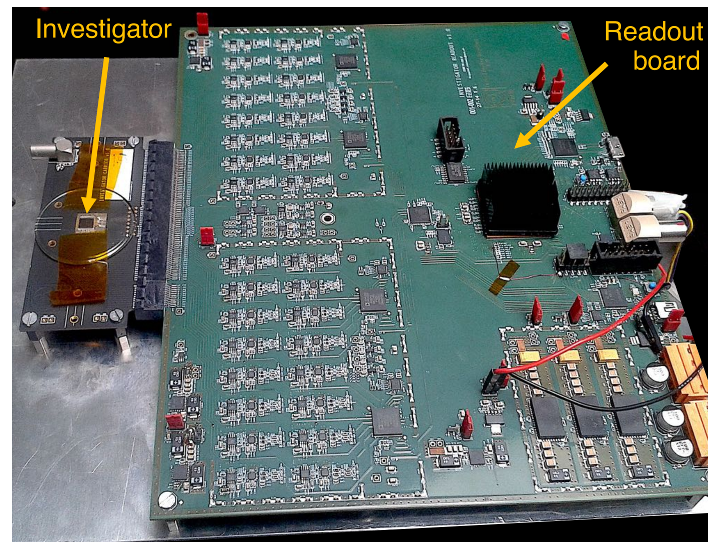
Schematic of process cross section of **standard process**:



Schematic of process cross section of **modified process**:



Investigator & external readout board:



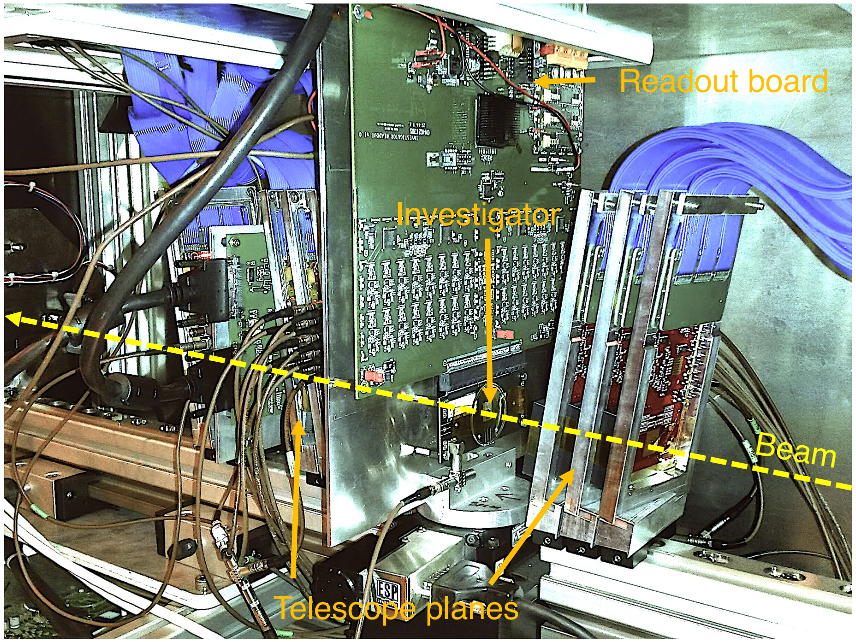
Test chip:

- Different mini-matrixes with 8x8 pixels
- Various pixel layouts to optimise the collection-diode geometry:
  - Minimise capacitance (~ 2 fF) ↔ fast timing (~ ns)
- External readout board (*designed by K. M. Sielewicz*)
- 64 ADCs to read out full waveform of 8x8 pixel matrix
- 65 MHz sampling clock limits achievable timing resolution

Test-beam

ALICE INVESTIGATOR integrated in CLICdp Timepix3 telescope at SPS beam-line:

Test-beam setup:



Benefit from good timing & spatial resolution of Timepix3 telescope:

- Timing resolution ~ ns
- Single point tracking resolution on DUT ~ 2 µm

Synchronisation of Investigator & telescope data:

If at least one pixel crosses a threshold of signal/noise > 8:

- Store waveform from all pixels
- Sent time stamp to telescope planes
- Used for offline synchronisation

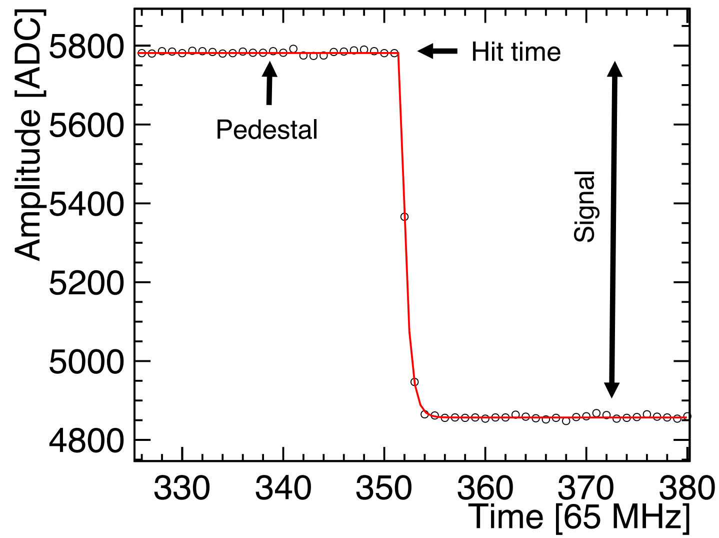
Note: veto of telescope planes during dead times of Investigator to avoid bias in efficiency

Analysis & definition of observables

Investigator event reconstruction:

- Signal defined as magnitude of amplitude drop
- Noise defined as RMS of fluctuation around baseline
- Cut on S/N > 5 for each single pixel
- Fit exponential function f(t) to waveform of each pixel to extract exact timing and signal:

Example of pixel waveform fit:



$$f(t) = \begin{cases} \text{Pedestal} & t \leq t(\text{hit}) \\ \text{Pedestal} + \text{Signal} * (e^{[t-t(\text{hit})] / t(\text{rise})} - 1) & t > t(\text{hit}) \end{cases}$$

Quality cuts:

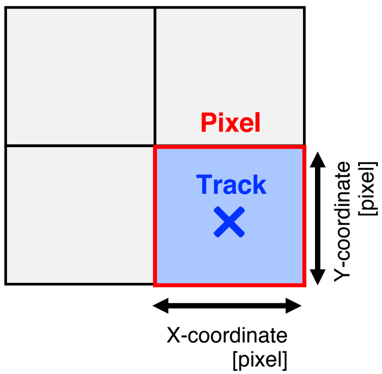
- Distance between track and Investigator hit < 2 pixel
- Masking of half of edge pixels

Charge sharing

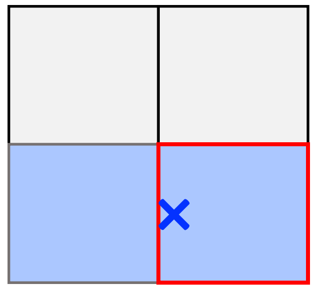
Investigation of track position in pixel for different cluster sizes to study charge sharing on sub pixel level:

Geometrical expectation:

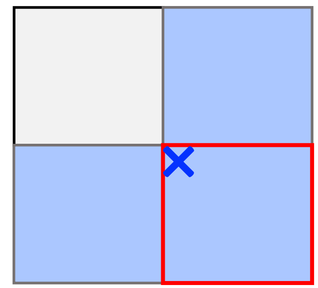
Cluster size 1:



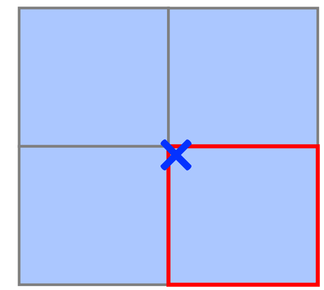
Cluster size 2:



Cluster size 3:



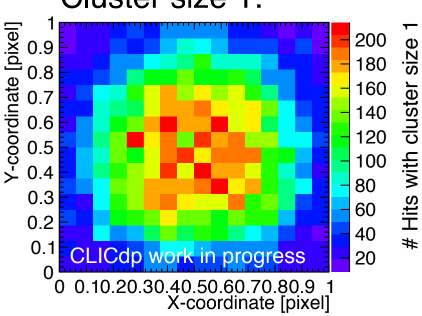
Cluster size 4:



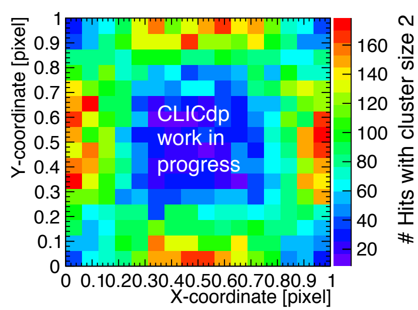
Results for pixel size 28 µm, bias voltage 6 V, 25 µm epi-thickness, modified process:

Seed threshold ~ 140 e^-, neighbor threshold ~ 50 e^-

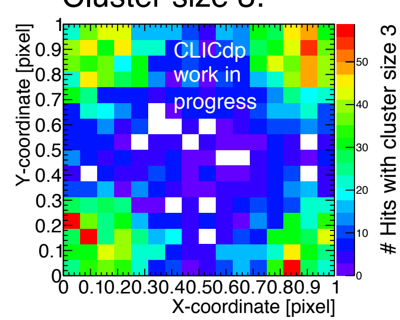
Cluster size 1:



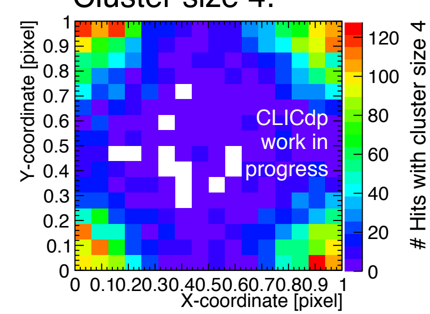
Cluster size 2:



Cluster size 3:



Cluster size 4:



→ Benefit from good tracking resolution of CLICdp Timepix3 telescope

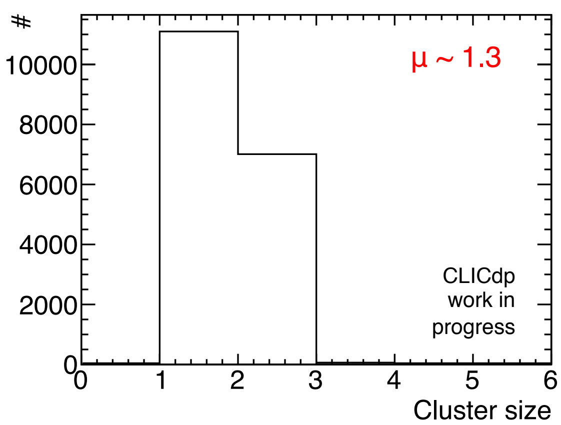
→ *Detailed understanding of charge sharing on sub pixel level*

Spatial & timing resolution

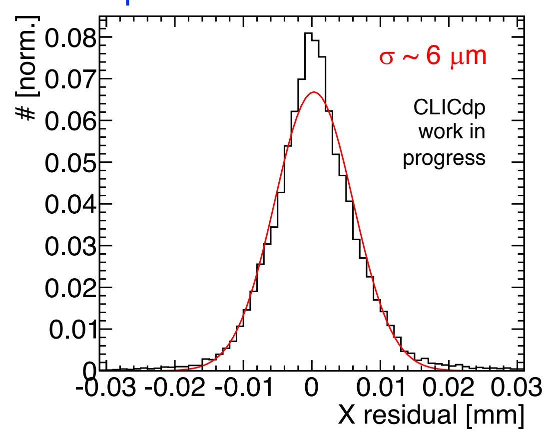
Results for pixel size 28 µm, bias voltage 6 V, 25 µm epi-thickness modified process:

Seed threshold ~ 140 e⁻, neighbor threshold ~ 50 e⁻

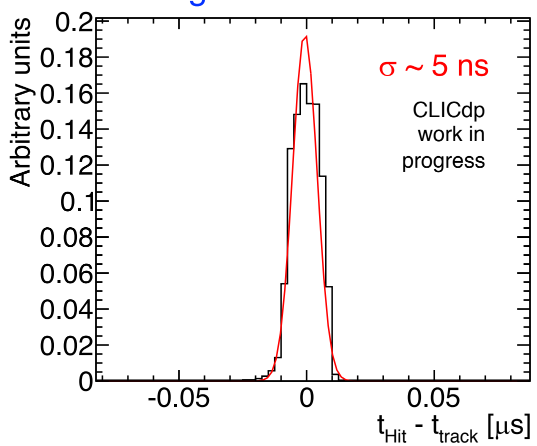
Cluster size in X:



Spatial residual in X:



Timing residual:



- Spatial reconstruction by charge interpolation and η-correction to correct for non-linear charge sharing

➜ Charge sharing leads to improved spatial resolution of ~ 6 µm (binary expectation ~ 8 µm)

- Timing residual determined by difference between hit time of first pixel in cluster and mean track time

➜ Timing resolution of ~ 5 ns (note: limited by sampling frequency of 65 MHz)

➜ *Spacial & timing resolution well within requirements for CLIC tracker (external readout)*

Efficiency

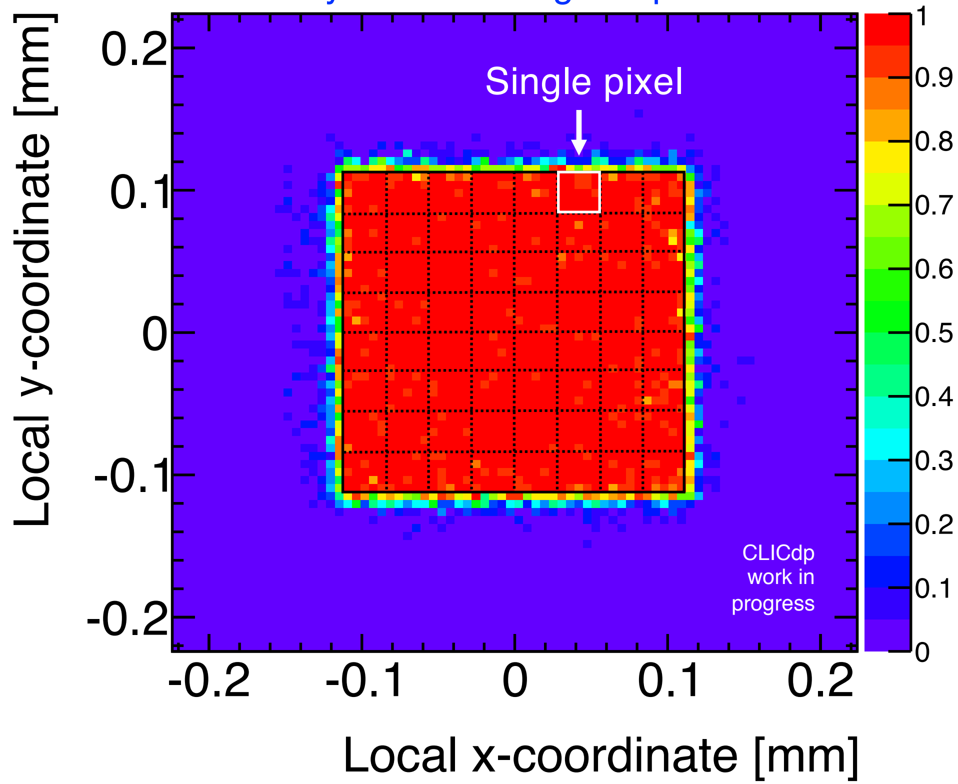
Results for pixel size 28 µm, bias voltage 6 V, 25 µm epi-thickness modified process:

Seed threshold ~ 140 e$^-$, neighbor threshold ~ 50 e$^-$

If a track is reconstructed through the Investigator:

- If Investigator hit within distance of 2 pixels from track
  → Count 1 for efficiency
- If NO Investigator hit within distance of 2 pixels from track
  → Count 0 for efficiency
- Histogram filled at local track position extrapolated on Investigator

Efficiency over Investigator pixel matrix:



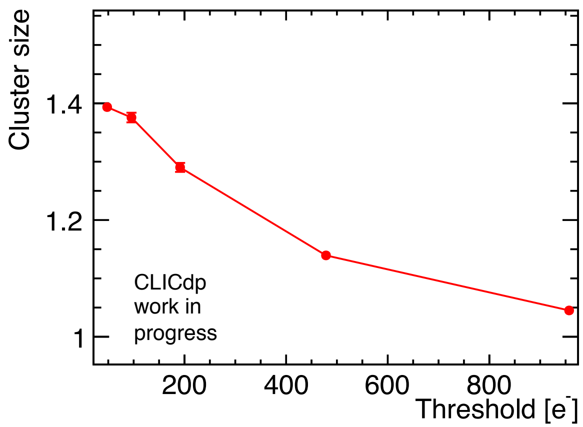
- Global efficiency of ~ 99.3 % (after masking of half of edge pixels, study ongoing)

→ *Good performance in full phase space*

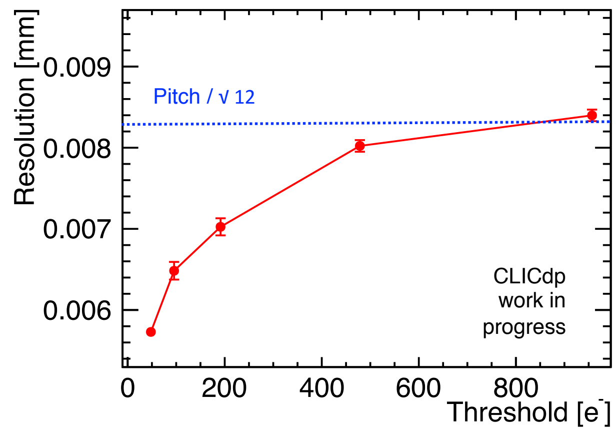
Threshold scan

Results for pixel size 28 µm, bias voltage 6 V, 25 µm epi-thickness modified process:
Calibration with Fe-source applied to convert threshold to e^-

Cluster size vs. threshold:



Resolution vs. threshold:



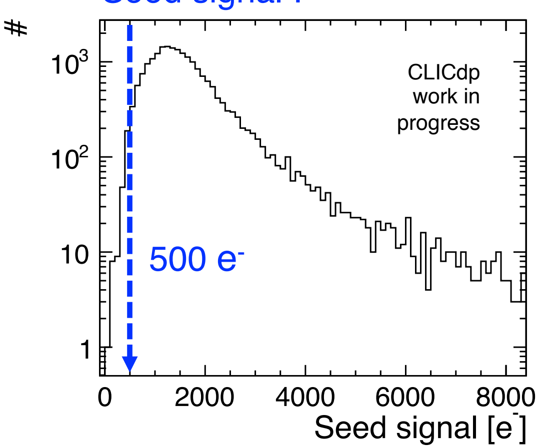
General dependency:

Cut into neighbor signal:

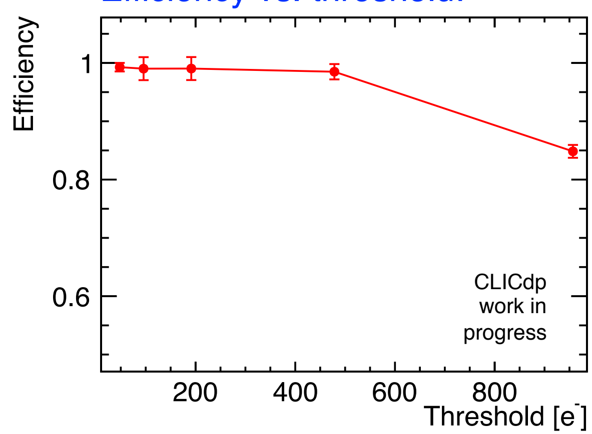
- Decrease of cluster size
- Degradation of resolution

until binary limit

Seed signal :



Efficiency vs. threshold:



Very high threshold > 500 e^-:

Cut into seed signal:

- Decrease of efficiency

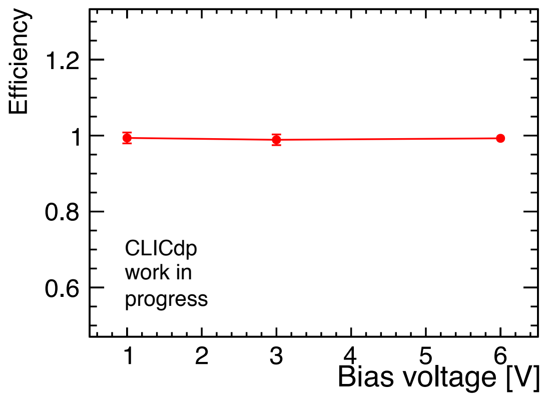
➔ *Need low threshold to gain in resolution and be fully efficient*

Bias scan

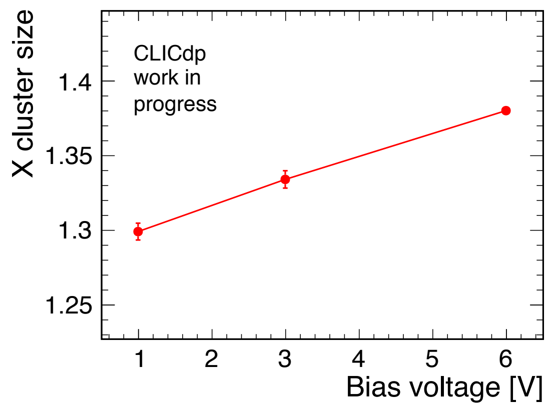
Results for pixel size 28 μm, 25 μm epi-thickness modified process:

Calibration with Fe-source applied to convert threshold to e^-

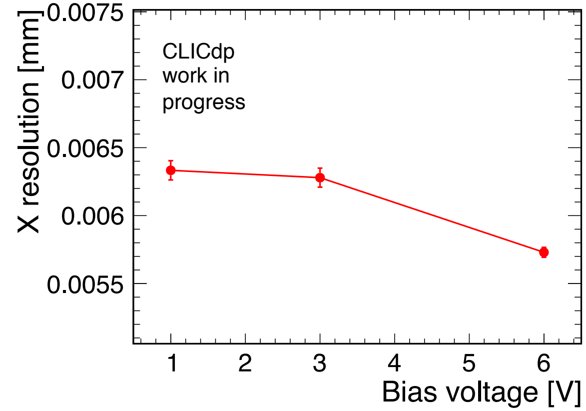
Efficiency vs. bias:



Cluster size X vs. bias:

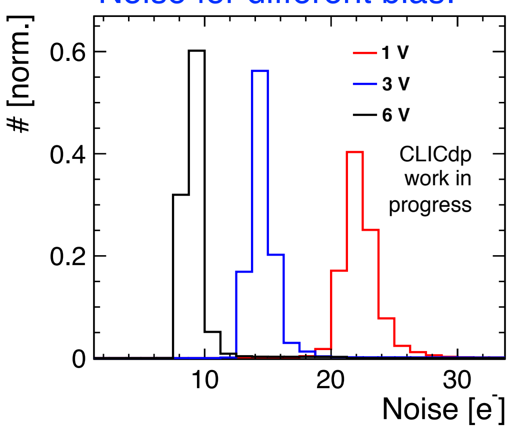


X resolution vs. bias:

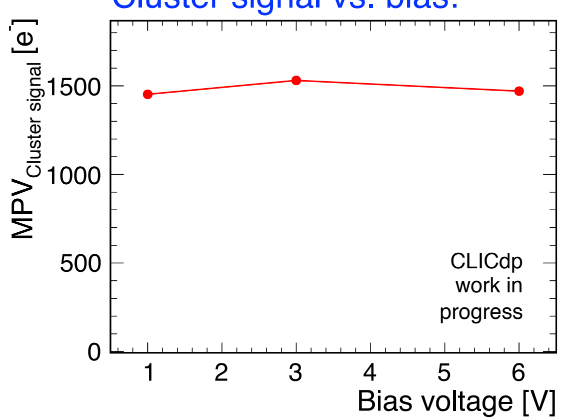


- No significant changes in efficiency
- Lower cluster size and worse resolution for low bias:

Noise for different bias:



Cluster signal vs. bias:



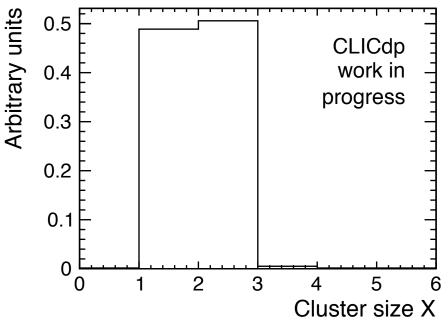
- Higher noise for lower bias voltage due to higher input capacitance for lower voltage
- No significant changes in signal
- Higher cut on signal/noise
- Less charge sharing for lower bias because of higher threshold

➔ *Need high bias to achieve low noise to be able to push the threshold to low values and gain in resolution*

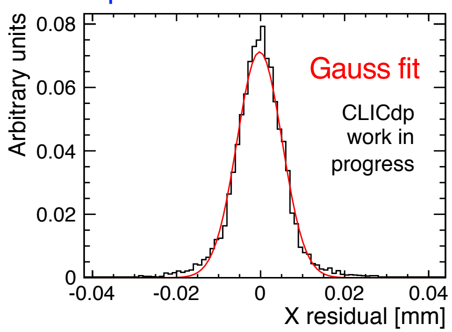
Comparison of two different submissions

Results for pixel size 28 µm, bias voltage 6 V **standard process**:

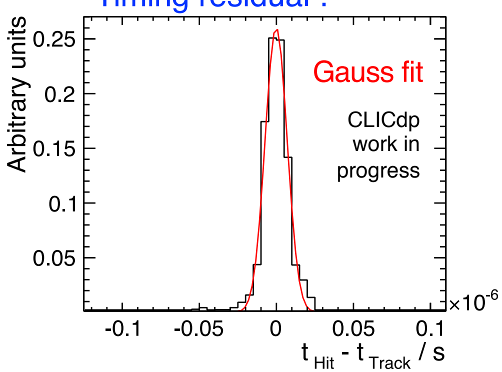
Cluster size X:



Spatial residual X:



Timing residual :

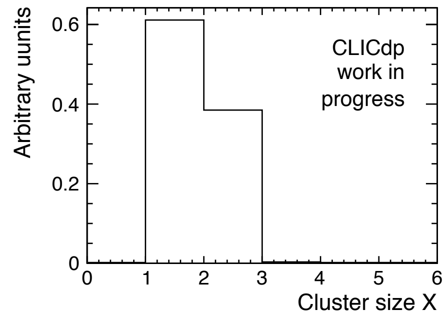


Summary table:

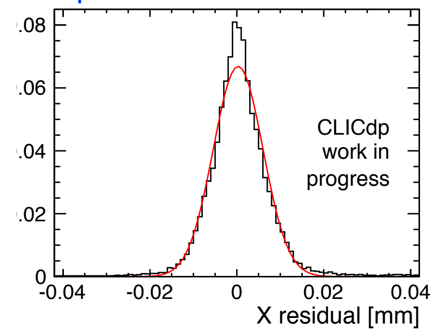
Cluster size X	**1.5**
Spatial resolution X [µm]	**5**
Timing resolution ns	**7**
Seed threshold [e-]	**200**
Neighbor threshold [e-]	**70**
Epi thickness [µm]	**18**

Results for pixel size 28 µm, bias voltage 6 V **modified process**:

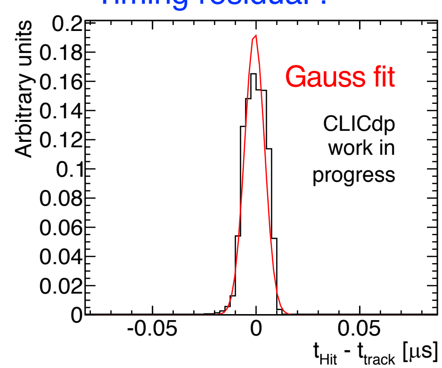
Cluster size X:



Spatial residual X:



Timing residual :



Summary table:

Cluster size X	**1.3**
Spatial resolution X [µm]	**6**
Timing resolution ns	**5**
Seed threshold [e-]	**140**
Neighbor threshold [e-]	**50**
Epi thickness [µm]	**25**

Magenta = main different parameters

Changes in second submission to achieve full depletion:

➔ Expect that less diffusion results in lower cluster size & faster timing

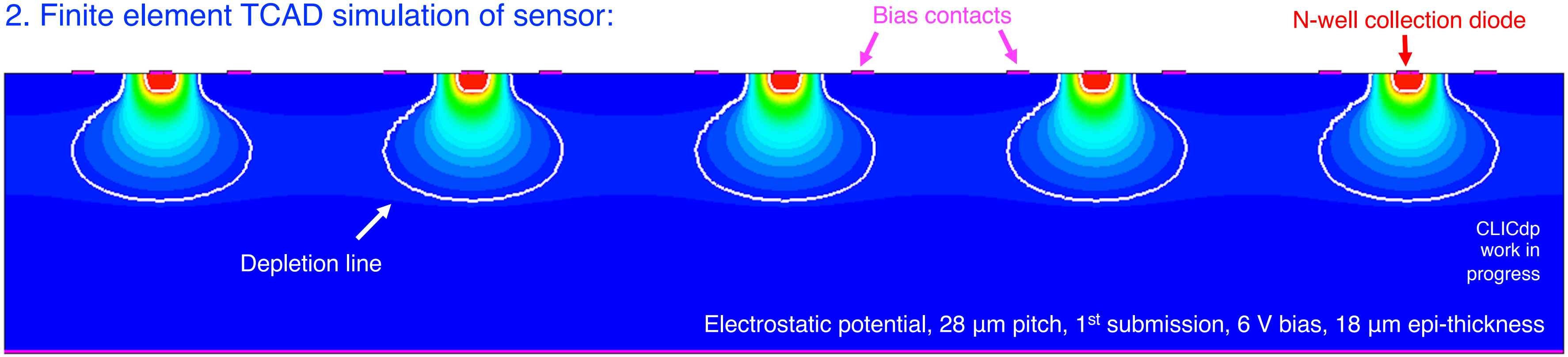
➔ *Despite thicker epi layer for modified process, lower cluster size and faster timing compared to standard process*

2 dimensional simulation of standard process

Simulation chain:

1. Geant4 simulation of energy deposit in silicon

2. Finite element TCAD simulation of sensor:



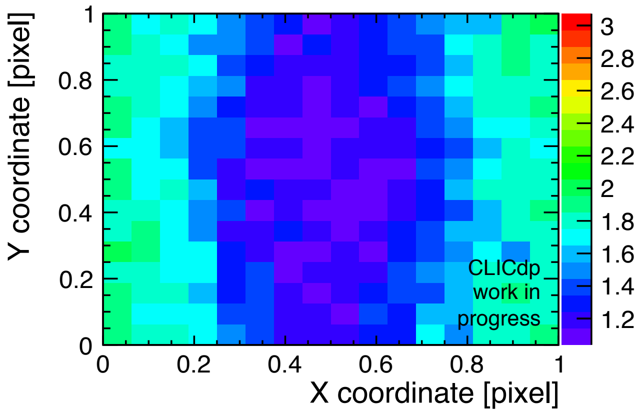
- Simulate sensor geometry, doping and bias application
- Transient simulation using particle with energy deposit from GEANT4
- Scan particle incident position over unit cell, representing full physical problem and calculate induced charge

3. Fast model of threshold application, energy fluctuations, telescope resolution and reconstruction

Comparison of simulation & data

Comparison of 3d-data and 2d-simulation:

Mean X cluster size in pixel / data:



Observation:

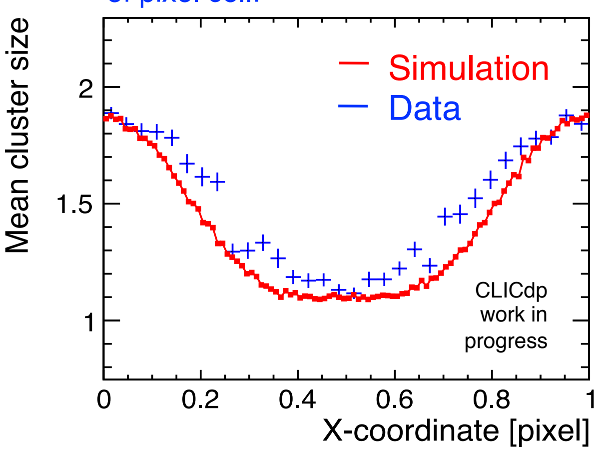
- Charge sharing in X does not change significantly along Y dimension of pixel

➔ Can compare X-cluster size in pixel and X-residual between data and simulation (*approximation*)

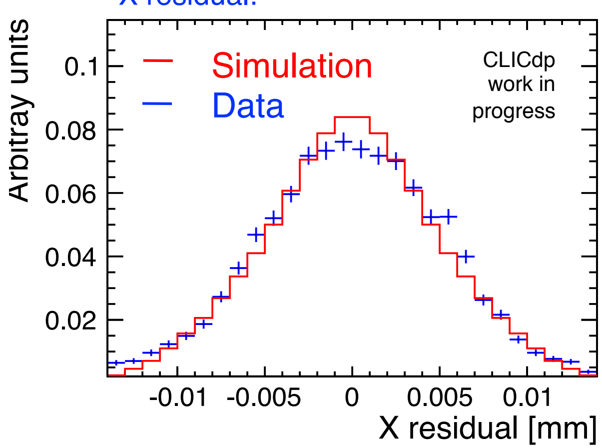
Comparison of simulation & data, pixel size 28 µm, bias voltage 6 V, 18 µm epi-thickness standard process:

Seed threshold ~ 200 e^-, neighbor threshold ~ 70 e^-

Mean X cluster size in x dimension of pixel cell:



X residual:



- Calibration applied to define threshold in simulation

➔ *Good agreement of simulation in X residual and in-pixel X cluster size*

Summary & outlook

Investigator HR-CMOS process studied in various test-beam campaigns:

- Charge sharing on in-pixel level well understood
- Bias and threshold scan performed
- Qualitative comparison of different submissions

- Overall performance meeting requirements for CLIC Tracker:
  - Single point resolution ~ 6 μm
  - Efficiency ~ 99.3 %
    (study ongoing)
  - Timing resolution ~ 5 ns

Results for modified process
28 μm pixel size
Test-chip with external readout

→ Studies used as input for design of fully monolithic tracker chip for CLIC
(see Iraklis talk in this session: *An overview of CMOS sensor technologies for CLIC*)

Simulation of standard process:

- Validated with test-beam data ongoing, good agreement so far
- Can be used to investigate performance for different pixel layouts