Recent results with SOI pixel detector

R. Dasgupta*

on behalf of CLICdp
and Cracow groups: AGH-UST and IFJ-PAN

* AGH University of Science and Technology

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SOI Technology

and

Prototype SOI pixel chip

Monolithic pixel detectors in SOI

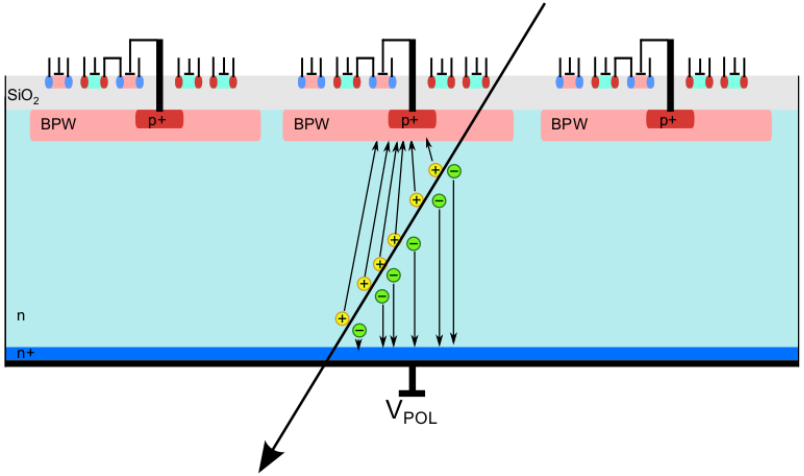
Properties

- Minimum pitch $< 10\ \mu m$
- Small sensor capacitance (good SNR)
- Double SOI $\rightarrow$ radiation hardness
- Wide temperature range $(4 - 400K)$
- Thinner (down to 50 μm) and cheaper then hybrid solutions

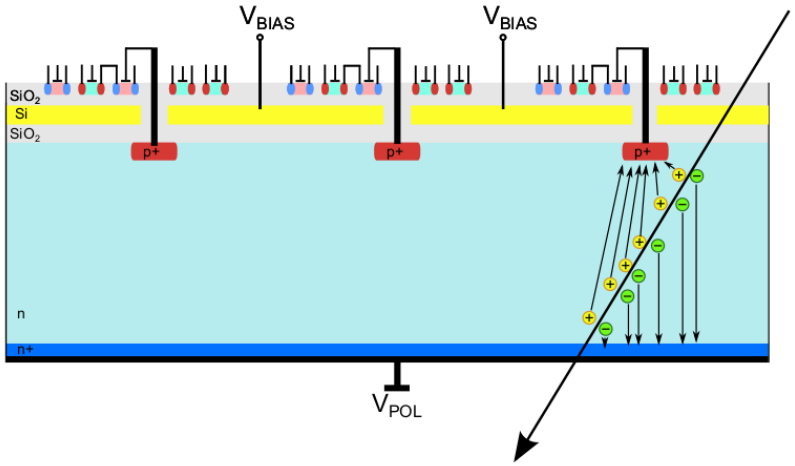
Double Silicon-On-Insulator

- voltage applied on Mid-Si layer allows to correct the potential changes caused by positive charges induced by irradiation,
- Mid-Si shields electronic from negative influence of high voltage needed for fully depletion.

SOI STRUCTURE



DOUBLE SOI STRUCTURE

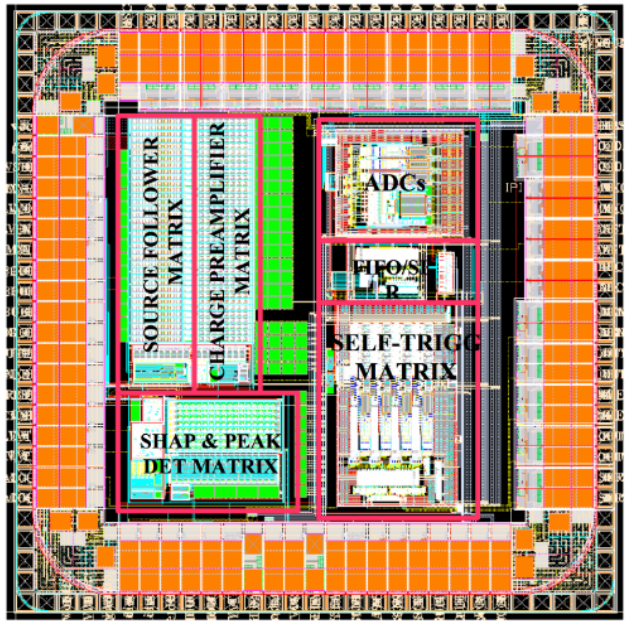


Lapis offers 200 nm Fully-Depleted Low-Leakage SOI CMOS with four wafer types: FZ(n), CZ(n), FZ(p) and Double SOI(p)

Prototype SOI pixel chip

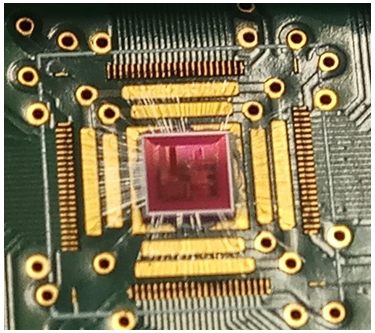
Architecture overview :

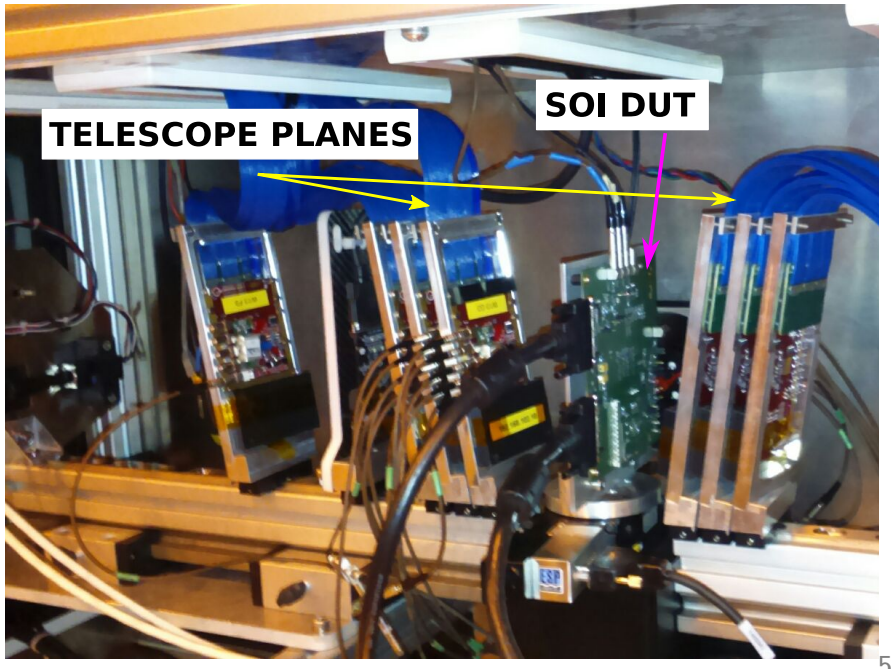
- Submatrixes with different source-followers types (various layouts and transistor sizes),
- In total 16×36 pixels (each $30\mu m \times 30\mu m$)
- Rolling shutter readout (integration time for one frame: $\sim 100\mu s$),
- Different wafer types **(FZ(n),CZ(n), FZ(p) Double SOI)** with different substrate thickness (300-500 μm) and resistivity → For this study only FZ(n)



Testbeam:

- Two testbeams: June 2016 and August 2016, using CLICdp Timepix3 telescope, in the SPS-H6 beamline

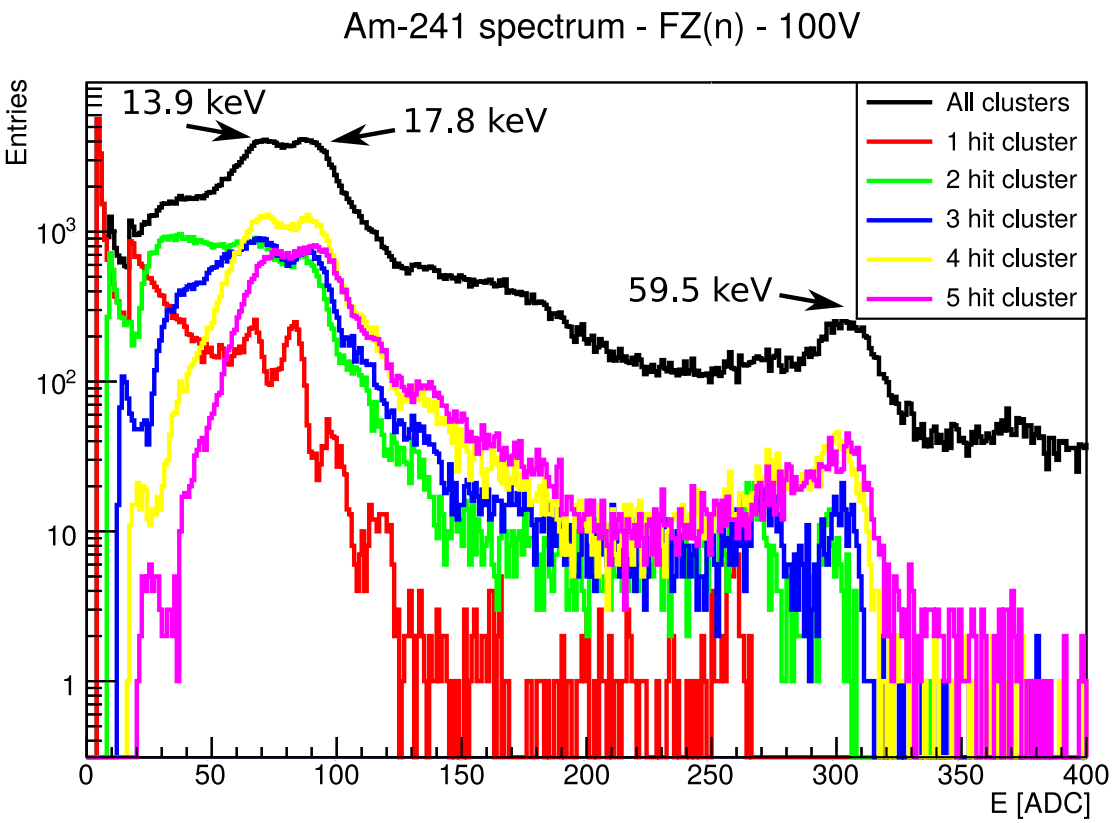


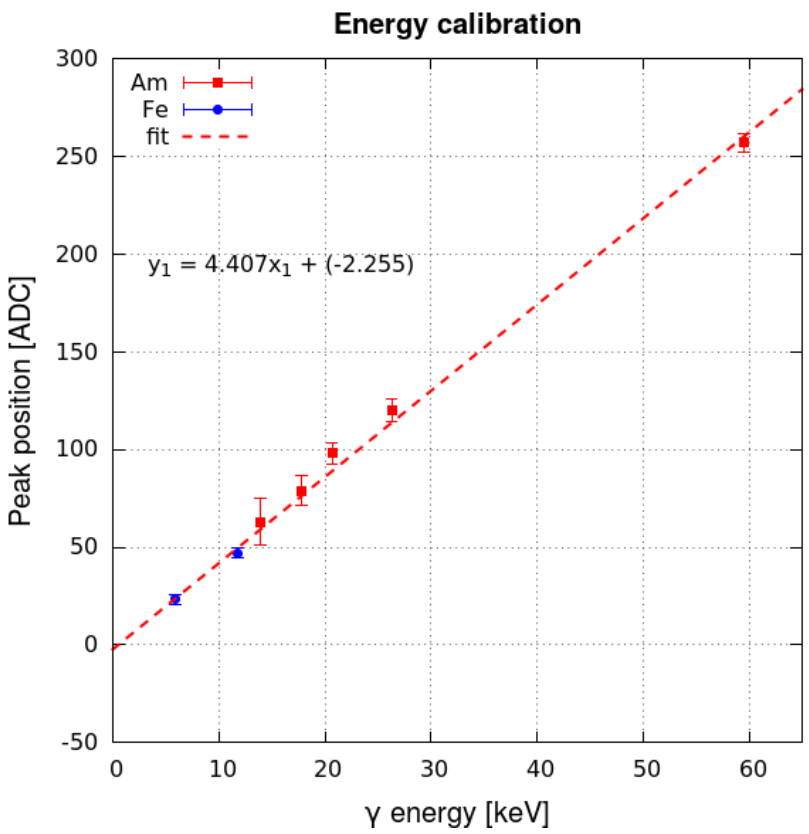


Detector characterization

- Energy resolution
- Full depletion
- Signal to noise ratio

Americium spectrum - lab measurement



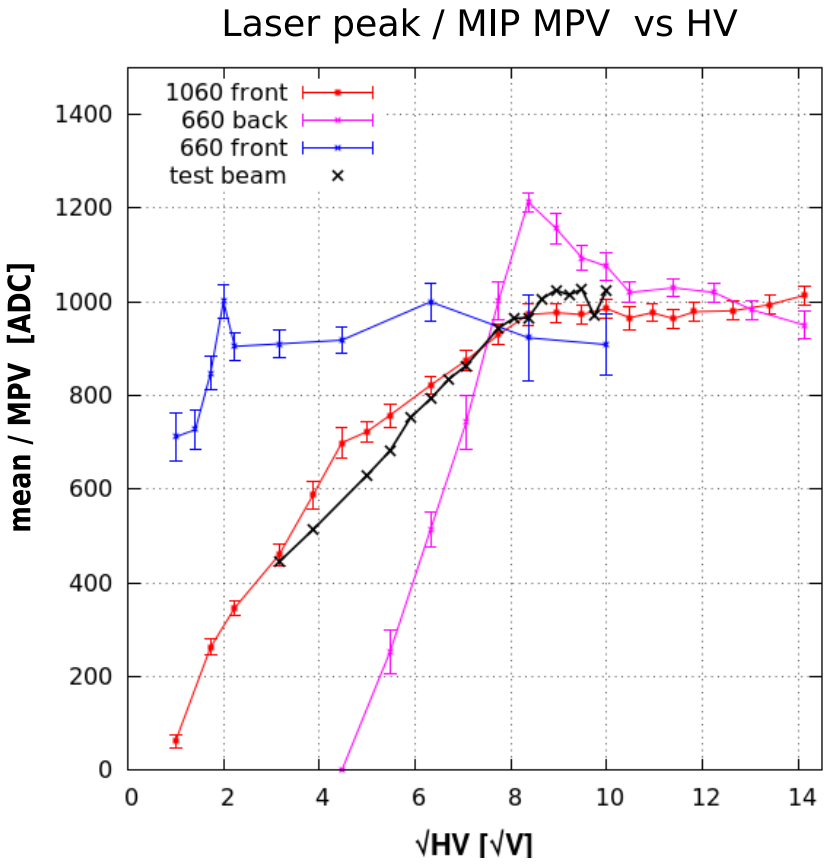


- Measurements with Am-241 and Fe-55 allowed energy calibration.
- Five Am-241 and two Fe-55 lines are reconstructed.
- Pixel noise for the best submatrix is around 120 e^-.

Full depletion voltage estimation

HV scans with MIPs (testbeam) and laser (lab) performed:

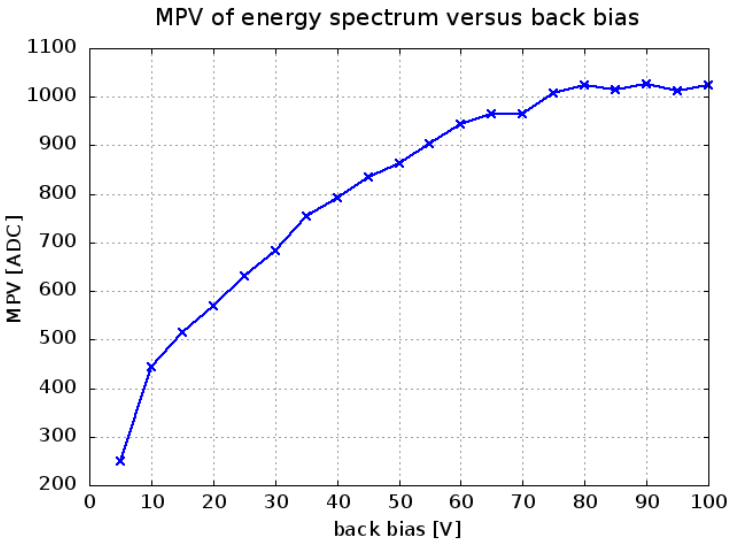
- black curve shows the MPV of landau fit from testbeam,
- 660 nm laser front and back shallow illumination ($\sim 10\mu m$),
- 1060 nm laser goes through whole sensor,
- 1060 nm behaves like MIP,
- 660 nm seen from the back $\rightarrow$ sign of full depletion.

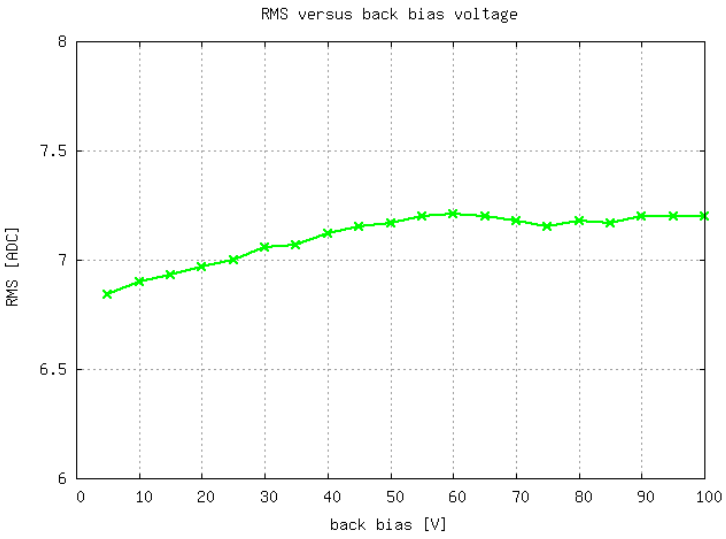


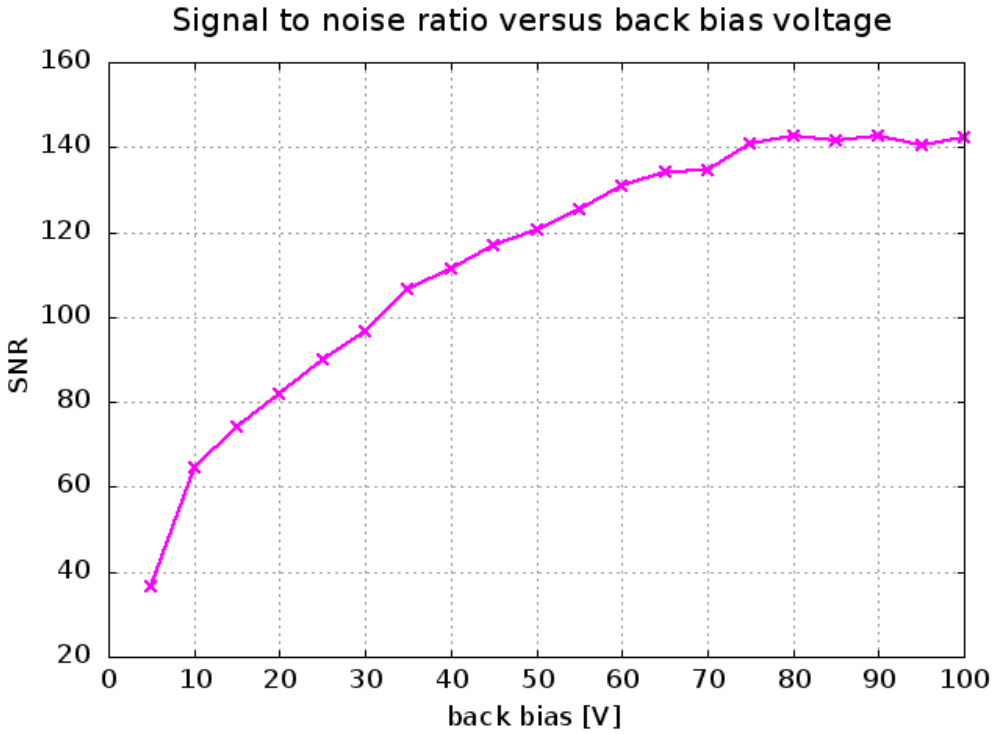
Full depletion

The full depletion is achieved around 80V.
The thickness of the wafer is around 500 μm and resistivity above 30 $k\Omega$.

Signal to noise ratio







- Noise: pixel RMS is around 7 ADC.
- Very good signal to noise ratio.

Clusterization methods

Different methods of clusterization in order to improve position calculation:

TWO-SEED METHOD

SEED (above 1nd th)

NEIGHBOURS (above 2nd th)

1.2σ	0.7σ	0.5σ	0.1σ
0.5σ	10.9σ	1.2σ	0.5σ
0.7σ	9.8σ	5.1σ	0.1σ
0.1σ	0.2σ	3.0σ	0.1σ
0.2σ	0.6σ	0.1σ	0.2σ

ALL-ADJACENT METHOD

SEEDs (above 1nd th)

NEIGHBOURS (all adjancet to seeds)

1.2σ	0.7σ	0.5σ	0.1σ
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- Find pixels with signal above first threshold (signal $> 9\sigma = 9 \times$ pixel noise)
- Find all adjacent pixels above second threshold (signal $> 2\sigma$)
- When any pixel found, repeat algorithm for each new one.
- 4-pixel cluster is found.

- Find pixel with signal above threshold (signal $> 9\sigma$)
- When seed found, found all next adjacent seeds and repeat for each new one.
- Add to cluster all seeds neighbours
- 12-pixel cluster found.

Clusterization methods

Different methods of clusterization in order to improve position calculation:

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Better for energy resolution

Better for spatial resolution

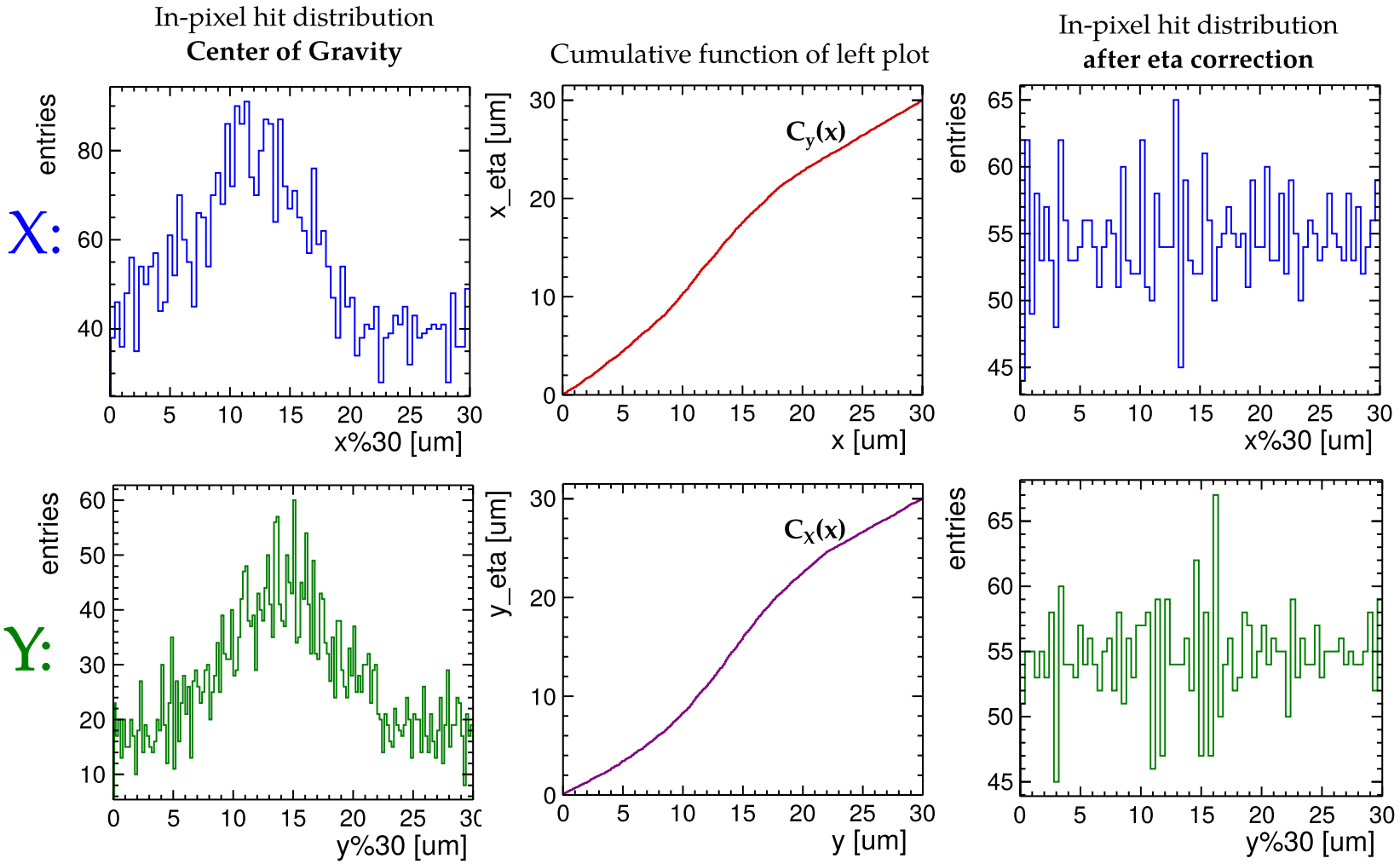
Spatial resolution

Eta correction

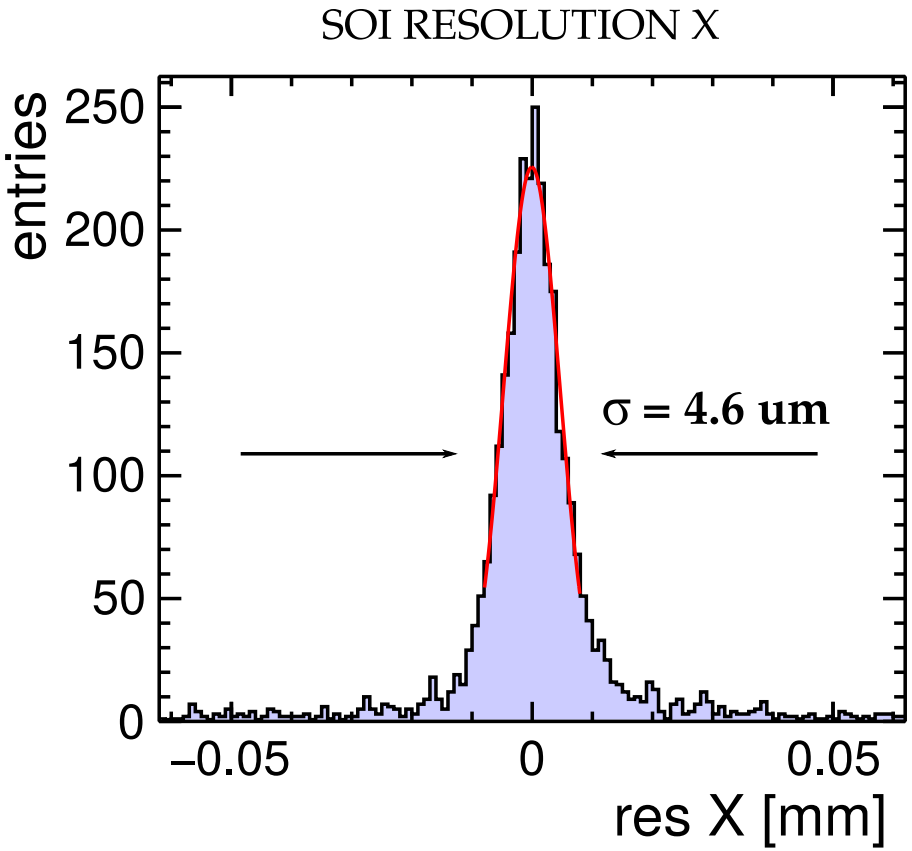
For position reconstruction two methods were tested:

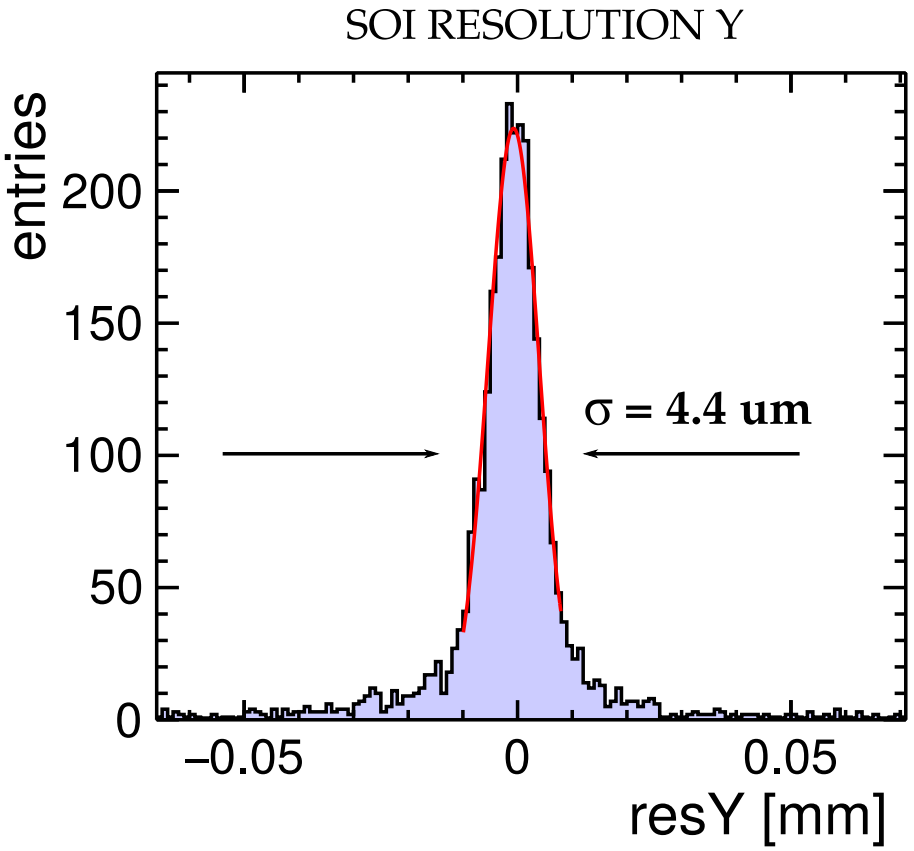
1. Center of Gravity
2. **Eta correction**

The in-pixel distribution is plotted → the cumulative function of this distribution is calculated: $C_X(x)$ → the corrected position x_{ETA} is given by: $x_{ETA} = C_X(x_{COG})$, where x_{COG} is the hit position obtained from center of gravity method.



Spatial resolution of FZ(n) SOI detector at 90V





all-adjacent, rotation, eta - X

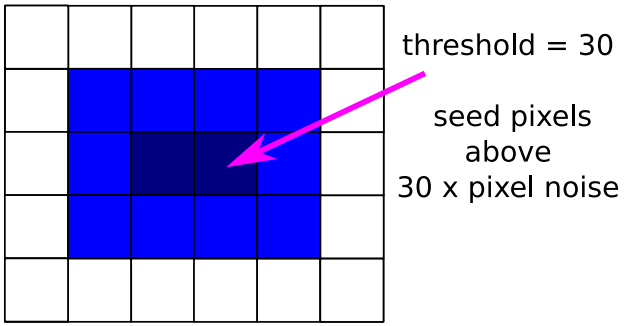
$X_{res} = 4.6\ \mu m$

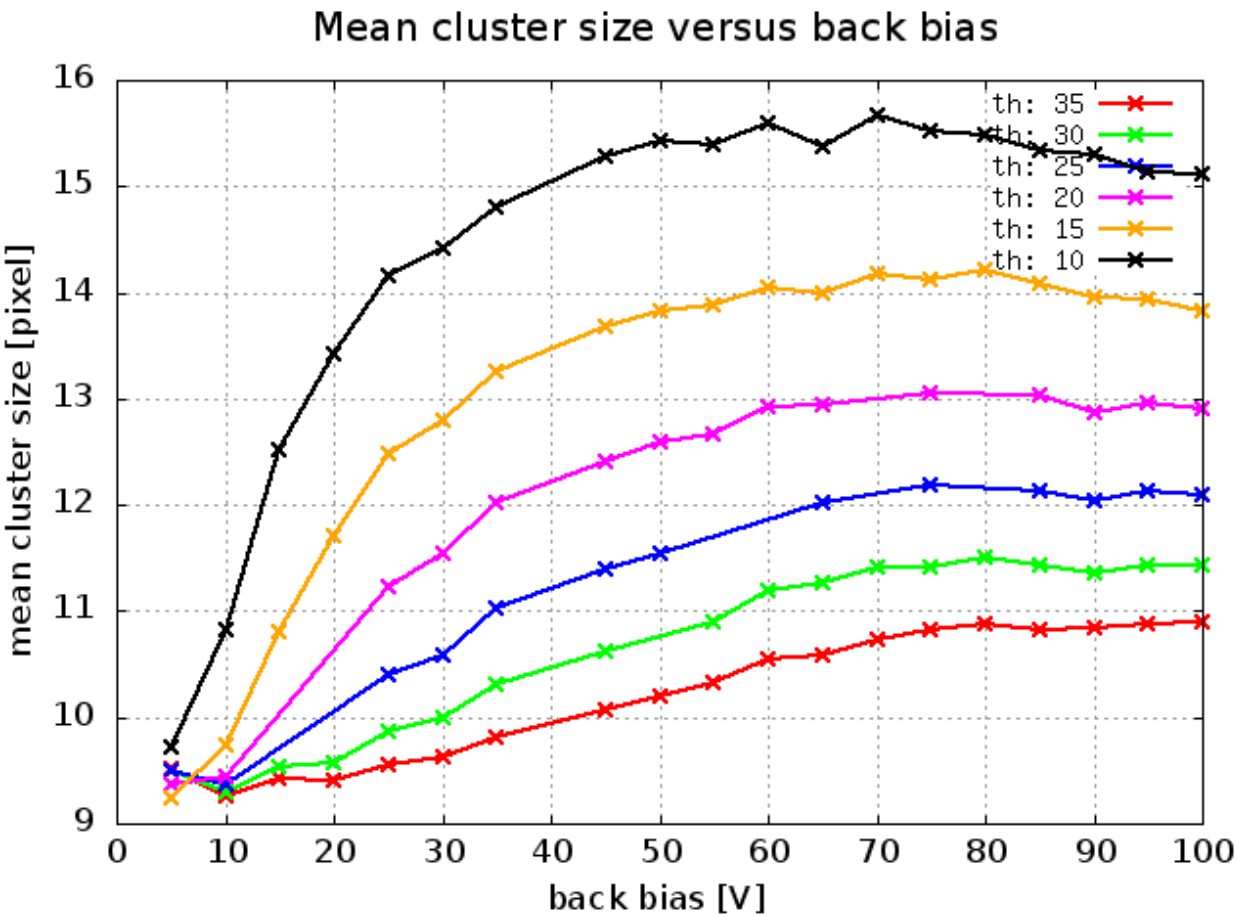
all-adjacent, rotation, eta - Y

$Y_{res} = 4.4\ \mu m$

Taking into account the telescope resolution ($\sigma_T = \sim 2\mu m$) the SOI detector resolution is around $\sigma_{SOI} = \sim 4\mu m$.

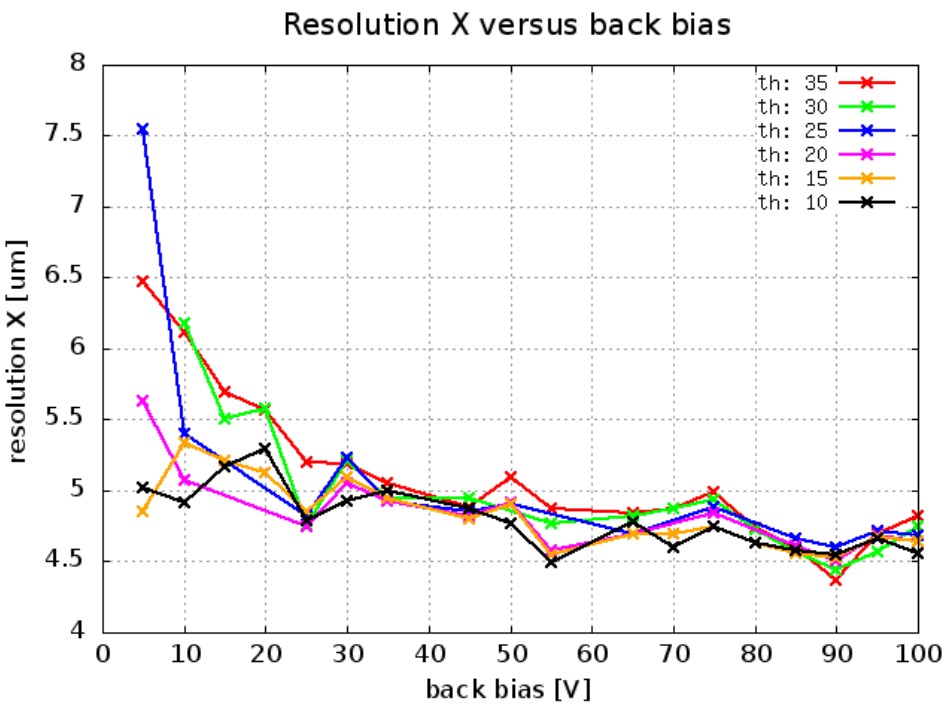
Cluster size versus back bias voltage





- Minimum cluster size is determined by clusterization method (9 pixels).
- Mean cluster size decreases with growing threshold.
- After full depletion mean cluster size is stable.

Resolution versus back bias voltage



- Resolution is weakly dependent on cluster threshold.
- From 30 V (depletion region around 300 μm) good resolution is obtained, with small improvement for higher bias.

Summary

1. SOI pixel detector was tested **successfully for the first time in CLICdp testbeam**.
2. **High signal to noise ratio**: above 100 from 30 V back bias voltage.
3. **Full depletion** is achieved around $\sim$ **80V** $\rightarrow$ 500 μm wafer thickness and $\sim 30k\Omega$ resistivity.
4. **Spatial resolution** for 30 μm SOI pixels of **around** 4 μm **was obtained.**
5. Ongoing studies: analysis for Double SOI wafer.

Close future plans:

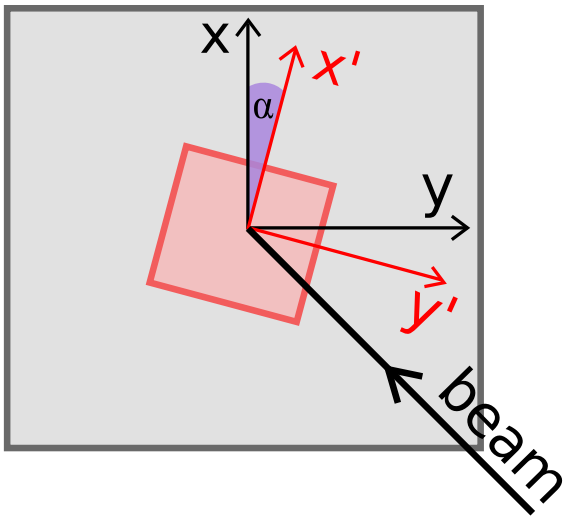
- New larger, more uniform SOI chip is fabricated and will be tested on July testbeam.
- Next chip with timing information is being designed.

THANK YOU FOR ATTENTION !

Alignment of SOI pixel chip

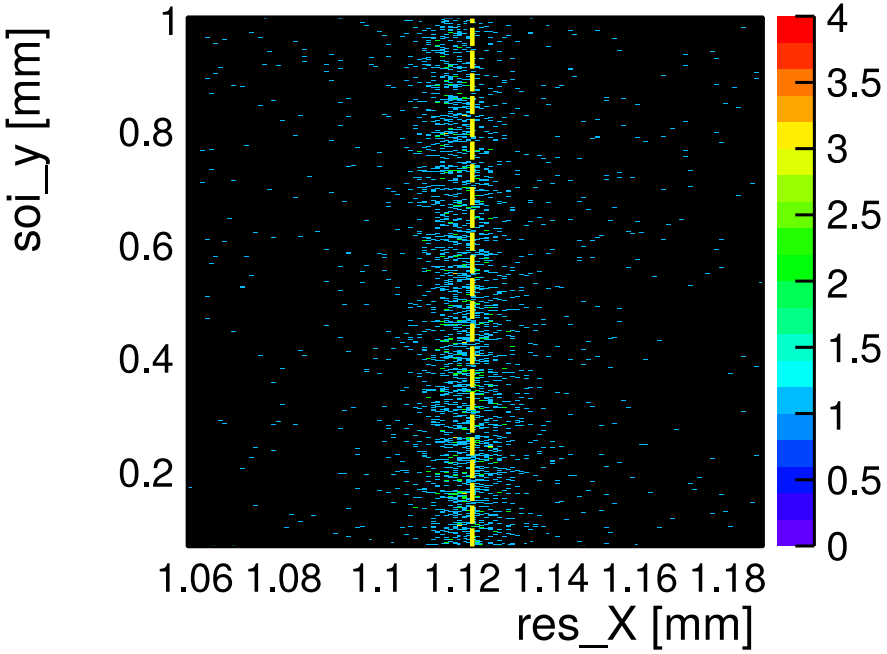
Two alignment methods were applied:

1. slope of soi y hit position versus residuum x,
2. minimum residuum versus rotation angle.

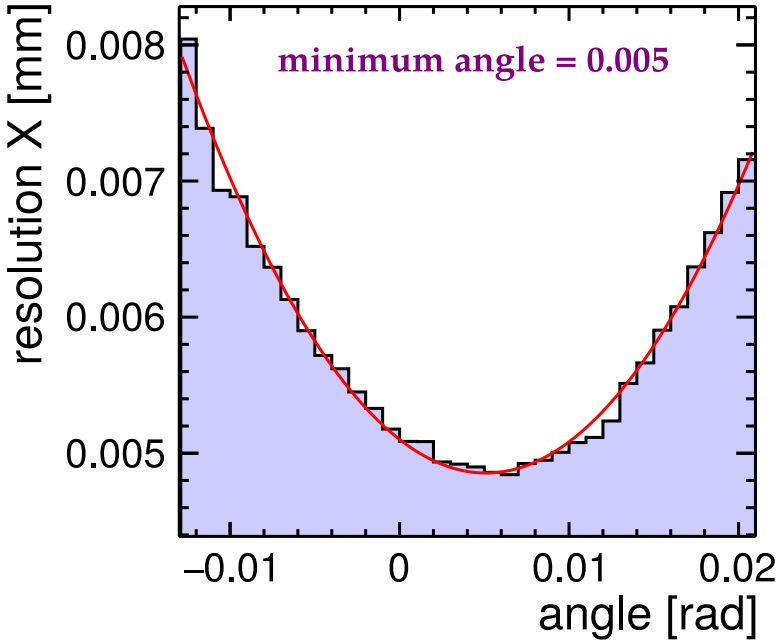


- both methods gave the same angle
- rotation angle is:
  $\alpha_{rot} = 0.005\ [rad] = 0.285\ [deg]$

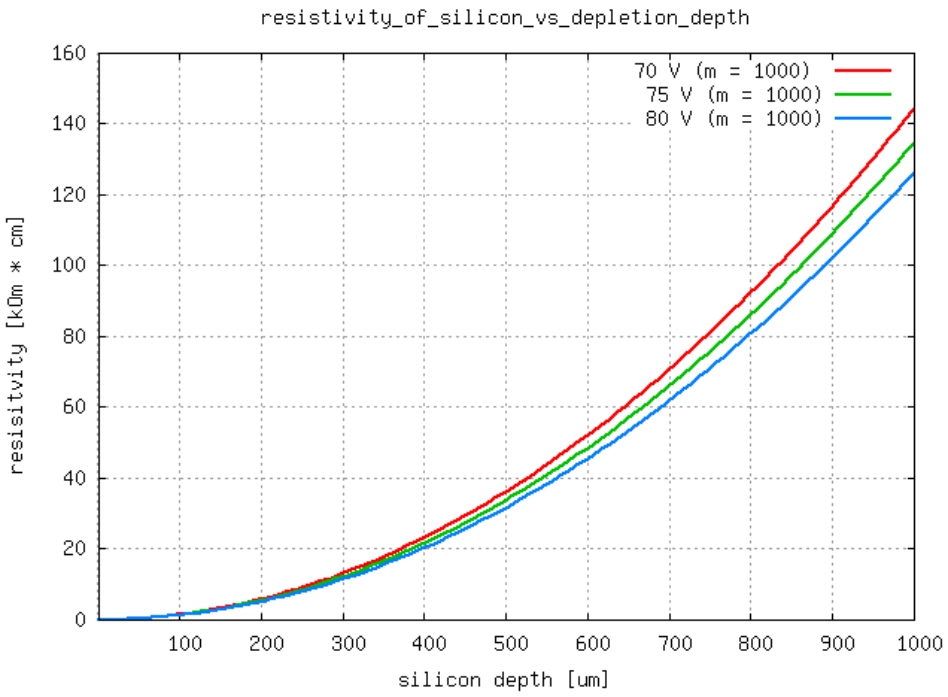
1 METHOD:

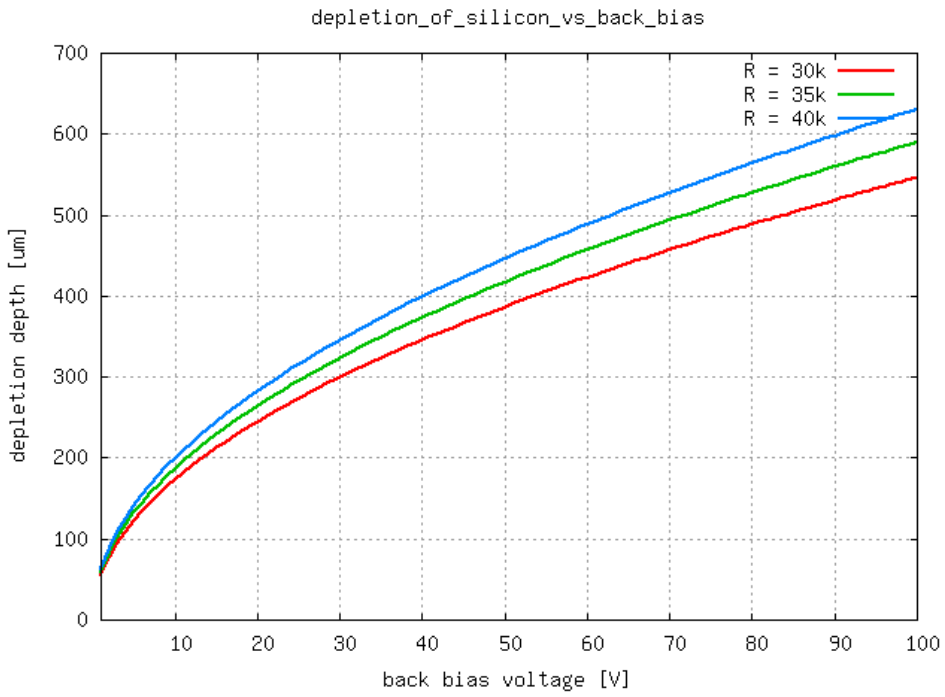


2 METHOD:



Resistivity of the wafer and depletion depth





$$V_d = \frac{d^2}{2\epsilon\mu\rho_d} \quad (1)$$

$$\rho_d = \frac{d^2}{2\epsilon\mu V_d} \quad (2)$$

$$d = \sqrt{2\epsilon\mu V_d \rho_d} \quad (3)$$