



Xbox-3 Commissioning

Ben Woolley

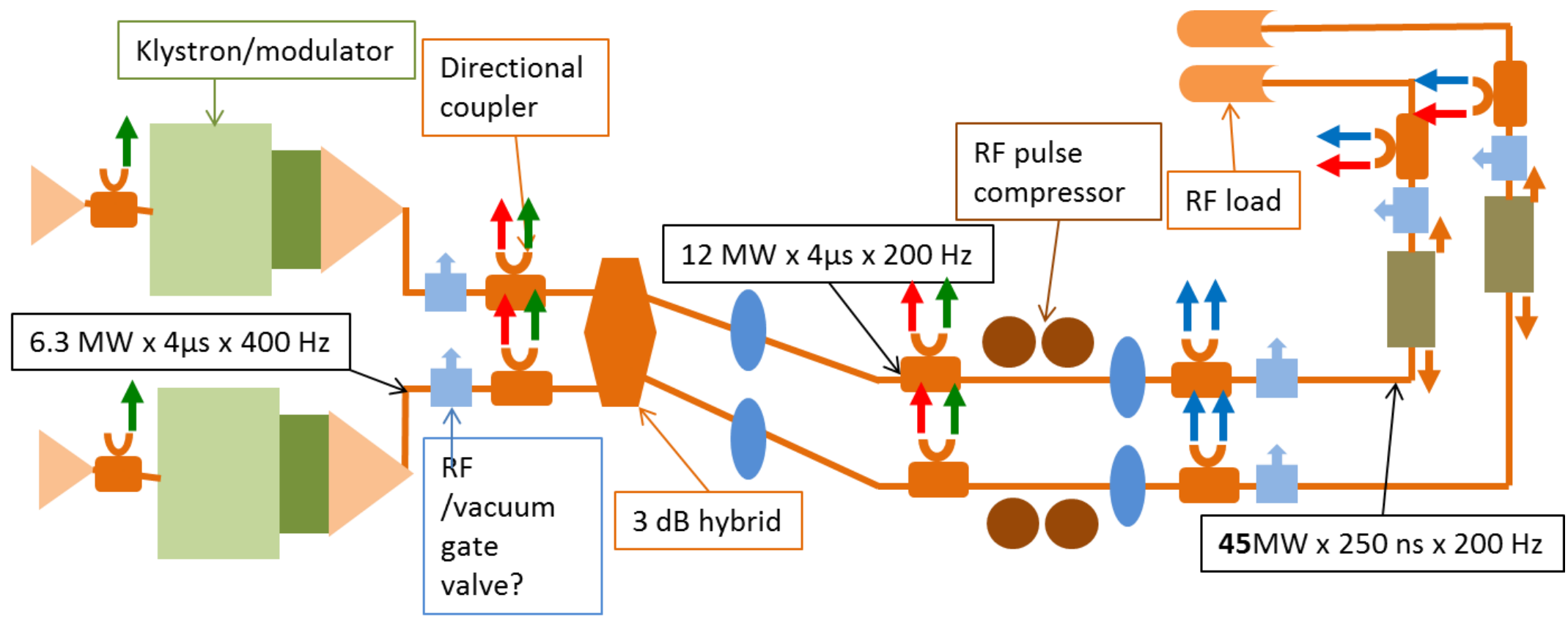
CLIC Workshop 2017

CERN, Switzerland

06/03/2017

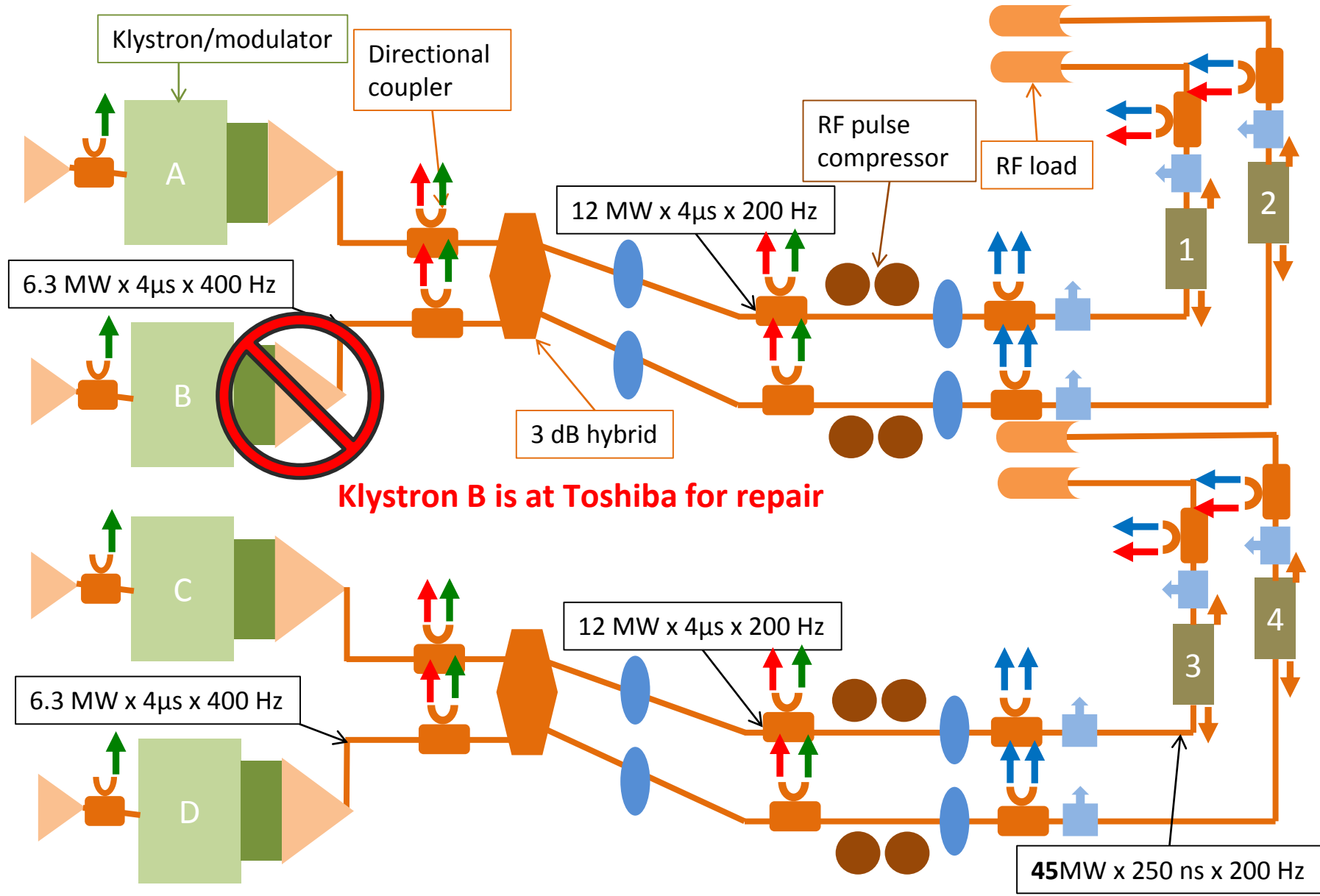
- Test stand specifications and layout
 - ≤ 250 ns pulse, ≥ 45 MW, ≤ 400 Hz pulse repetition rate, 4 test slots.
- Control systems
 - Down mixing and digitization.
 - LLRF signal generation and up mixing.
 - Power control: Pressure and BDR.
 - Pulse compressor tuning.
- Commissioning
 - New high power RF components.
 - Klystron B issues.
 - First Pulses line CD/34.
 - Conditioning progress.
- Structure installation
- Next steps
- Conclusion

Xbox-3 Layout

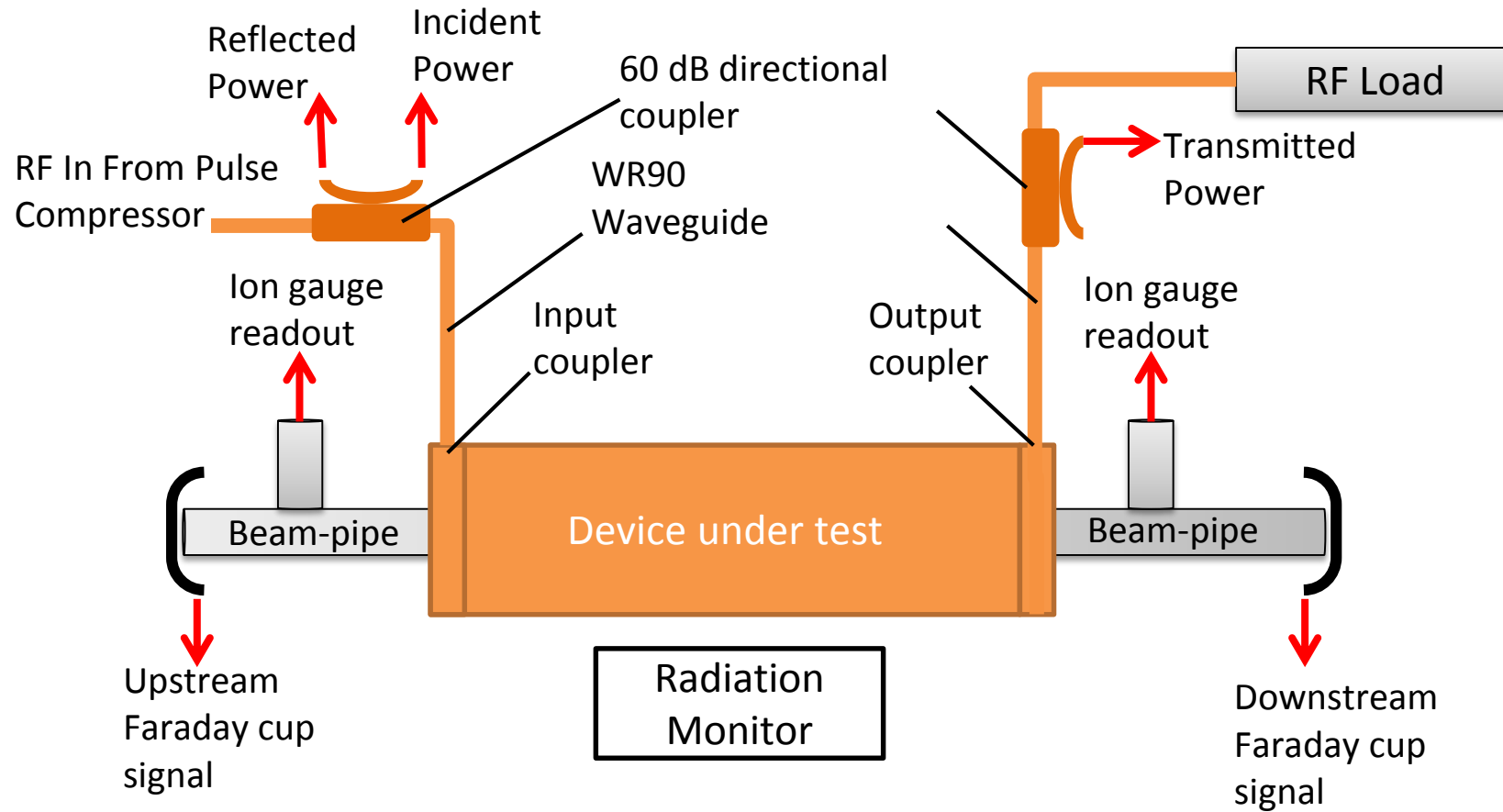


- ↑ x4:2 Faraday Cups (250MSPS ADCs) → Used to interlock the system and are interesting for high gradient physics.
- ↑ x6 Log detectors ~50MHz Bandwidth, 45dB dynamic range (250MSPS ADCs) → Used for interlocking the system.
- ↑ x6 FPGA IQ demodulation 400-MHz AC (228MSPS ADCs) → Phase and amplitude needed for reliable line/phase switching.
- ↑ x6:3 FPGA IQ demodulation 400-MHz AC (1600MSPS ADCs) → Most interesting signals for BD physics.

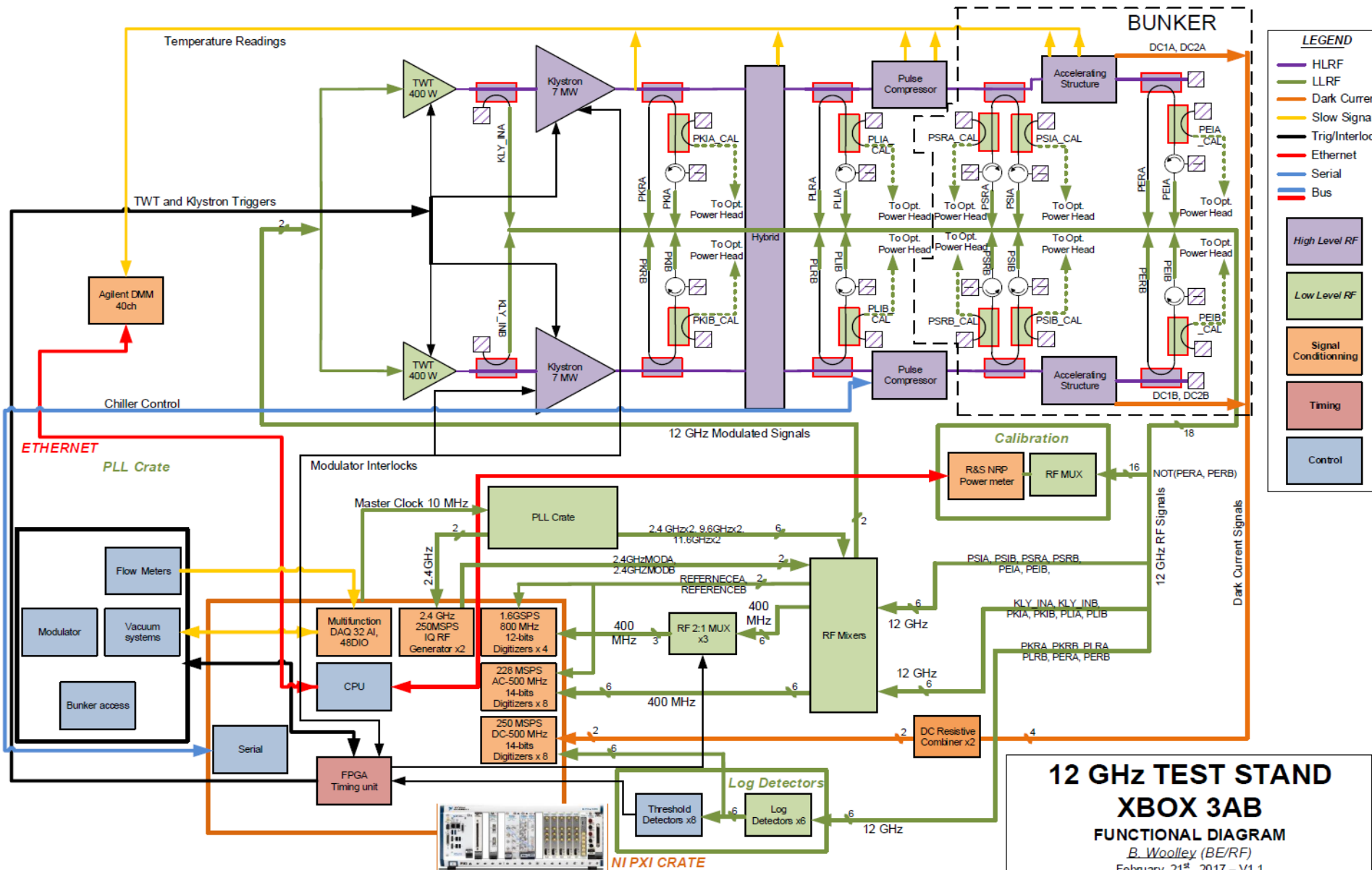
Xbox-3 Layout



Diagnostics of the DUTs



Full Layout and Diagnostics for 1/2 of Xbox-3



**12 GHz TEST STAND
XBOX 3AB
FUNCTIONAL DIAGRAM**
B. Woolley (BE/RF)
February 21st, 2017 – V1.1

ORGANISATION EUROPEENNE POUR LA RECHERCHE NUCLEAIRE
EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

Laboratoire Européen pour la Physique des Particules
European Laboratory for Particle Physics

NI-PXI Crate

- Allows up to 17 expansion cards to be used. Digitizers, RF generators, DMMs, serial interface etc. Plus powerful quad core controller.
- OS is NI's LabVIEW Real-Time, easily programmable in 'almost' standard LabVIEW language, with the stability and speed that real-time programming allows.
- Acquisition and interlock cards use FPGA interface for added reliability and speed.



CPU/Controller

RF Gen x2

DC 250MHz ADCs 8ch

AC 228MHz ADCs 8ch

AC 1600MHz ADCs 4ch

Timing/Interlock Card

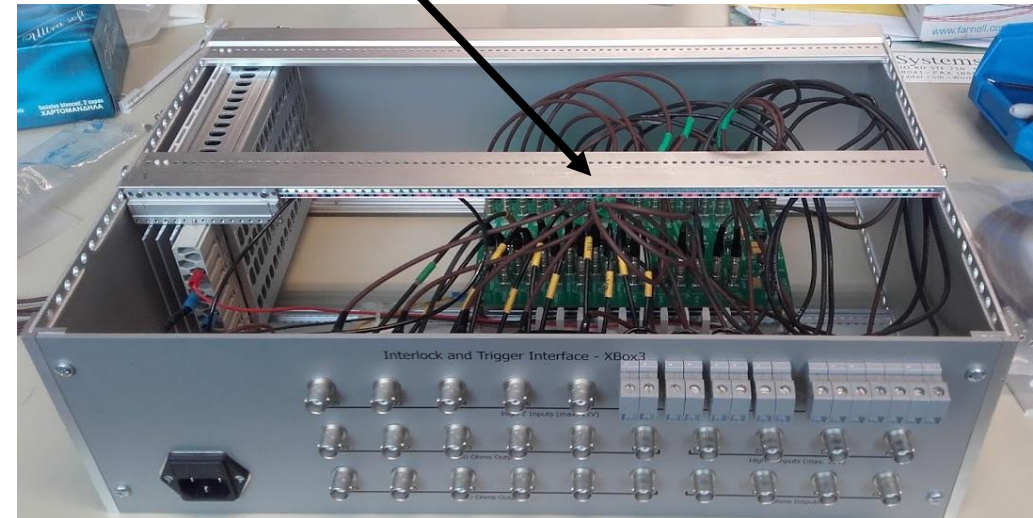
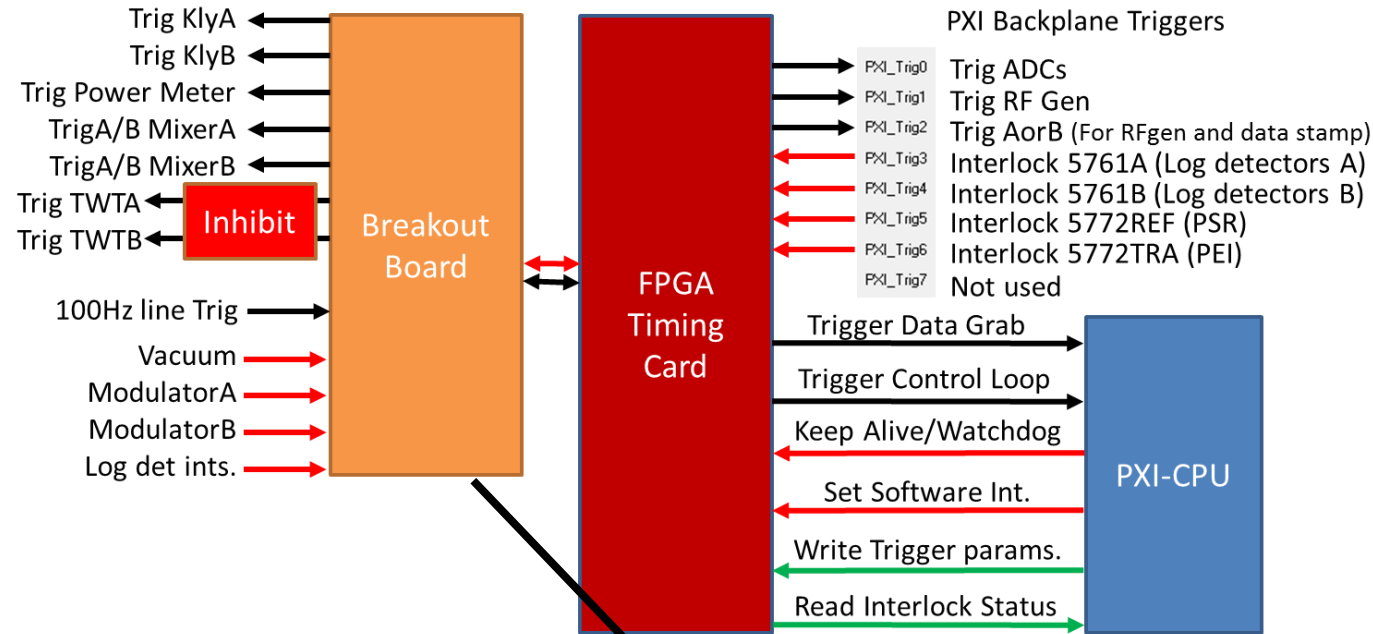
RS485 for Vacuum/Flow meters

RS232 for Chillers

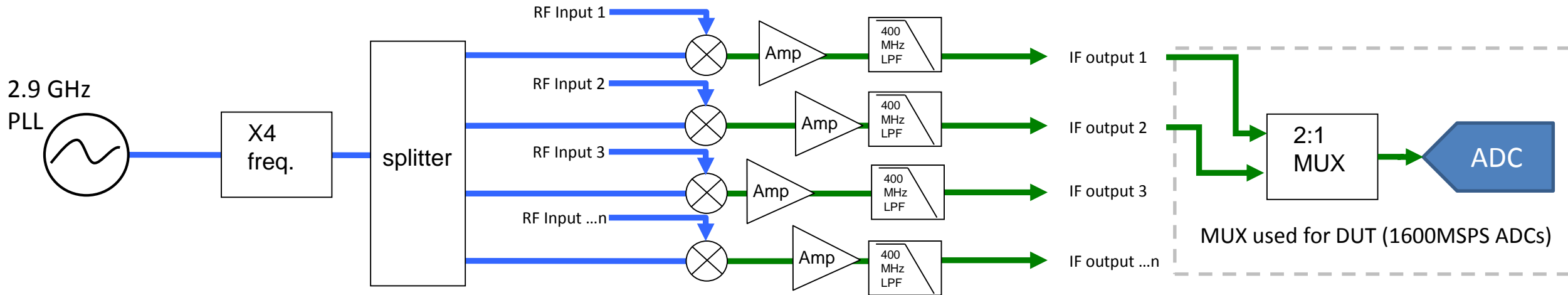
Spare Scope (BLMs?)

Safety, Interlocks and control Algorithms

- Main personal safety issue is X-ray radiation during operation.
 - Interlocks on the bunker door and klystron/modulator access doors stop modulator pulsing if opened.
 - Modulator interlocked is radiation levels are too high inside or outside of the bunker.
- Machine protection issue is from high vacuum and reflected power to the klystron.
 - Double interlocking of the vacuum; 10^{-5} mbar interlocks the modulator and 10^{-7} mbar interlocks the LLRF driver.
 - Reflected power is monitored by log detectors which stop the LLRF output if a certain level is breached.
- Interlock hardware
 - Modulator control system is used for radiation and access interlocks.
 - NI 6583 module attached directly to an FPGA in the PXI crate is the main trigger and interlock module at Xbox-3. This is used for all other interlocks; vacuum, RF, high temperatures, etc.



Down-mixing and Digitization

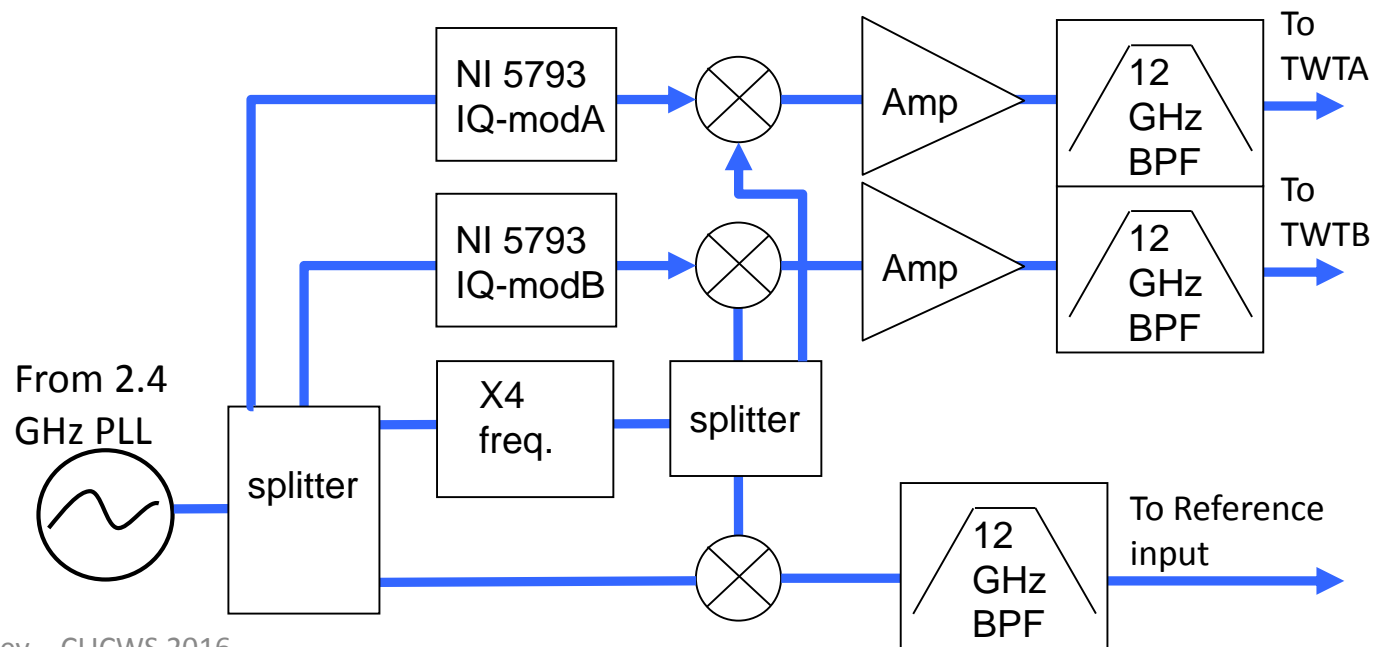


- 12 GHz signals are sent to a mixing crate containing a CERN built 2.9 GHz PLL (Stephane Rey) → x4 multipliers are used to produce 11.6 GHz.
- This is used to down-mix the signals to 400MHz IF.
- NI 5772 digitizer module over-samples at 1.6GSPS and FPGA IQ demodulation is used to obtain amplitude and phase for DUT signals.
- NI 5761 digitizer under-samples at 228MSPS and FPGA IQ demodulation is used to obtain amplitude and phase for the waveguide signals.

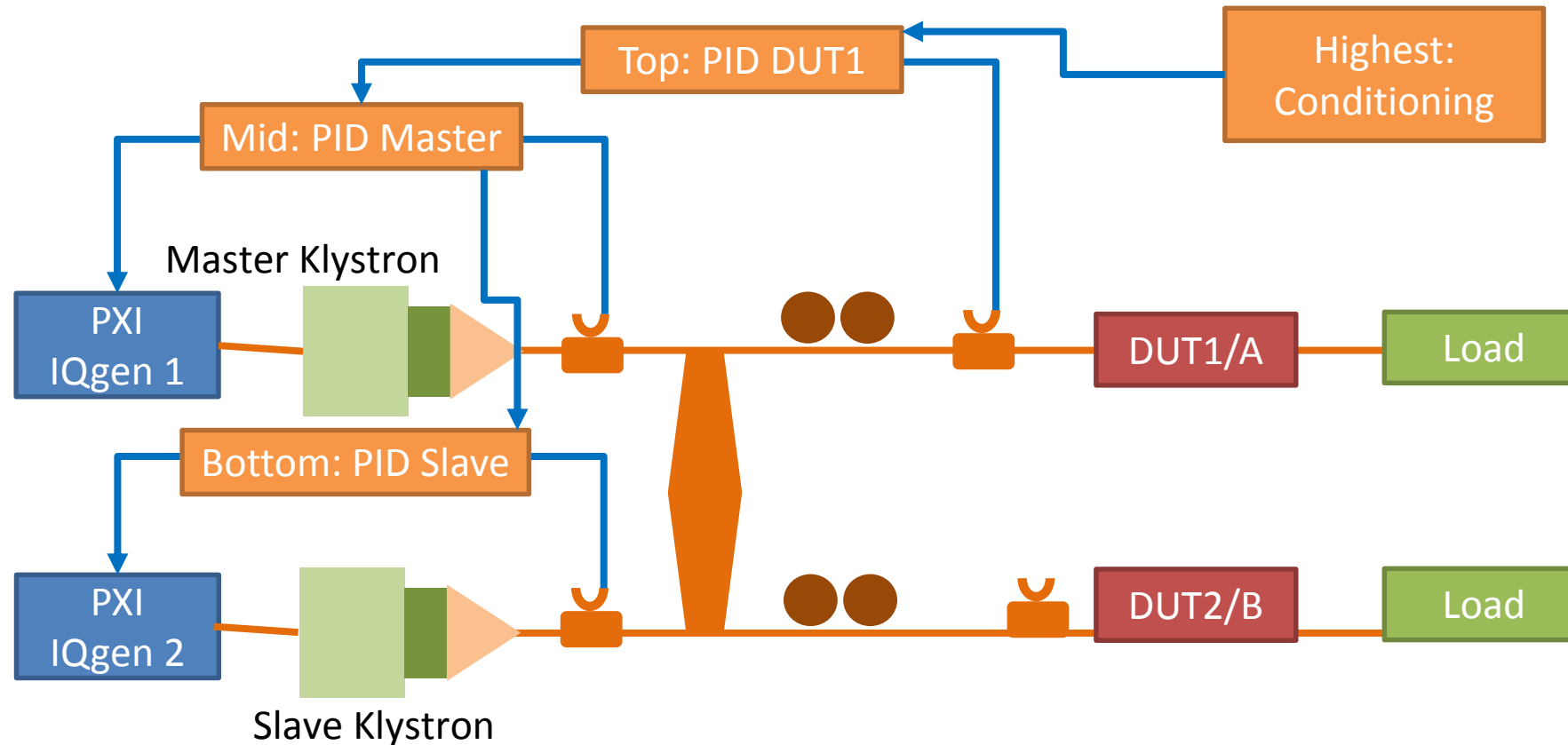


LLRF Generation and Up-mixing

- 2x Arbitrary signals in amplitude and phase needed, one for each klystron.
- NI 5793 IQ modulator with 200MHz bandwidth and 250MSPS IQ voltage generator is used to produce an arbitrary signal which can be varied in amplitude and phase at 2.4GHz.
- The signals are mixed up to 12 GHz using a mixer with a 9.6GHz input.
- Automatic control of low-level signal → Feedback on acquired signals to obtain correct power level and pulse shape.
- Pulse to pulse phase switching is needed → Each card stores 2 different pulses: one for line A/1 and another for line B/2.
 - Either of these pulses can be outputted by setting a hardware trigger high or low (PXI_Trig2).

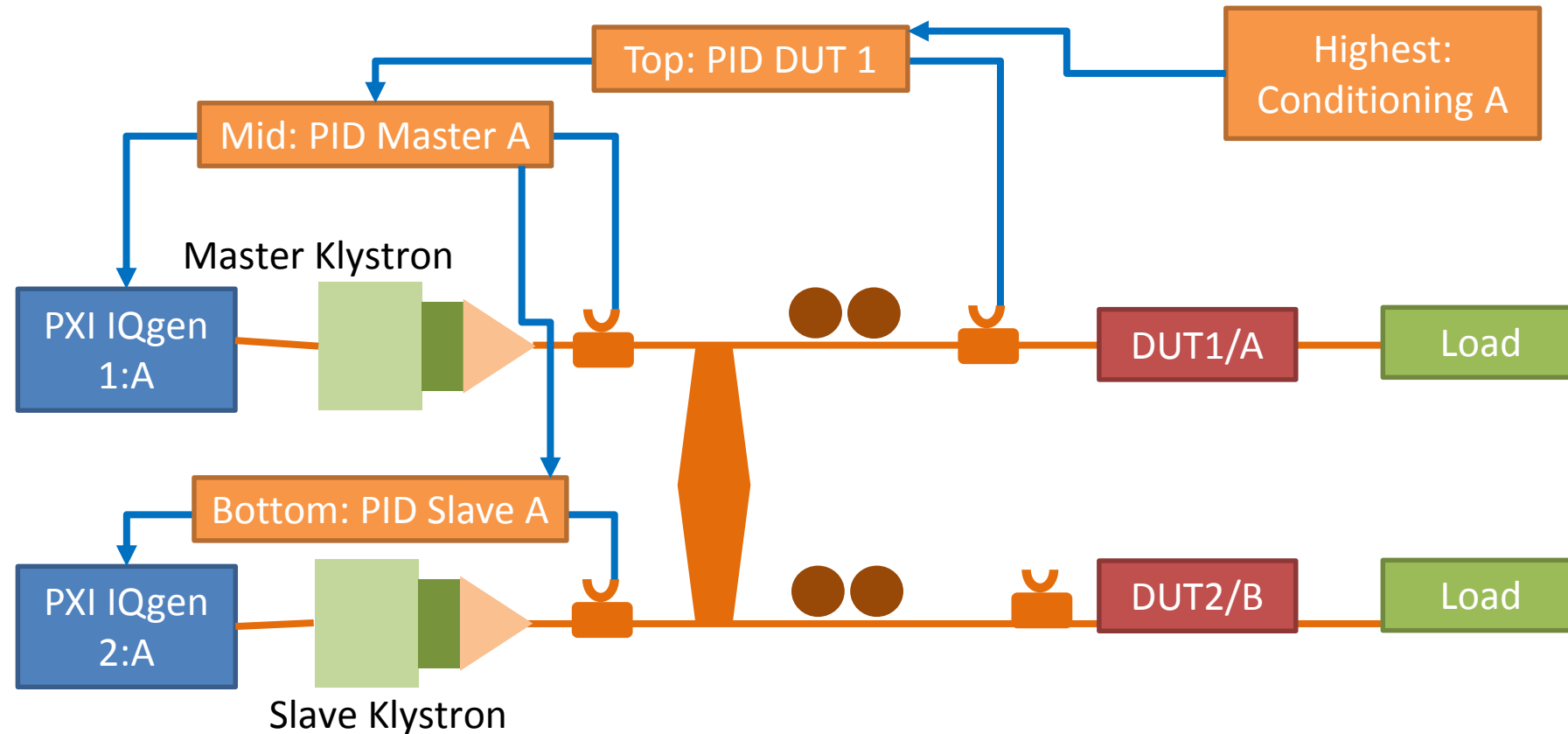


RF feedback algorithms: POWER



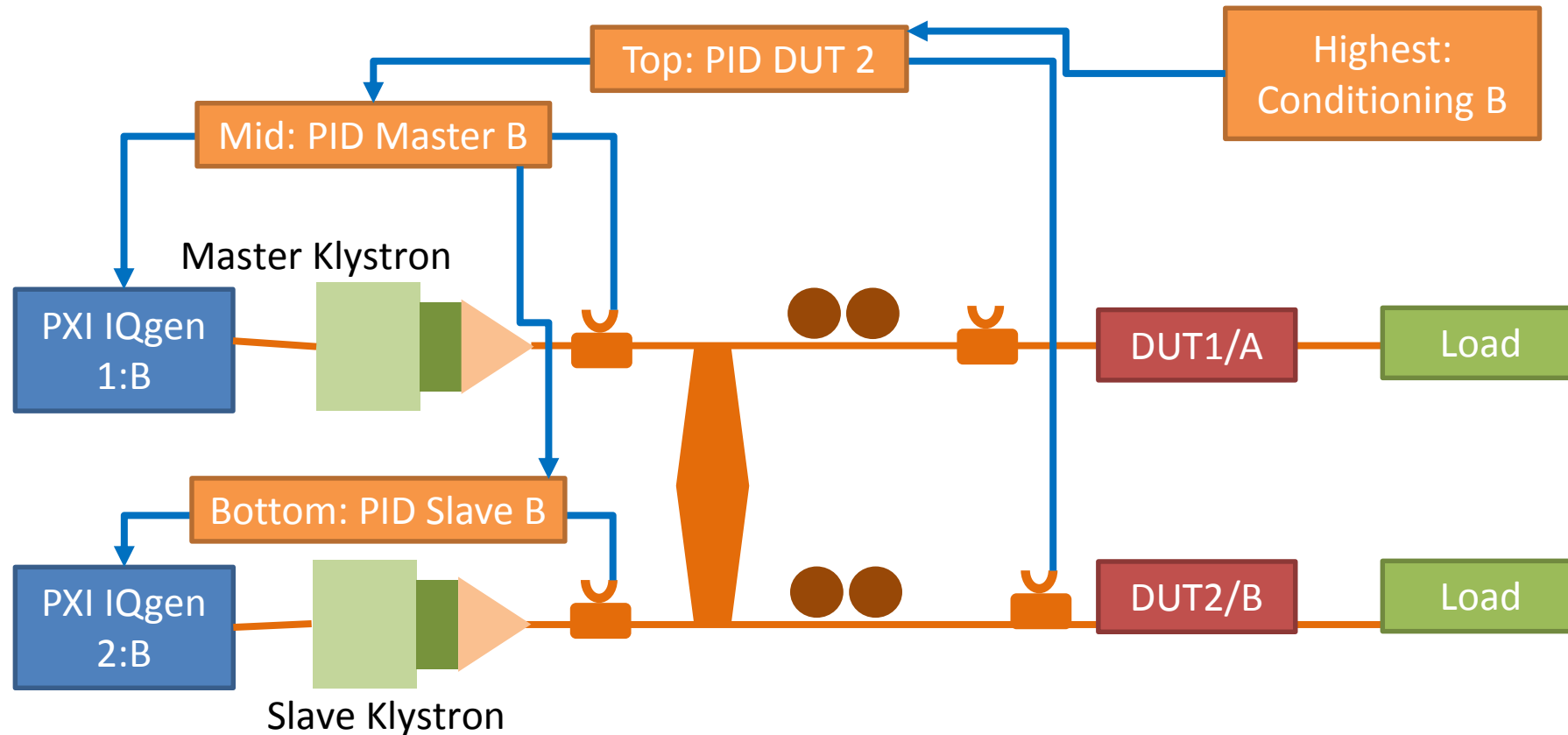
- Top: The DUT PID requests more/less power from the Master PID depending on the power level to the DUT.
- Mid: The Master PID requests more/less power from the PXI IQgen 1 card depending on the power level to the master.
- Bottom: The Slave PID tries to make the output power of the Slave klystron equal to the master klystron by controlling the power of PXI IQgen 2.

RF feedback algorithms: POWER A



- Top: The DUT PID requests more/less power from the Master PID depending on the power level to the DUT 1.
- Mid: The Master PID requests more/less power from the PXI IQgen 1 card depending on the power level to the master.
- Bottom: The Slave PID tries to make the output power of the Slave klystron equal to the master klystron by controlling the power of PXI IQgen 2.

RF feedback algorithms: POWER B

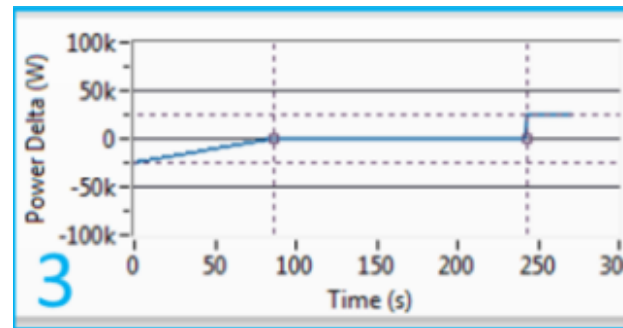


- Top: The DUT PID requests more/less power from the Master PID depending on the power level to the DUT 2.
- Mid: The Master PID requests more/less power from the PXI IQgen 1 card depending on the power level to the master.
- Bottom: The Slave PID tries to make the output power of the Slave klystron equal to the master klystron by controlling the power of PXI IQgen 2.

Conditioning Control Algorithms

1. Pulse length and LLRF frequency are set:
 2. Fast → pulse to pulse
 - PID loop on the incident power to the structure
 3. Medium → seconds-minutes
 - increase power by 10kW every few minutes if no BD
 - reduce power by 10kW if successive BDs too close in time
 4. Slow → hours
 - BDR measurement and stop power increase if it is too high
 - BDR measurement performed across a moving window of approx. 1M pulses.
 - Use PID loop using the system pressure as a process variable.
 - Increase in pressure results in a reduction of power and vice versa.

OR →



Pulse Compressor Pulse Flattening

The flat-top data is fitted with a 5th order polynomial.

The following feedback is applied.

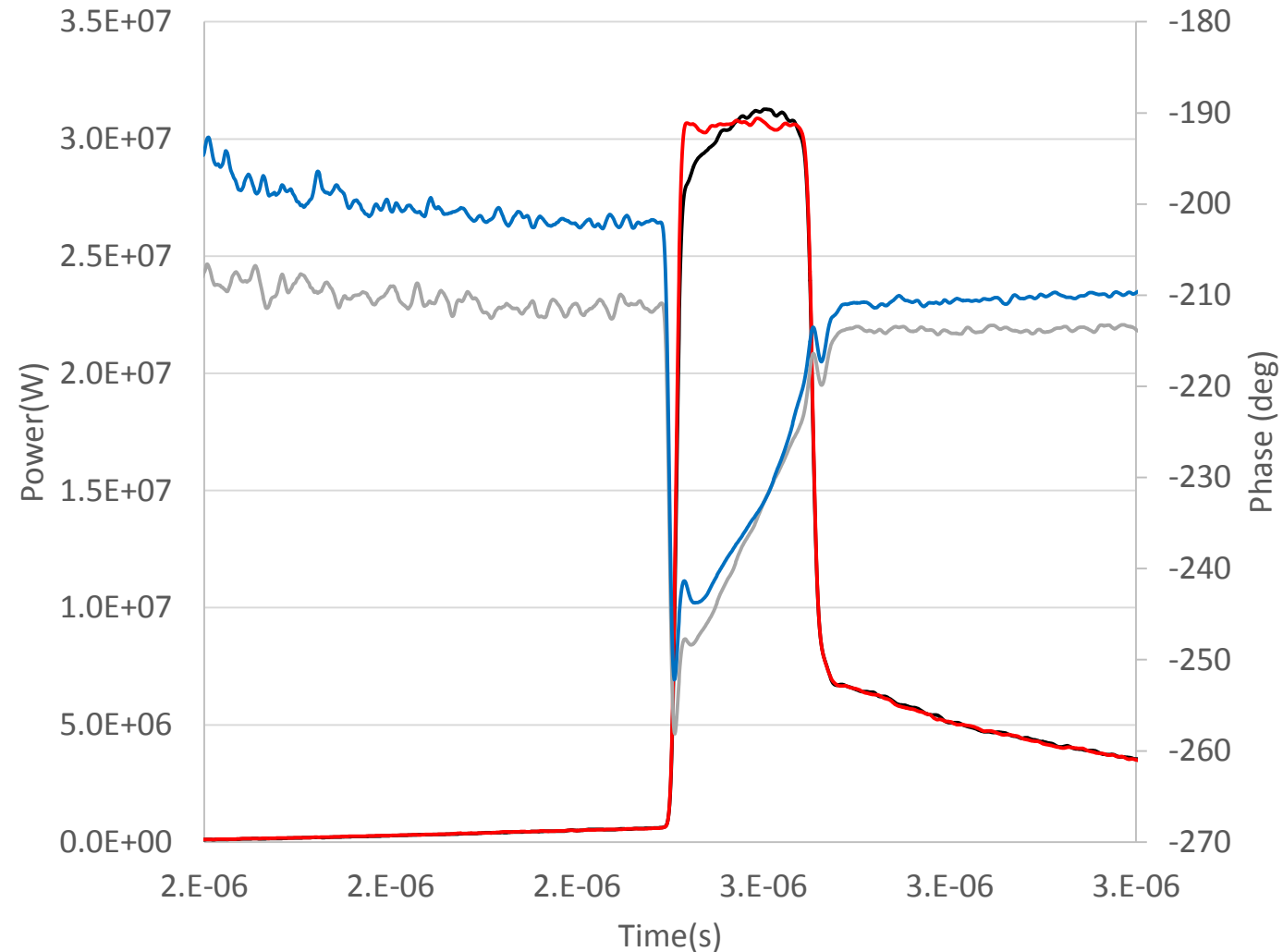
$$\Phi_{n+1} = \Phi_n + g_p(A_{SP} - A_n) + g_d(dA_n/dt)$$

A_{SP} amplitude set point

A_n current amplitude

g_p proportional feedback gain

g_n differential feedback gain



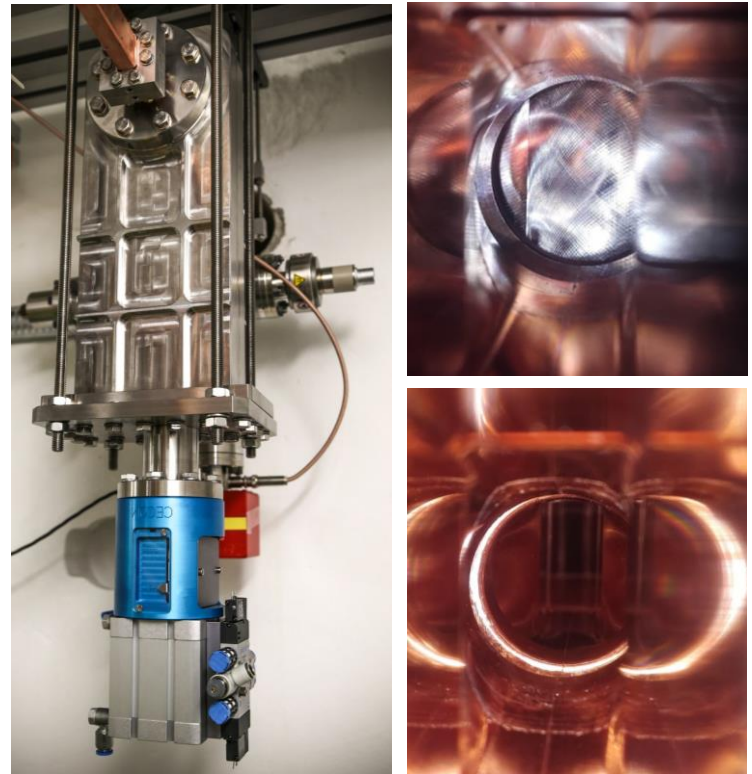
— Power - Output Power Linear Ramp — Power - Output Power PD
— Phase - Output Phase Linear Ramp — Phase - Output Phase PD

New RF components

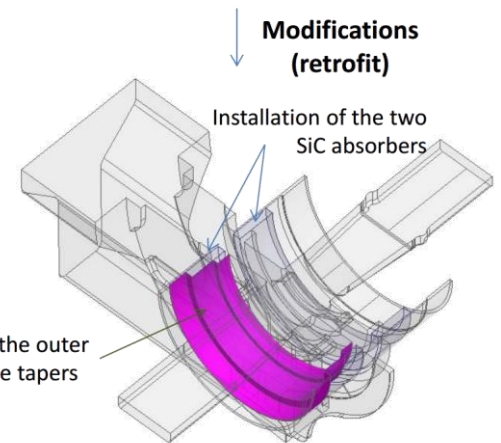


Pulse Compressor
(same as Xbox-2 but with lower coupling)
See: Matteo Volpi this pm.

B. Woolley – CLICWS 2017



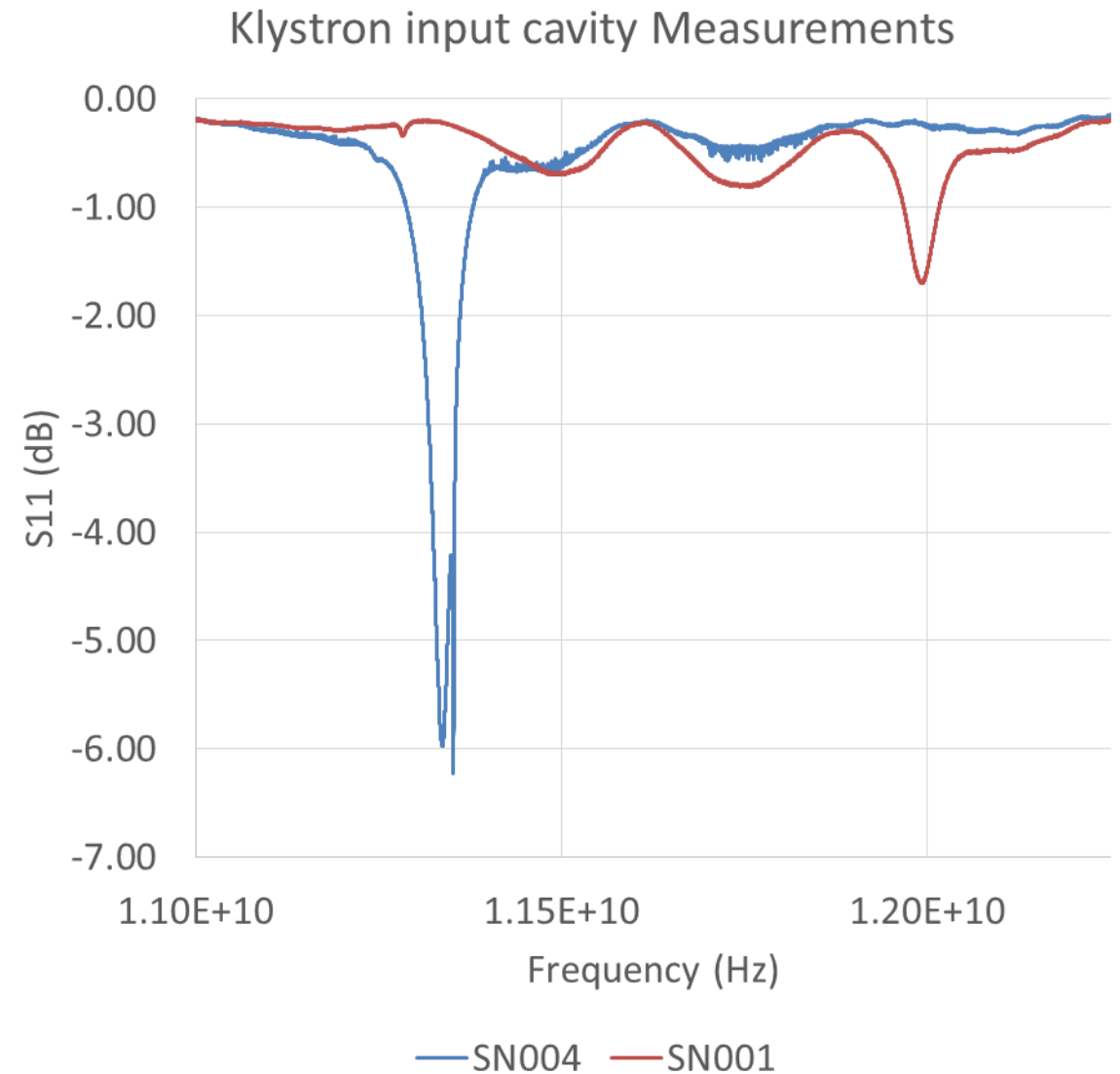
Modified RF gate Valve (With SiC absorber)



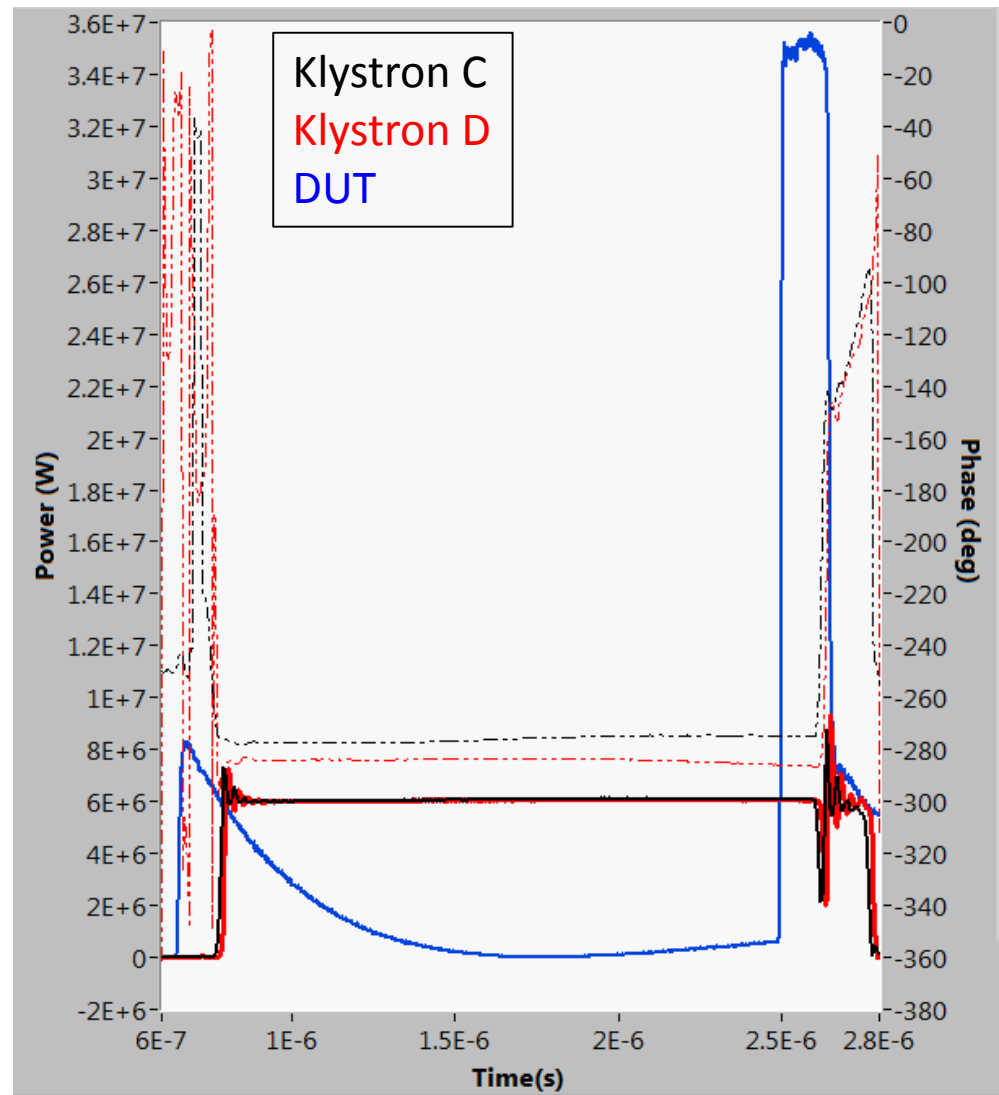
Compact 3D printed Load
See: Alexej Grudiev Tues pm.

Start-up: Klystron B issues

- During the first pulsing we noticed Klystron B (SN004) had a very low gain.
- Only producing a few 10s of kW for input power of 60W. (Should be >5MW).
- Added an extra directional coupler to the klystron input to measure reflection from the input cavity → 100% reflection.
- Finally used a VNA to measure the klystron input cavity.
- Input cavity de-tuned by > 600 MHz.



Pulses in line C and D

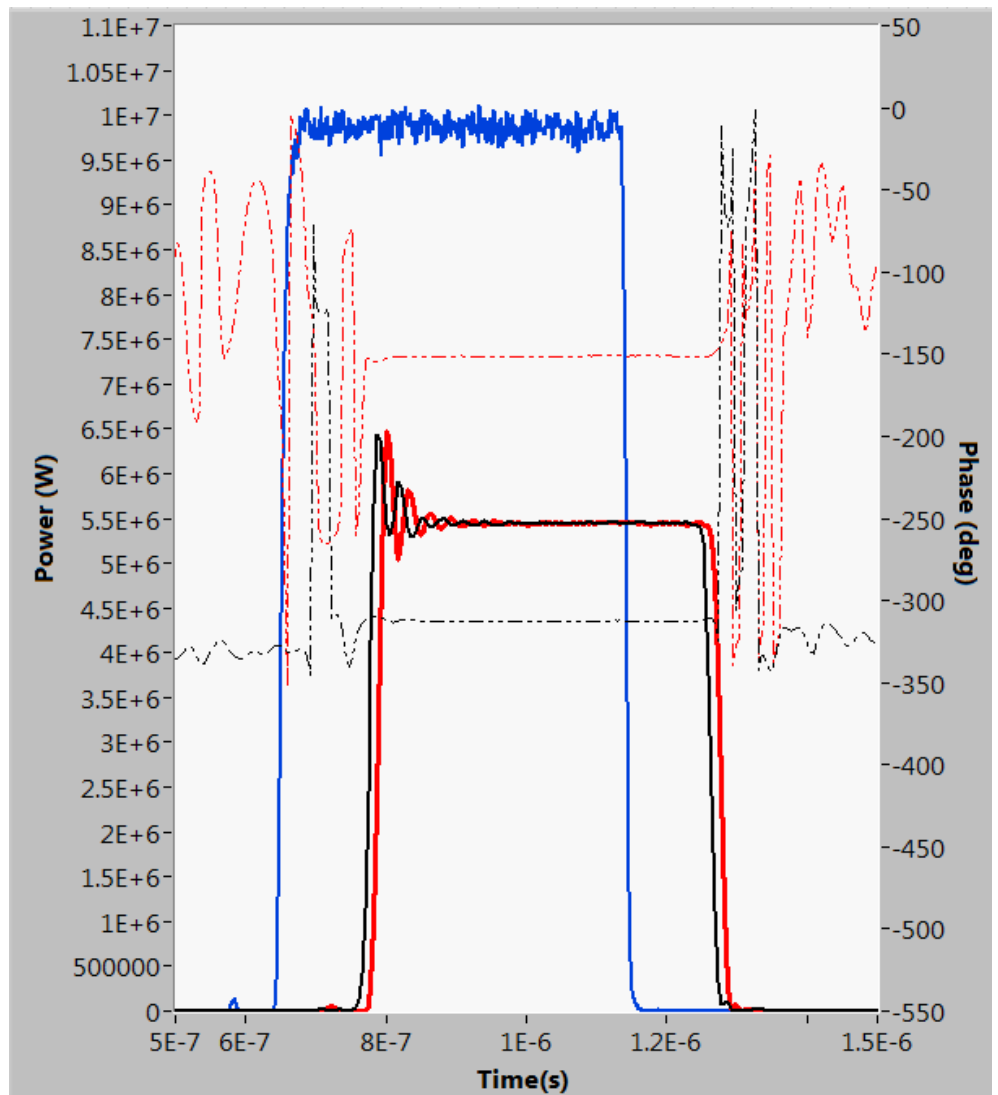


← Line C has pulse compressor so we can achieve higher power levels.

← The output phase difference from the klystrons is small $\approx 0^\circ$.

Line D has no pulse compressor; Lower power levels.

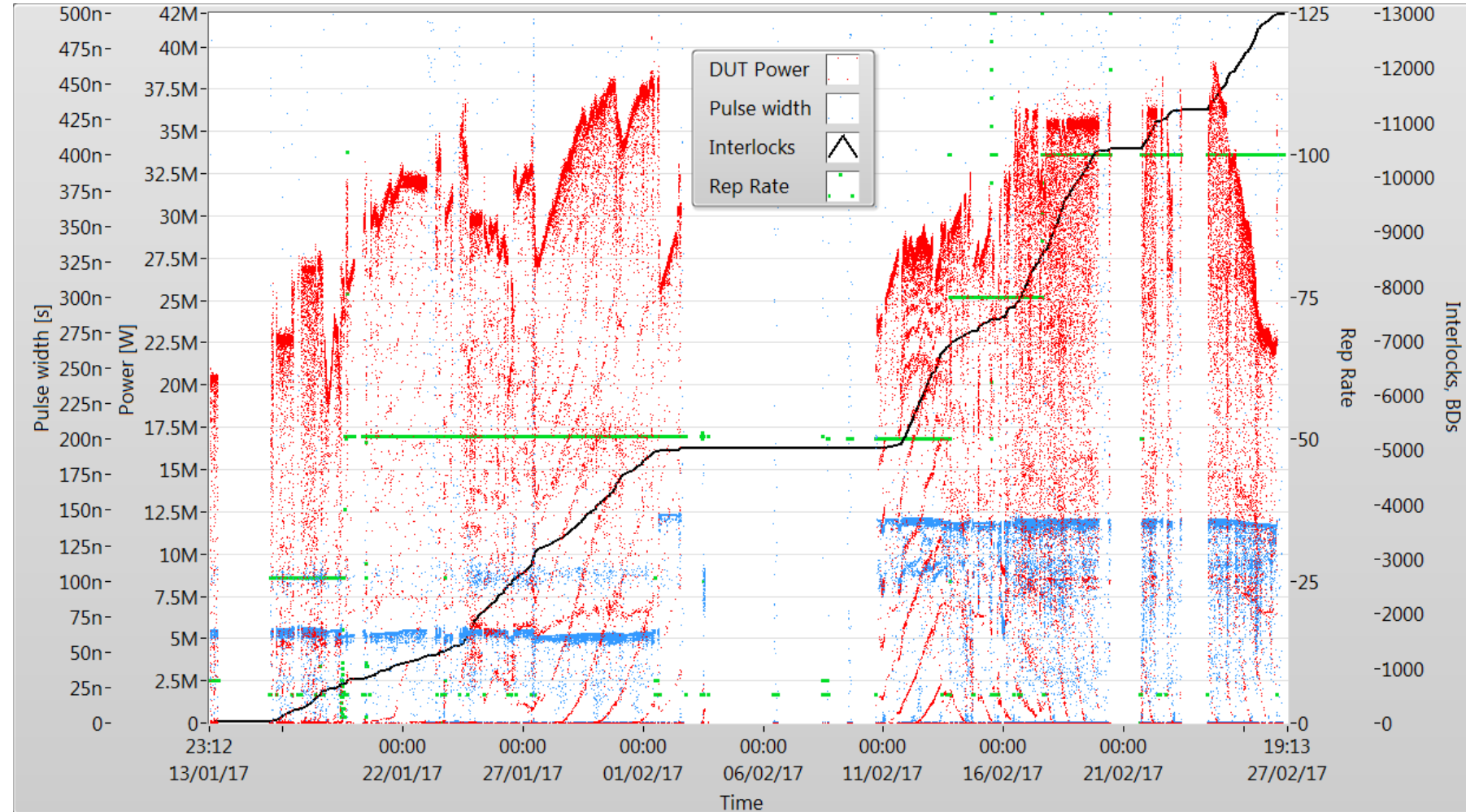
The output phase difference from the klystrons is $\approx 180^\circ$.



NOTE: Both of these pulses happened just 5 ms apart.

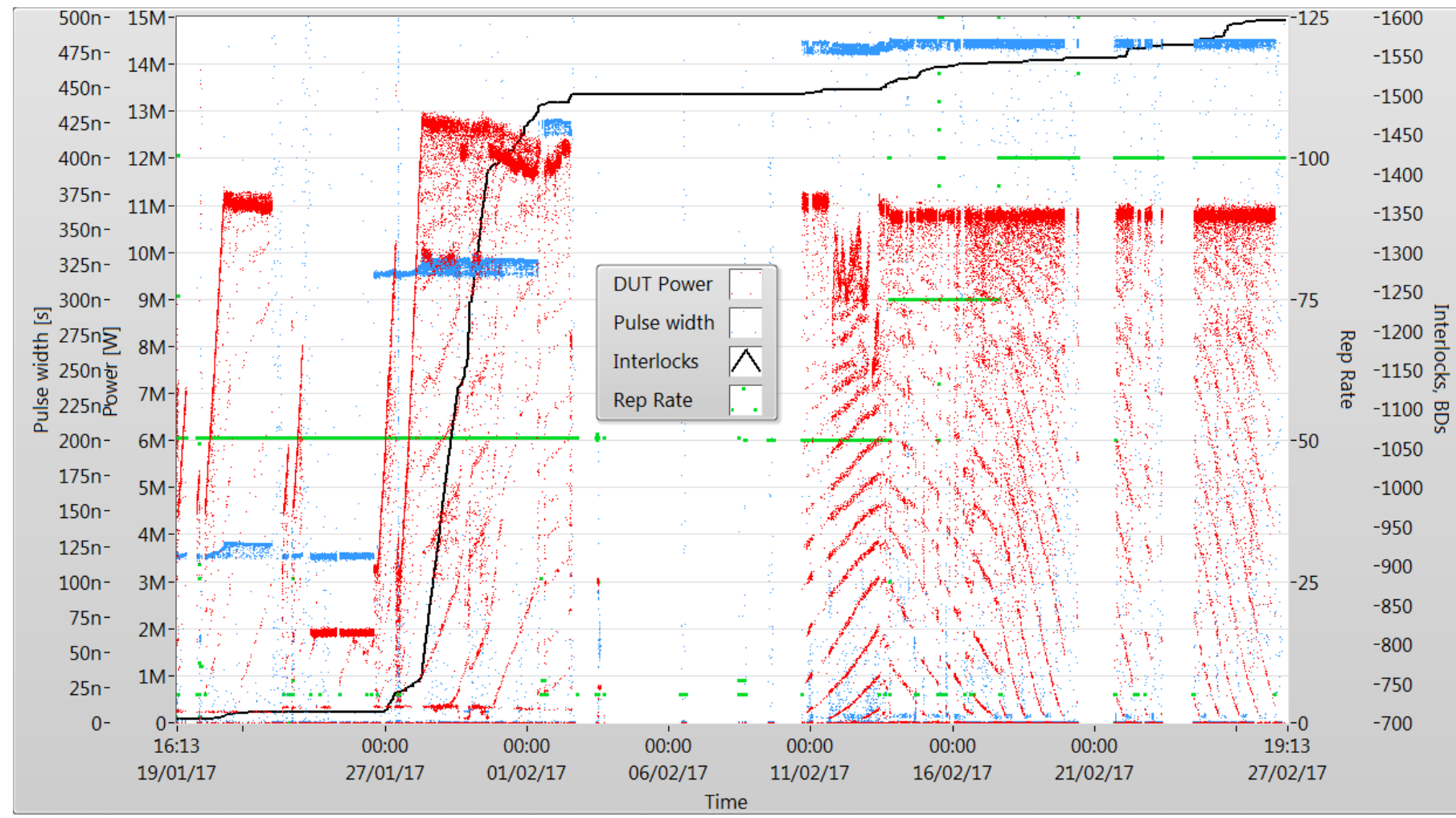
Conditioning plots: Line C/3

- Conditioning history for line 3.
- Main source of BDs/interlocks are the pulse compressor and the load.
- Started at 25Hz and 60ns pulse width.
- Later increased to 100Hz and 140ns pulse width.
- Final power reached ~40MW @ 140 ns.



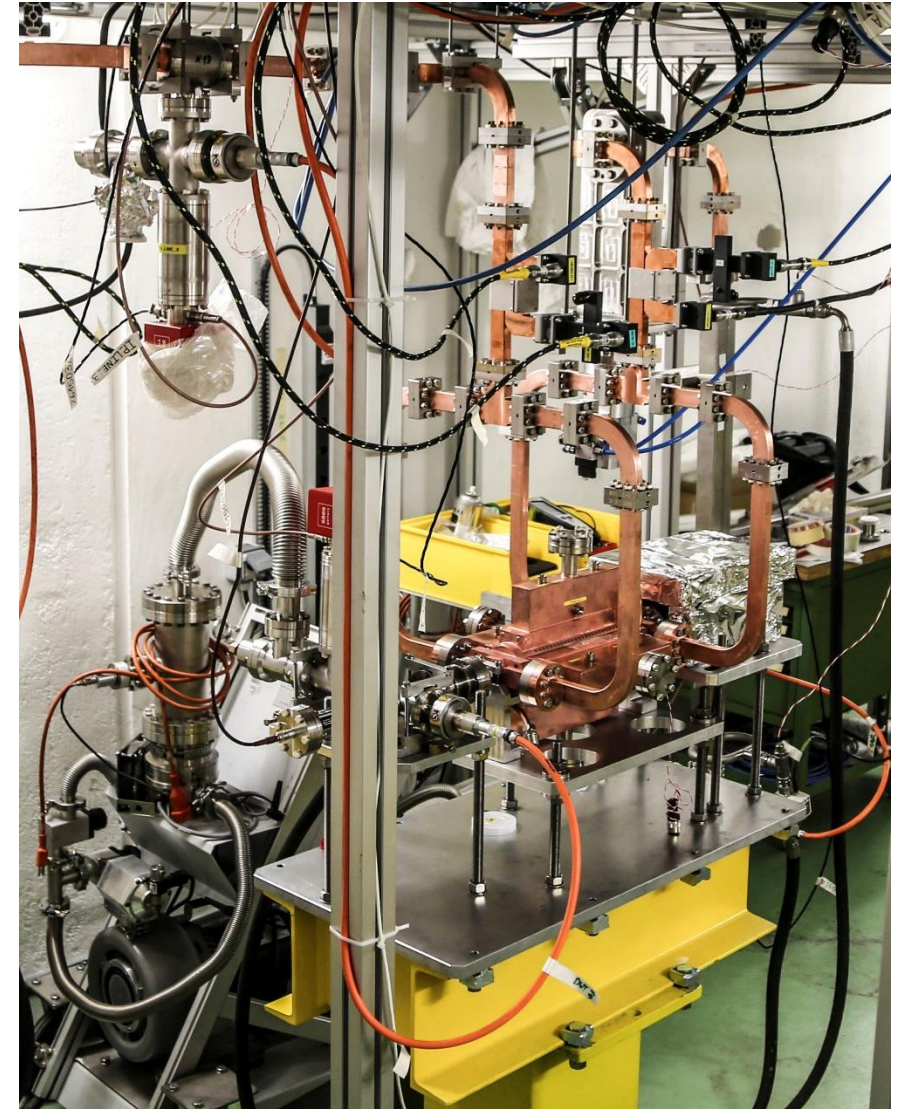
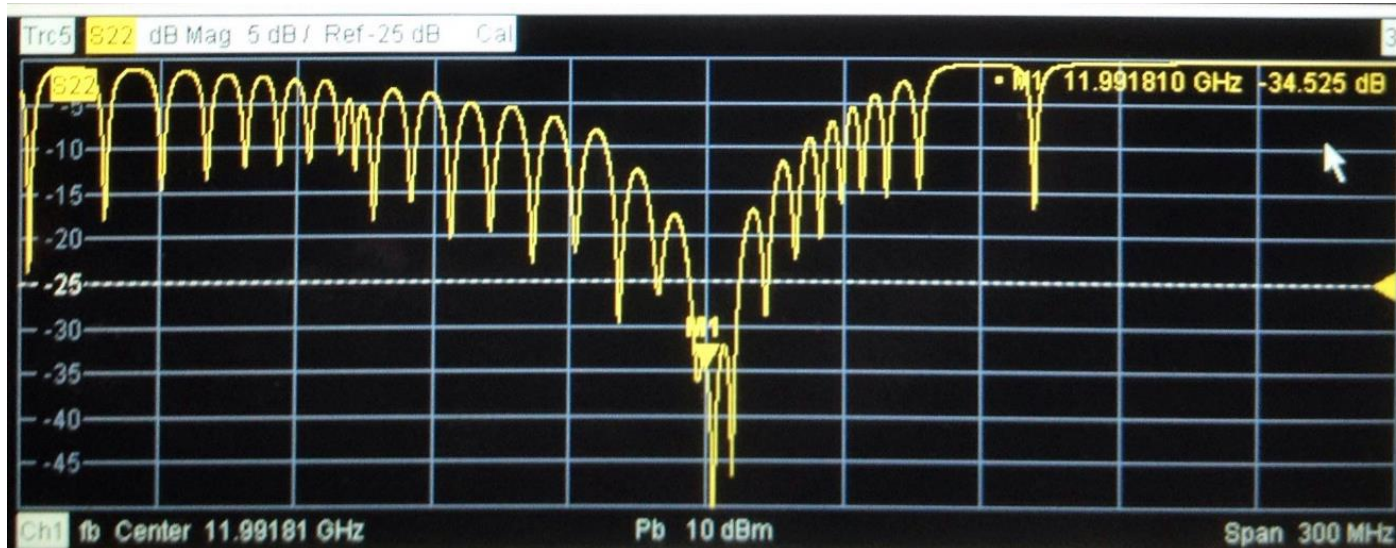
Conditioning plots: Line D/4

- Conditioning history for line 4.
- After initial conditioning period there were few interlocks.
- Started at 25Hz and 120ns pulse width.
- Later increased to 100Hz and 480ns pulse width.
- Final power reached ~11MW @ 140 ns.



First Structure installed: TD24SiC

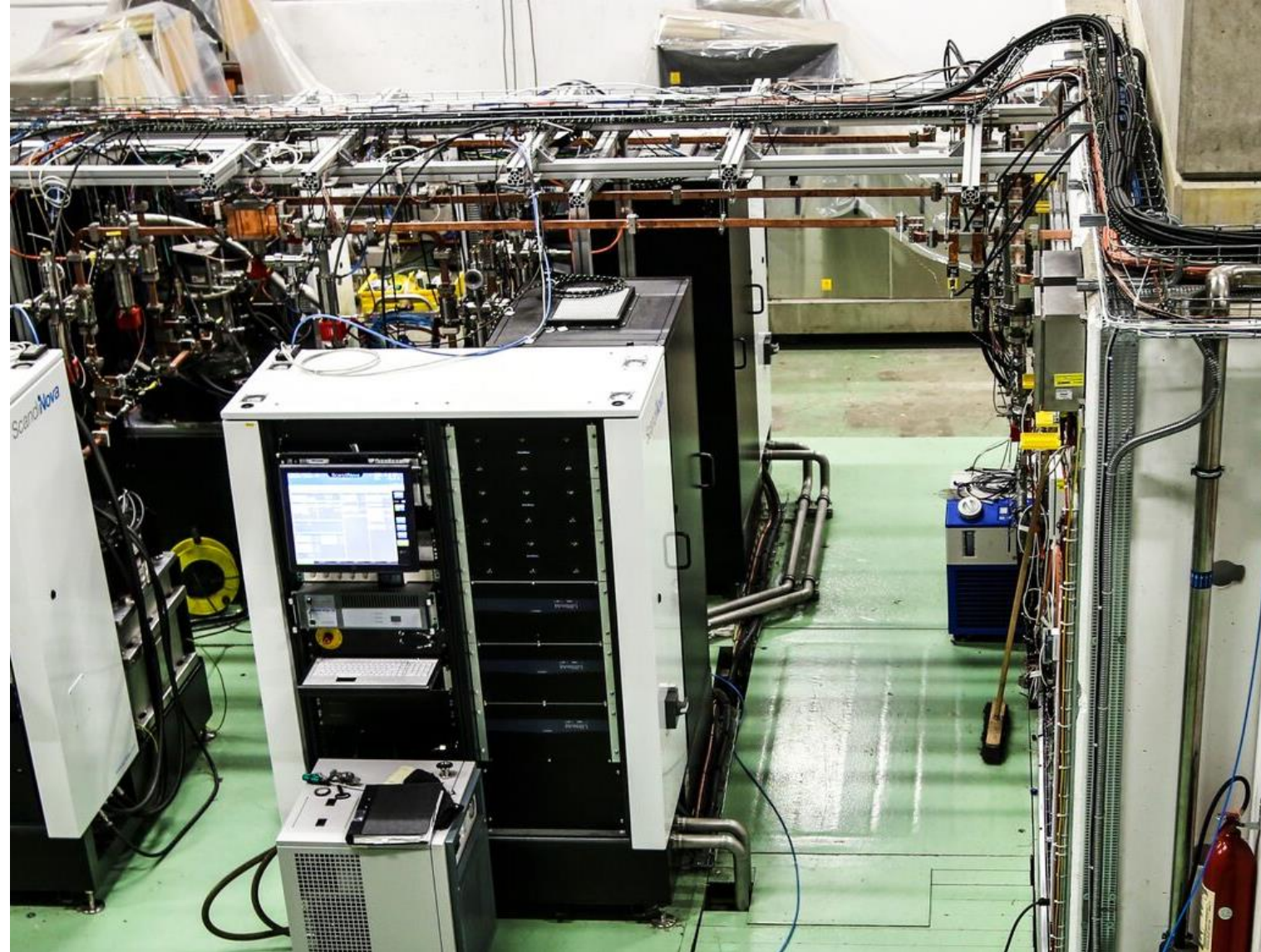
- Installed in line 3 as we have already proven that this line can produce ~ 40 MW @150 ns.
- S-parameters have been measured with splitters and waveguides already attached, to confirm good match (better than -34 dB!!)
- First test of a structure with absorbers on a CERN standalone test stand.



- Conditioning of line 4, Pulse compressor, RF gate valve + 3D printed load.
- After conditioning of line 4 is complete; Install PSI-built structure.
- Await delivery of klystron B from Toshiba.
- Install klystron B, 3rd and 4th pulse compressors.
- Commission lines A,B/1,2.
- Installation of other hardware: BLMs etc.

Conclusions

- All control hardware is installed and running as foreseen.
- Control algorithms work as expected: allow 24 hr, minimally attended operations.
- Successfully commissioned line 3, to 40MW, 150ns pulse width.
- A structure is installed in line 3, ready to be tested.
- Soon to have PSI-built structure installed.
- The Xbox-3 concept has been proven at high power.

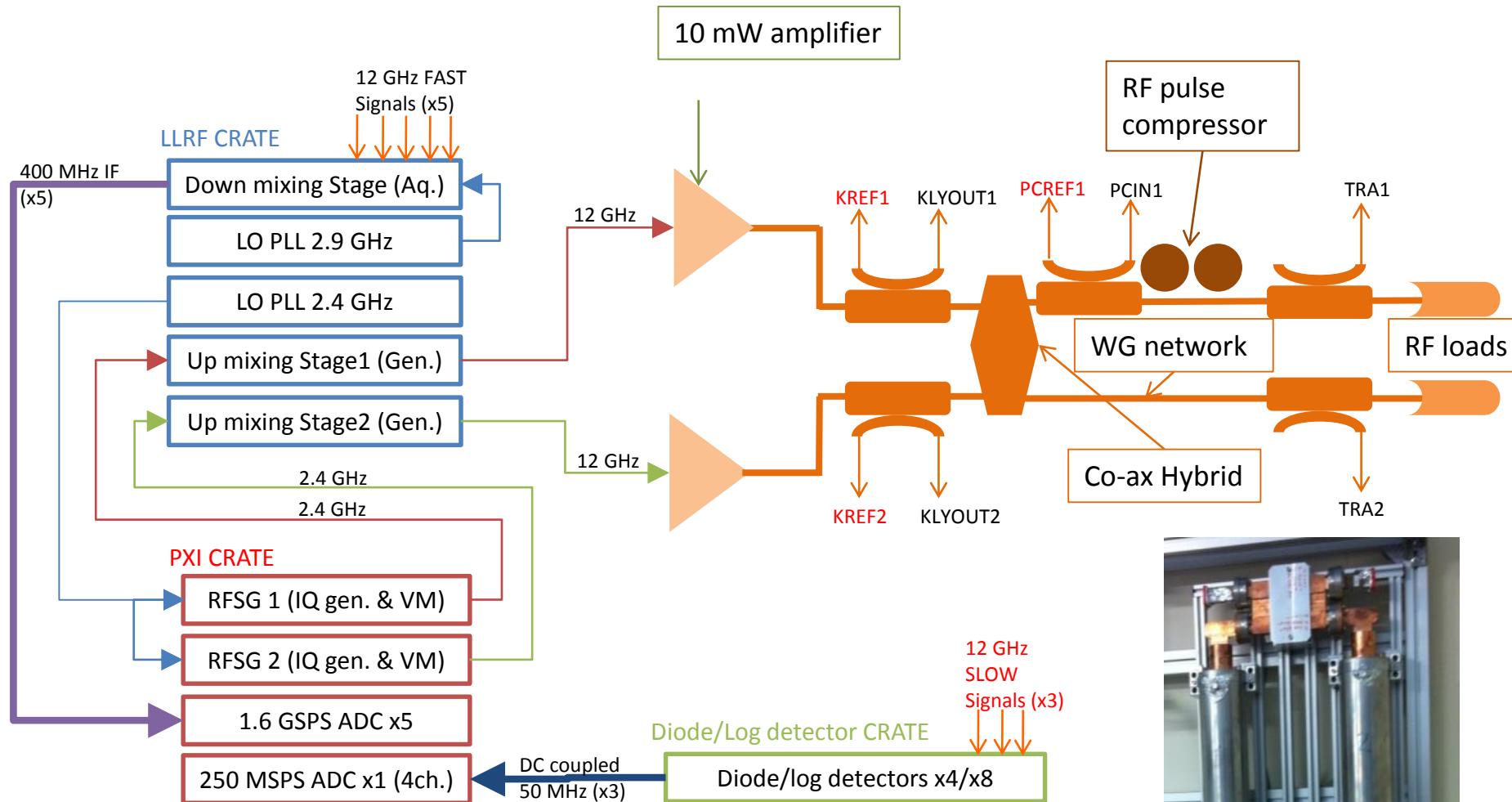


Thank you!

And also thanks to Matteo for the photos!

Extra slides

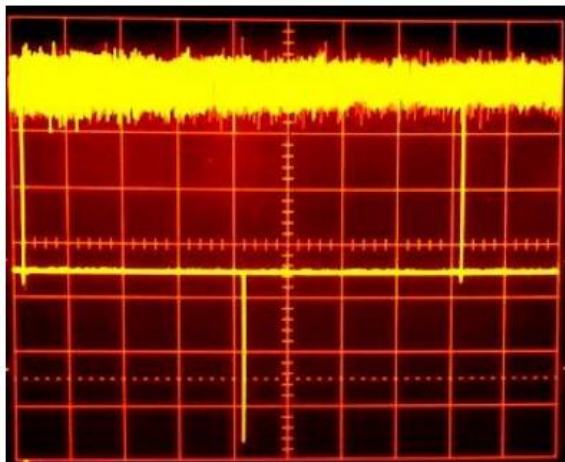
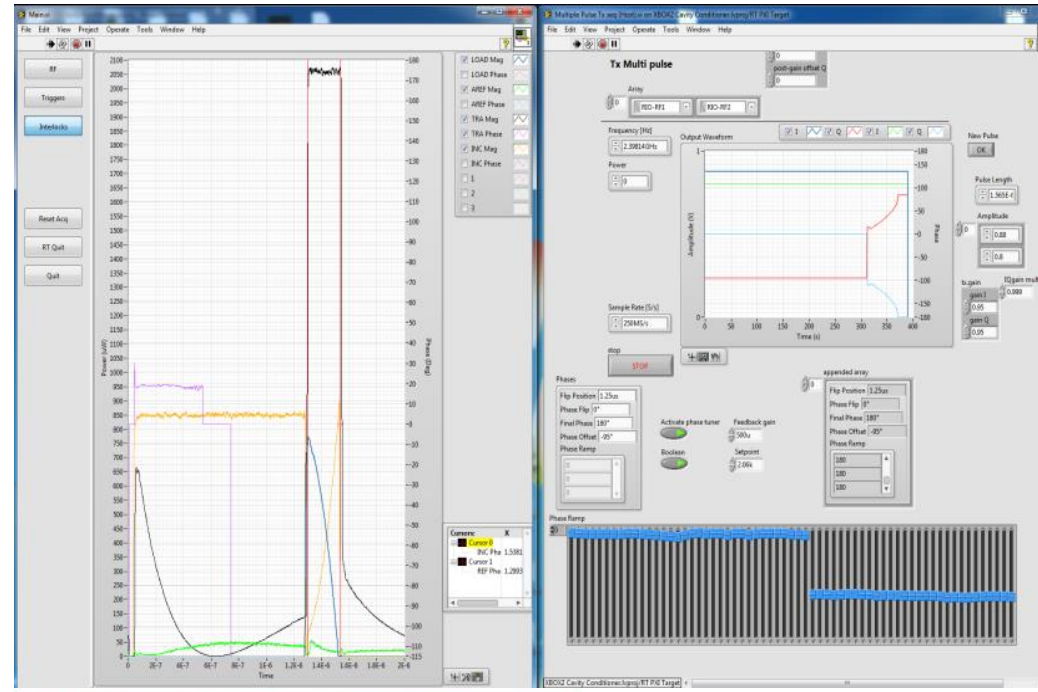
2-Way Combination Demonstration



PXI and LLRF crates are locked by 10 MHz reference

Results

- Concept of phase switching proved in 2013 with modified version of the Xbox-2 LLRF system.
- Low power hybrid and the Xbox-2 pulse compressor were used.
- Switching at 400 Hz was demonstrated (lower left).



Ch1

Ch2

0.5ms /div

