*Results of on-site performance tests on 20kW Solid State Wide Band Amplifier for the CLIC DB Front End at CERN**

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With thanks to P. Maus, S. Doebert, CERN

CLIC Workshop March 6-10, 2017

*** DAE (India) CERN Collaboration under NAT Protocol**

Motivation

•Under DAE (India) CERN collaboration in Novel Accelerator Technologies, of which CLIC collaboration is a part, a 20kW Solid State RF Power Amplifier R, D & D effort by RRCAT, Indore was agreed an as R & D and prototyping in this state of the art area.

•In CLIC WS 2016 we reported design, development and tests on 20kW SSPA completed using the design, fabrication, testing and qualification facilities available at RRCAT. The amplifier system was shipped to CERN in beginning of 2016 and has been reassembled after mechanical support improvements.

• Tests were done during January 2016, Oct 2016 and Jan-Feb 2017 which have shown conformance to the specifications provided to us.

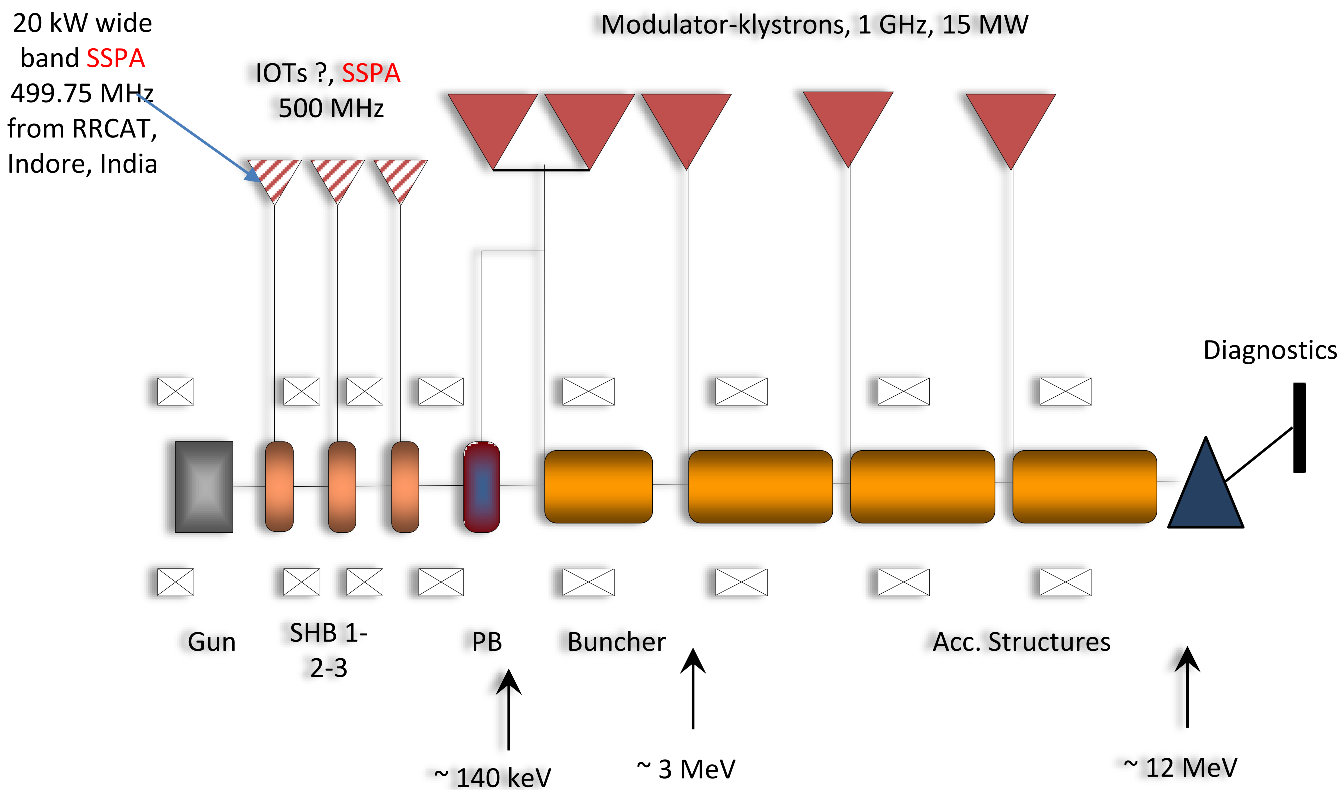
•Additional efforts on the 180 deg phase switching tests were also done successfully.

•Further investigations are in progress at CERN site.

Outline

- Technical Specifications of the 20kW SSPA
- 20kW SSPA architecture
- Final amplifier development and qualifications tests.
- Performance Test results done at CERN
- Conclusion

CLIC DB front end



For time being only major component development:
GUN, SHB, high bandwidth 500 MHz source, 1 GHZ MBK, modulator and accelerating structure in an high power test stand

Courtesy: Steffen Doebert

Sub-harmonic bunching system

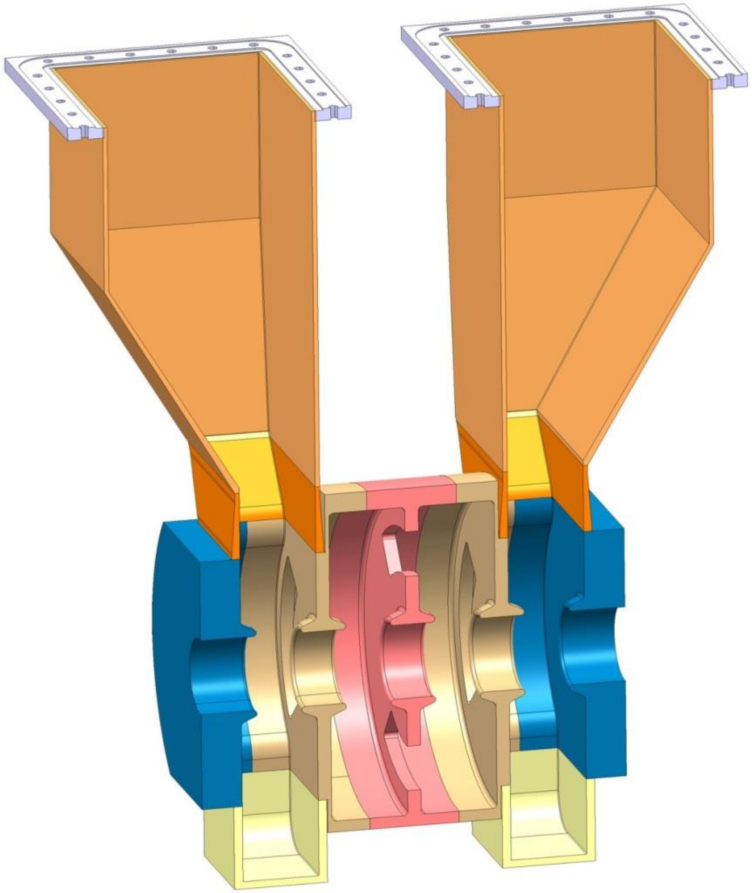
Power source:

500 MHz, 20-115 kW, wide band (60 MHz) sources needed for fast phase switching.

Solid state favored

Comment: On 20kW prototype Done under collaboration with RRCAT

	SHB 1	SHB 2	SHB 3
Beam velocity	0.62 c	0.62 c	0.62 c
Current	5 A	5 A	5 A
Voltage	15 kV	30 kV	45 kV
Bunch form factor	0.058	0.57	0.73
Detuning	1.6 MHz	12.1 MHz	12.7 MHz



Hamed Shaker

Courtesy: Steffen Doebert

Amplifier Final Specifications

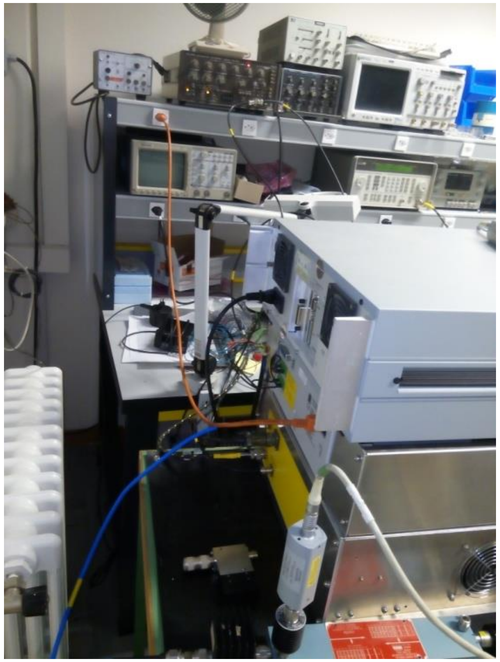
S.No.	Parameter	Value
01	Peak Power @499.75MHz	>73.1dBm
02	Gain @ Peak Power at 499.75 MHz	59dB
03	3dB bandwidth @ 14dBm I/P power	469.75MHz-529.75MHz
04	Pulse width	140.3µs
05	PRR	Up to 50 Hz
06	RF connectors	N-type (Input) DIN 7/16 (Output)
07	Pulse to pulse variation in amplitude	< 0.1dB
08	Pulse to pulse variation in phase	<+/-1°
09	In Pulse amplitude variation @ 499.75 MHz	~0.2dB
10	In Pulse Phase Variation @499.75 MHz	~4°
11	Dimensions	800mm (width)x 1000mm (depth) x 2000mm (height)

Salient Features of 20kW SSPA

Recap

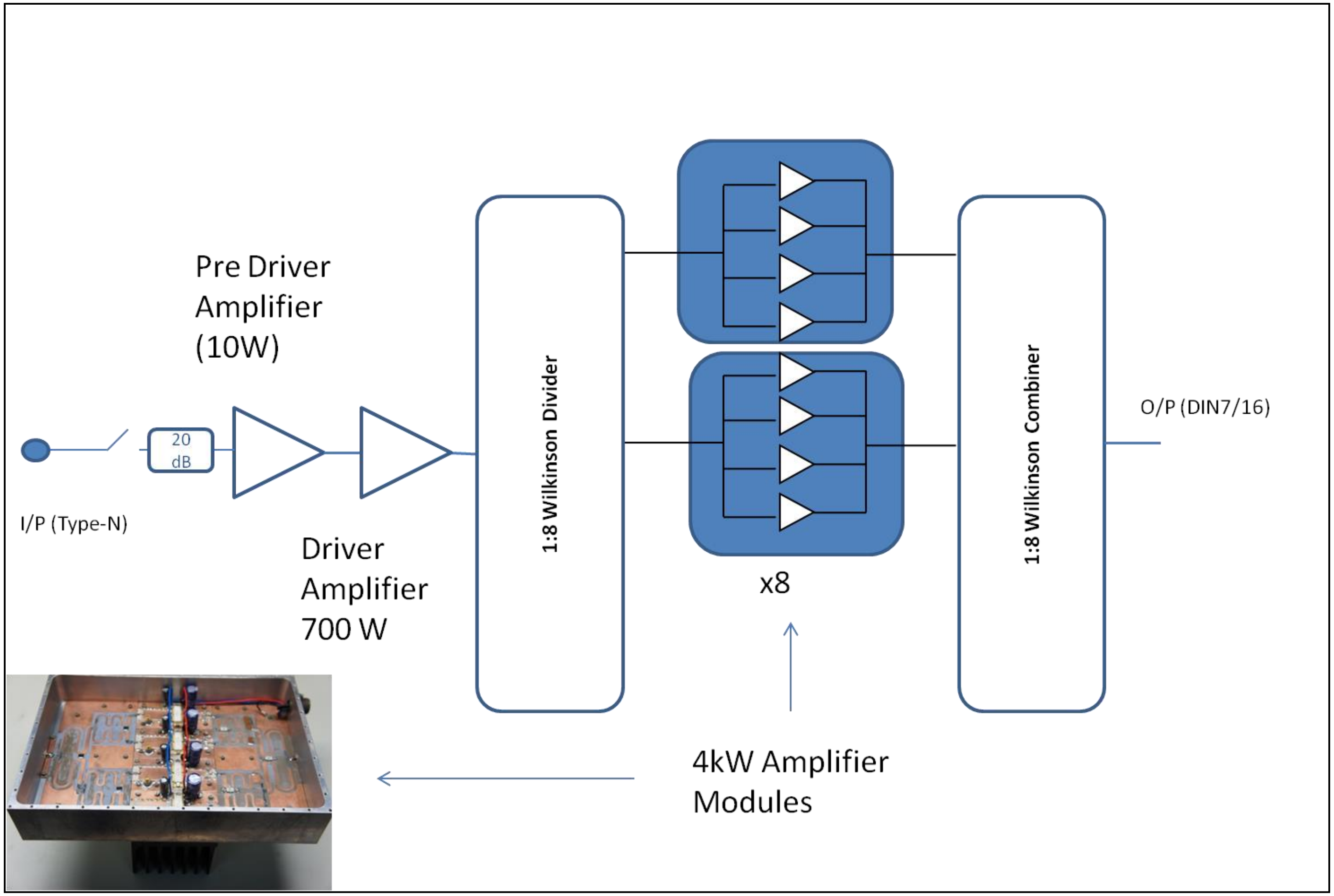
- Developed using high power push-pull LDMOS transistors
- The push-pull devices are operated under single ended configuration to reduce space and improve repeatability.
- The 20 kW is achieved by combination of 32 transistors.
- The high power combination is achieved using microstrip line planar combiner (Wilkinson Type).
- Design is highly modular, and size of each amplifier pallet (one transistor based amplifier), is 5cmx10cm only. A single pallet can provide upto 1400W peak power.

5kW Wideband SSPA Delivery to CERN from RRCAT



5kW prototype SSPA received at CERN undergoing tests during August 2015

Amplifier design



The amplifier is developed using eight amplifier modules capable of providing up to 4 kW of pulse power, which are combined by planar Wilkinson combiner and divider to generate 20 kW of pulsed output.

Description of stages of amplifier (CLIC WS 2016)

The amplifier has been developed as a three stage amplifier which consists of the following stages.

1 W Pre-driver amplifier
100 W GaN HEMT based driver amplifier
4kW High Power stage which is developed by combining 4 LDMOS transistors using Wilkinson combiner and divider networks on low loss flexible PTFE based laminates.
8 units of 4kW modules combined to provide over 20kW output.

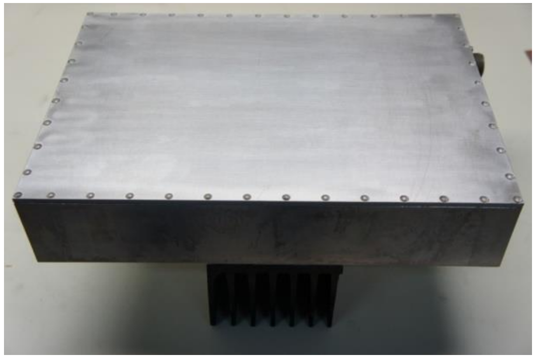
The switching ON time is defined by a RF switch which is having a controlled mono-shot circuit which sends TTL signal to switch for 150μs at rising edge of the input trigger (delay in RF ON ~200ns)

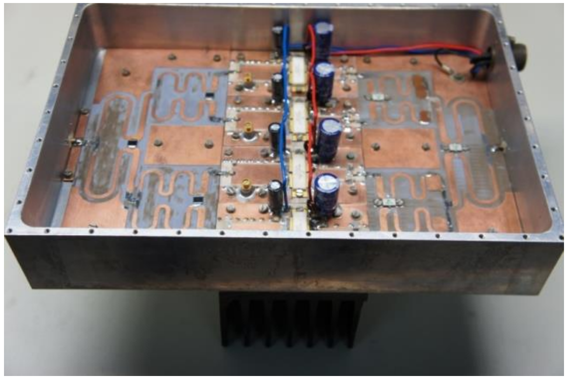
The three stages of the amplifier uses the following power supplies

1. 1W Pre-driver amplifier 24V, 600mA
2. Driver Amplifier 32V, 200mA for drain and -3.15V for Bias
3. High power stage 55V, 2A for drain and 2.15V for Bias

Input trigger signal 2.5V-5 V, 2 μs
(high Impedance)

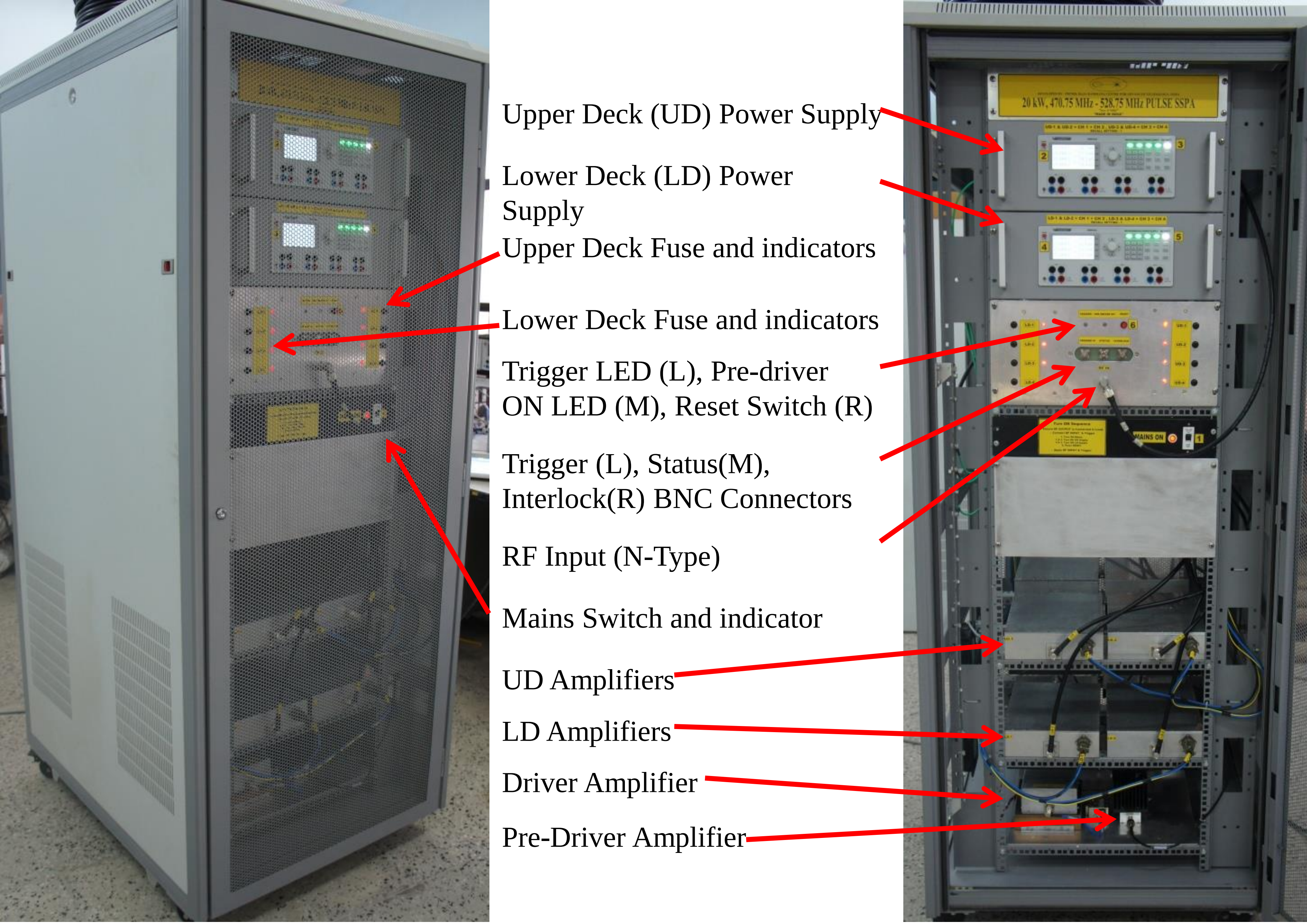
4kW module with 8:1 micro-strip power combiner





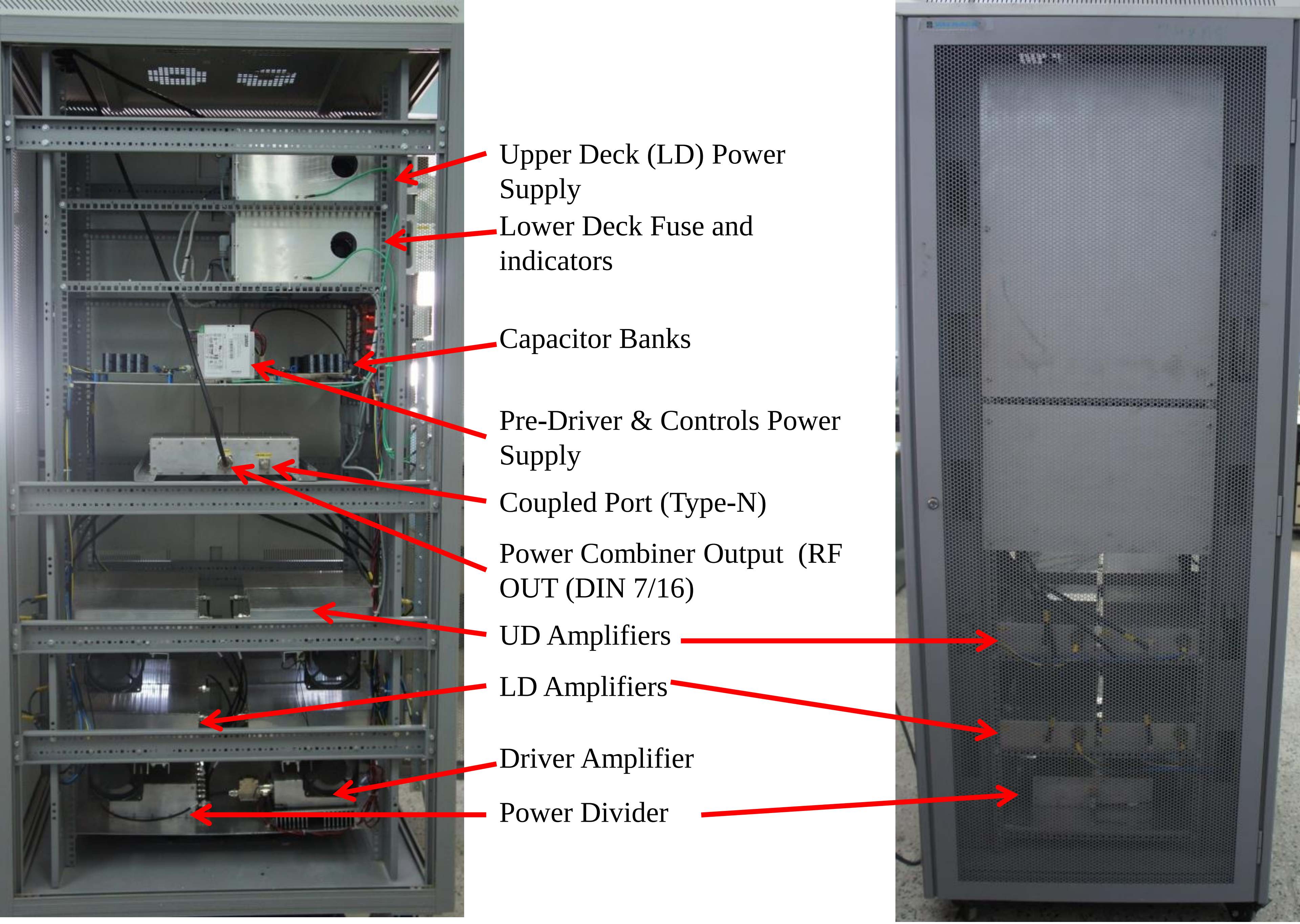
4kW amplifier modules

High Power Microwave combiner (microstrip line based) 8:1



Amplifier with door closed

Front View Door Open



Side View Panel Removed

Back View Door Closed

Details of the Front Panel Controls

2.4 Amplifier I/O connectors, interlocks and indicator description

Figure 2.4.1 The amplifier controls, interlocks and indicators are present on the front panel

The I/O connectors, interlocks and indicator are mounted on the front panel (see figure 2.4.1) are detailed below.

RF IN

Connector Type-N (F), maximum Input 14 dBm (CW or pulse).

TRIGGER IN

Connector BNC (F), this input accepts a TTL compatible signal, which controls the RF switch, TTL high – ON, TTL low – OFF.

Special Note 1:
Pre-driver is connected to RF2 port of the SPDT RF switch; in case pulse width modulation using this switch is not required. The pre driver can be connected to RF1 port of the RF switch and the front BNC should be terminated by a 50 Ohm termination (as shown in figure above). This will make RF switch always ON and in this case input RF should be pulse modulated. For details RF switch operation refer to its datasheet attached.

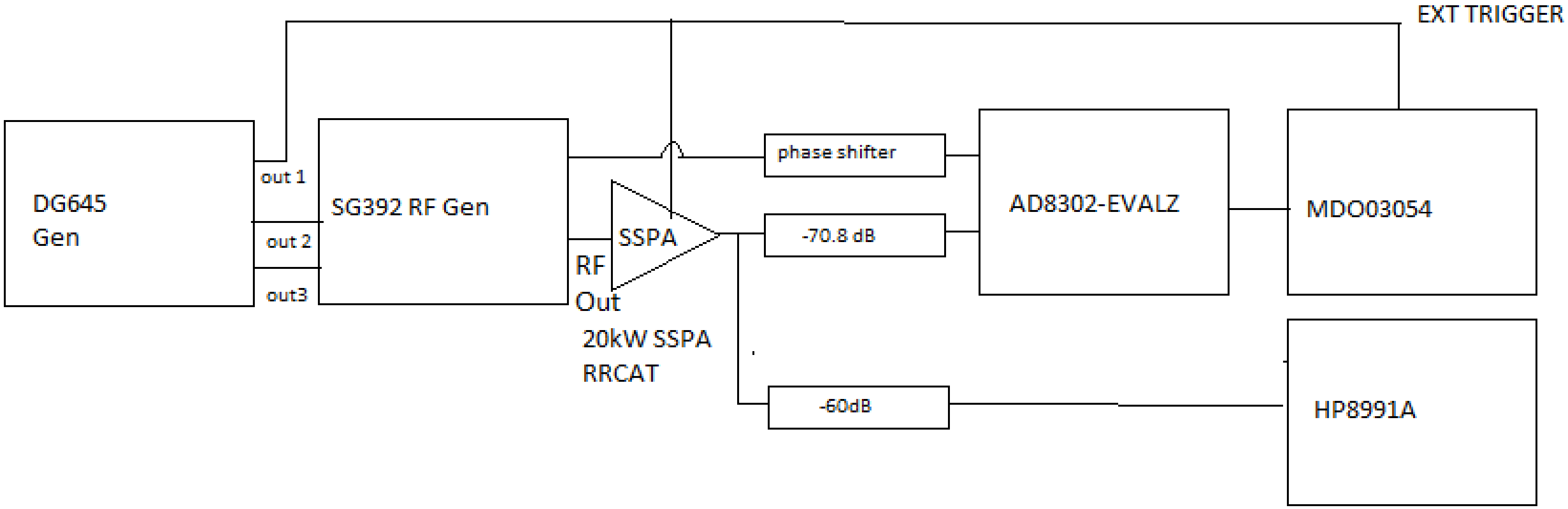
Drafted by PHPM Division, RRCAT | 8

Figure 2.6.1 The turn on sequence is mentioned on the front panel of the amplifier. The Turn ON and Turn OFF sequence are detailed on next page.

Performance tests on 20kW SSPA done at CERN

RRCAT-CERN Test Reports

Test set up at CERN for testing the RRCAT 20kW SSPA



2 Gain measurements

To measure the gain and frequency response, a cw RF signal was created by the SG392 and fed into the SSPA, whose output was read out with the HP8991A peak power analyser.
Test conditions: 50 Hz repetition rate, 140.3 μs pulse width, 14 dBm input.

Input Power	Meas Output	Coupling factor	Output Power
6	-12.5	70.8	58.3
7	-8.75	70.8	62.05
8	-5.87	70.8	64.93
9	-3.77	70.8	67.03
10	-1.67	70.8	69.13
11	0.14	70.8	70.94
12	1.47	70.8	72.27
13	2	70.8	72.8
14	2.33	70.8	73.13

Table 1: Gain response @499.75MHz

RF frequency	Meas Output	Coupling factor	Output Power
469.75	0.03	70	70.03
474.75	0.7	70.2	70.09
479.75	0.98	70.4	71.38
484.75	1.17	70.55	71.72
489.75	1.42	70.7	72.12
494.75	1.87	70.75	72.62
499.75	2.37	70.8	73.17
504.75	2.58	70.9	73.48
509.75	2.14	71	73.14
514.75	1.26	70.8	72.06
519.75	0.51	70.6	71.11
524.75	1.14	69.5	70.64
529.75	8	61	69

Table 2: Frequency response at 14dBm

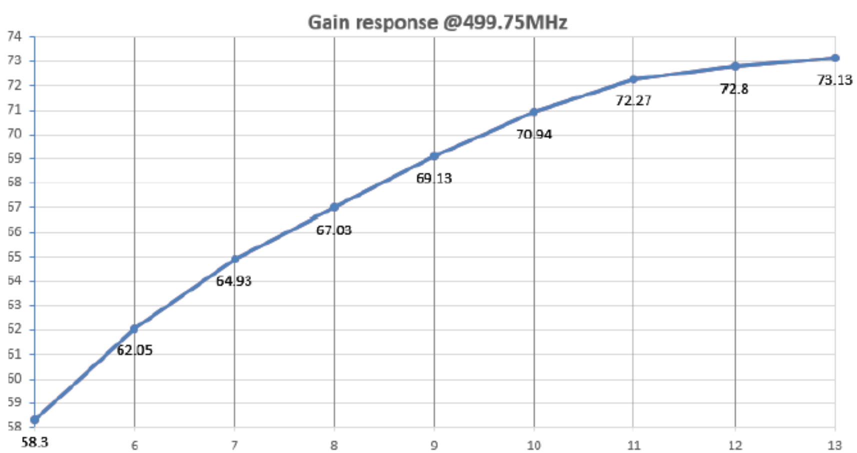


Figure 2: Gain response at 499.75MHz

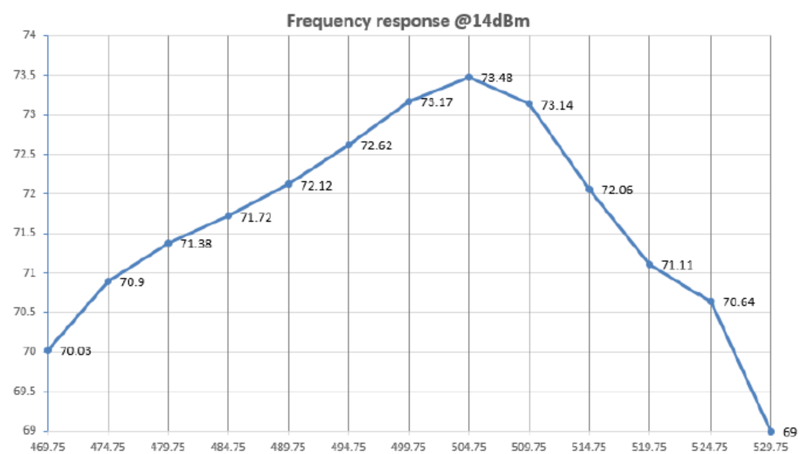
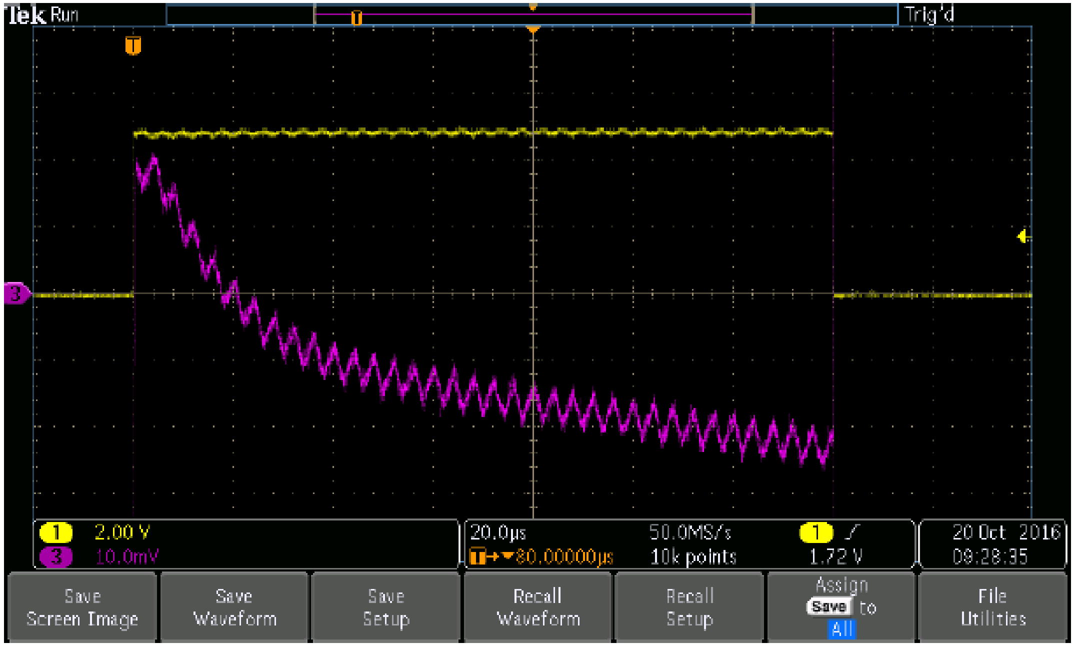


Figure 3: Frequency response at 14dBm

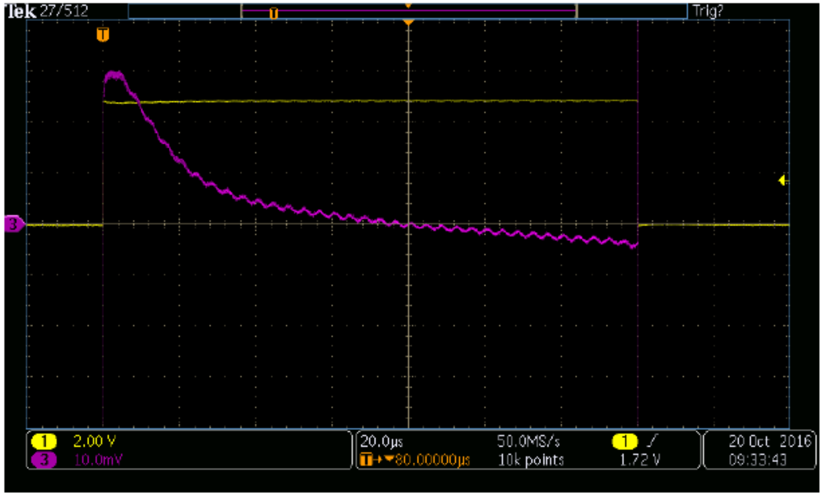
Phase measurements

Objective here was to measure the phase stability for different input powers. There a CW RF signal was created by SG392 signal generator and fed to SSPA, whose output was read with the AD8302-EVALZ. The following traces show the trigger signal (CH1) and the phase response as output from the AD8302 (CH3).

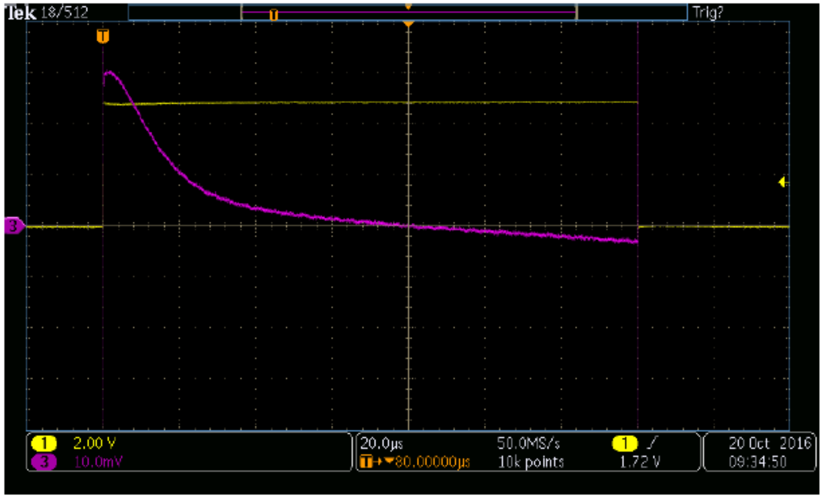
Test conditions: Pulse width 140 microsecs, PRR 50Hz, 10mV/deg phase card response.



Phase response at 13dBm input power. With the AD8302-EVALZ with resolution of 10mV/dg, the phase variation is 4 deg.



Phase response at 11dBm input power. With the AD8302-EVALZ with resolution of 10mV/dg, the phase variation is 3.3 deg.



Phase response at 9 dBm input power. With the AD8302-EVALZ with resolution of 10mV/dg, the phase variation is 3.3 deg.

4 180° phase shift

The aim was to investigate the phase and amplitude behavior and stability of the amplifier in case of a 180° phase shift in the middle of the RF pulse.
Figure 9 shows the trigger and IQ control signals for the 180° phase shift. These are provided by the DG645.

Test conditions: 50 Hz repetition rate, 140.3 µs pulse width, 70.15 µs IQ-modulation pulse width, ±0.5 V IQ-modulation voltage level, 10 mV/deg phase card response and 29 mV/dB gain card response.

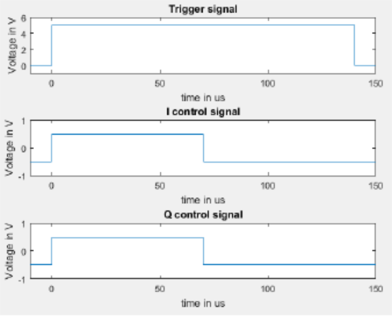


Figure 9: Trigger and IQ control signals

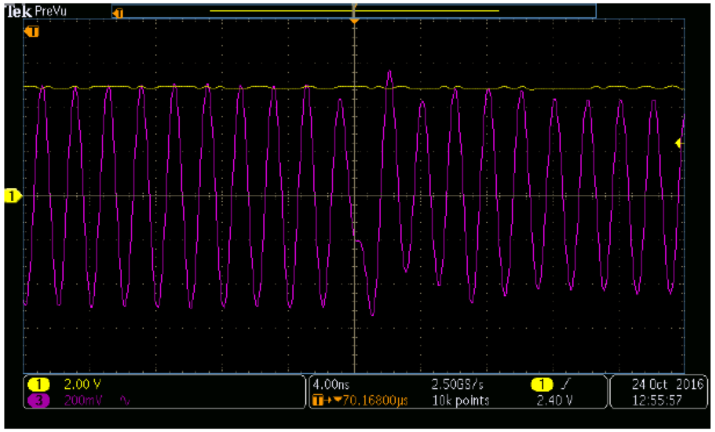


Figure 10: Phase shift of the SG392 RF output directly connected to the oscilloscope at 499.75 MHz and 7 dBm input power at the amplifier. It gets visible that the phase does a 180° shift, transmission time is 8 ns.

Figure 11: Phase shift of the SSAP output signal, 70.8 dB attenuated at 499.75 MHz and 7 dBm input power at the amplifier. Gradual phase shift process gets visible, transmission time 8 ns. The phase shift causes amplitude variations of around -40%/-4 dB.

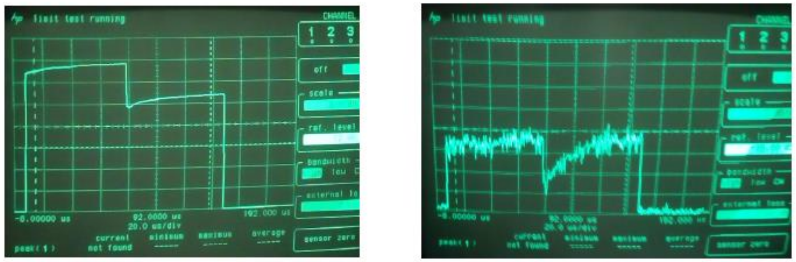
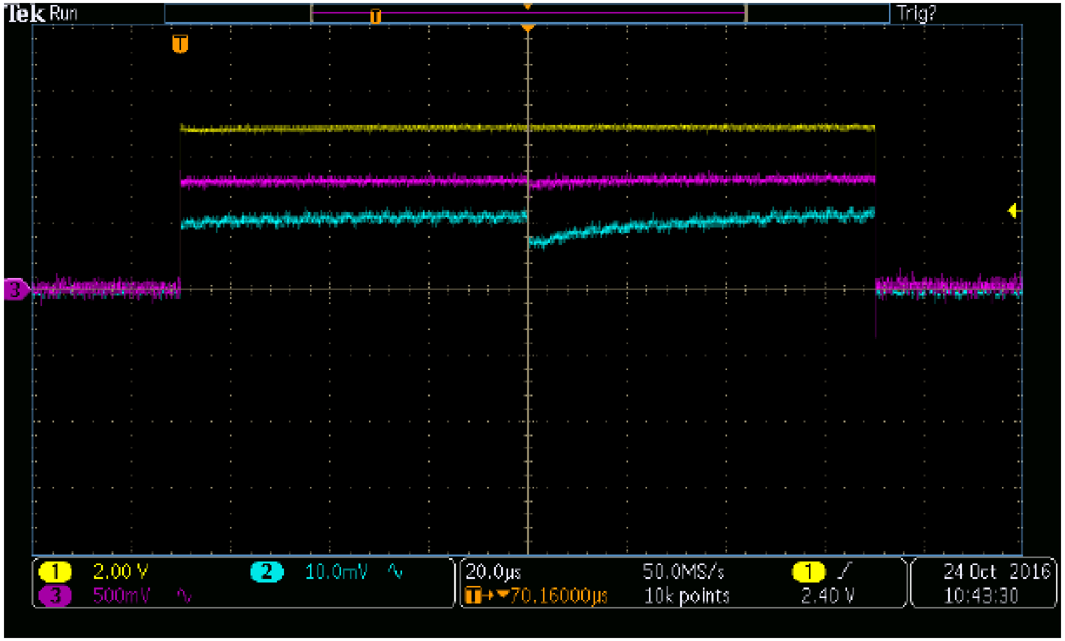
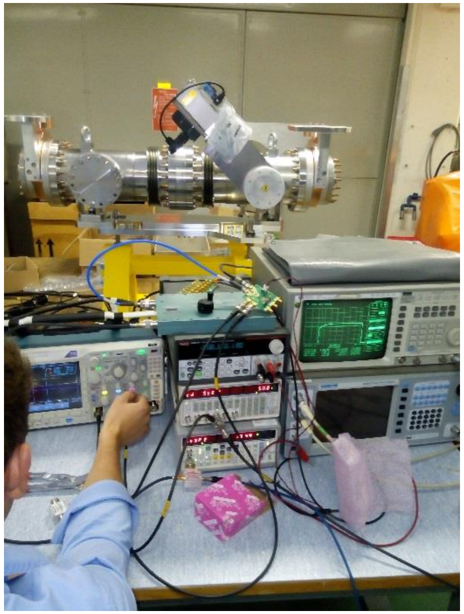


Figure 12: Gain output of the SSPA 60 dB attenuated, with control signals from fig. 9 on the left and adapted phase shift IQ control signals (±0.35 V) on the right. Control signals were adapted so the gain for the time before and after the phase shift is on the same level and so the gain for the modulated and unmodulated (cw) mode of the SG392 is on the same level. The strong noise is caused by different resolutions, 2 dBm/div on the left and 1 dBm/div on the right



Trigger signal (CH1), gain (CH2) and phase response (CH3) of the AD8302-EVALZ card to 180 deg phase shift in the middle of the trigger pulse at 499.75 MHz and 7dBm input power at the SSPA, 10mV/deg phase phase card response and 29mV/dB gain card response.



Tests repeated during Jan Feb 2017 at CERN

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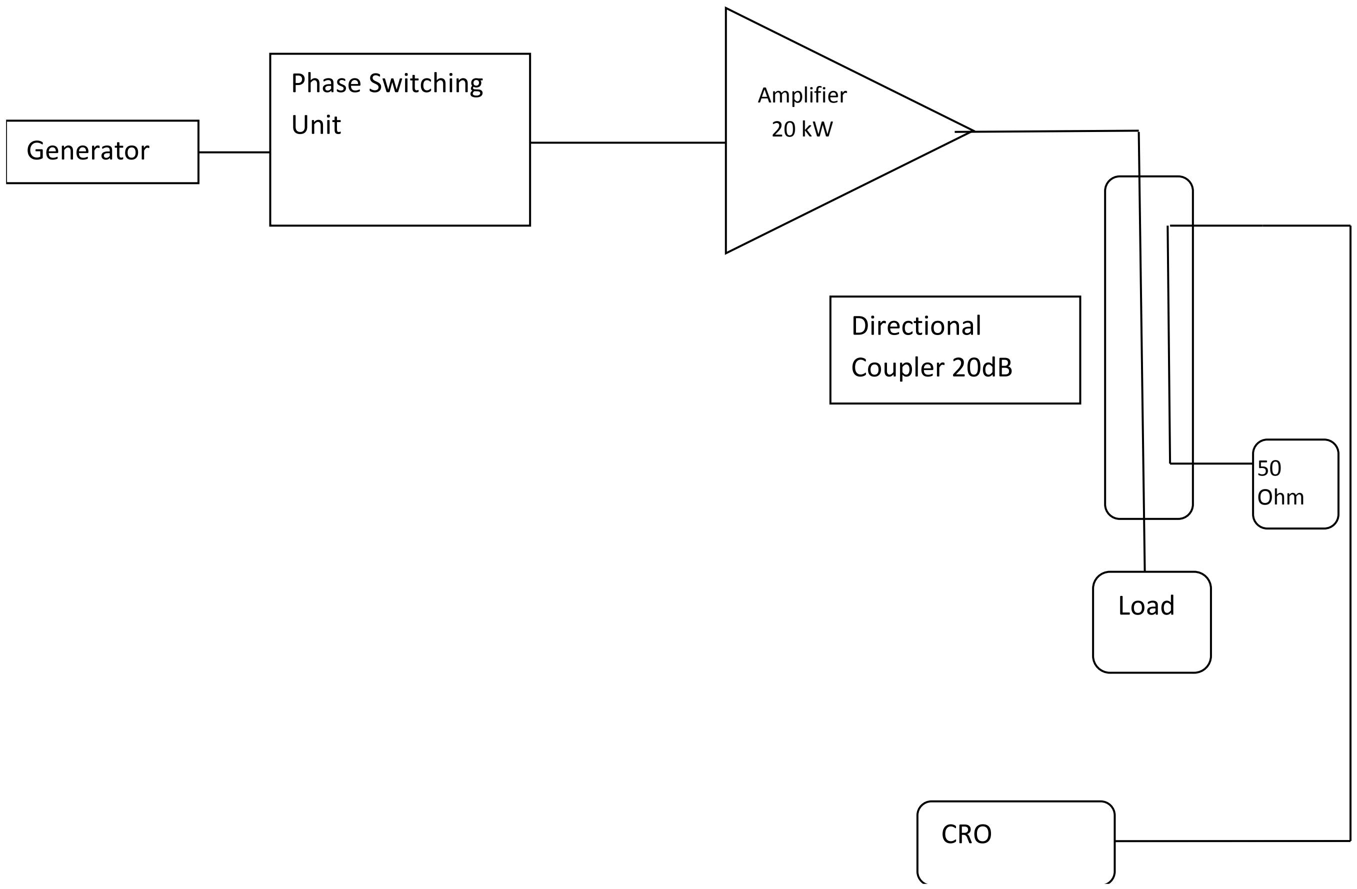
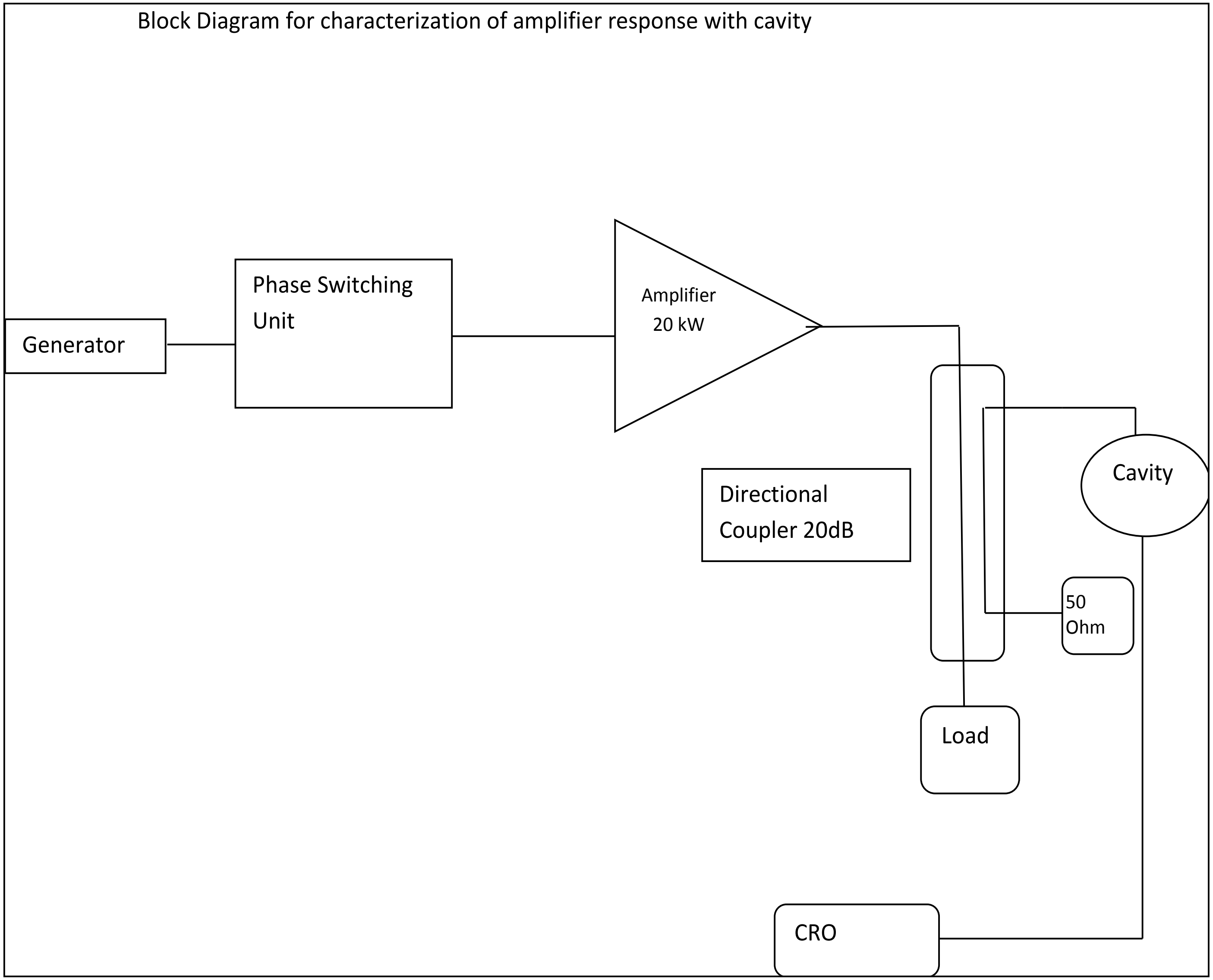
Block Diagram for characterization of amplifier response to phase switched input




Block Diagram for characterization of amplifier response with cavity
Generator
Phase Switching
Unit
Amplifier
20 kW
Directional
Coupler 20dB
Cavity
50
Ohm
Load
CRO

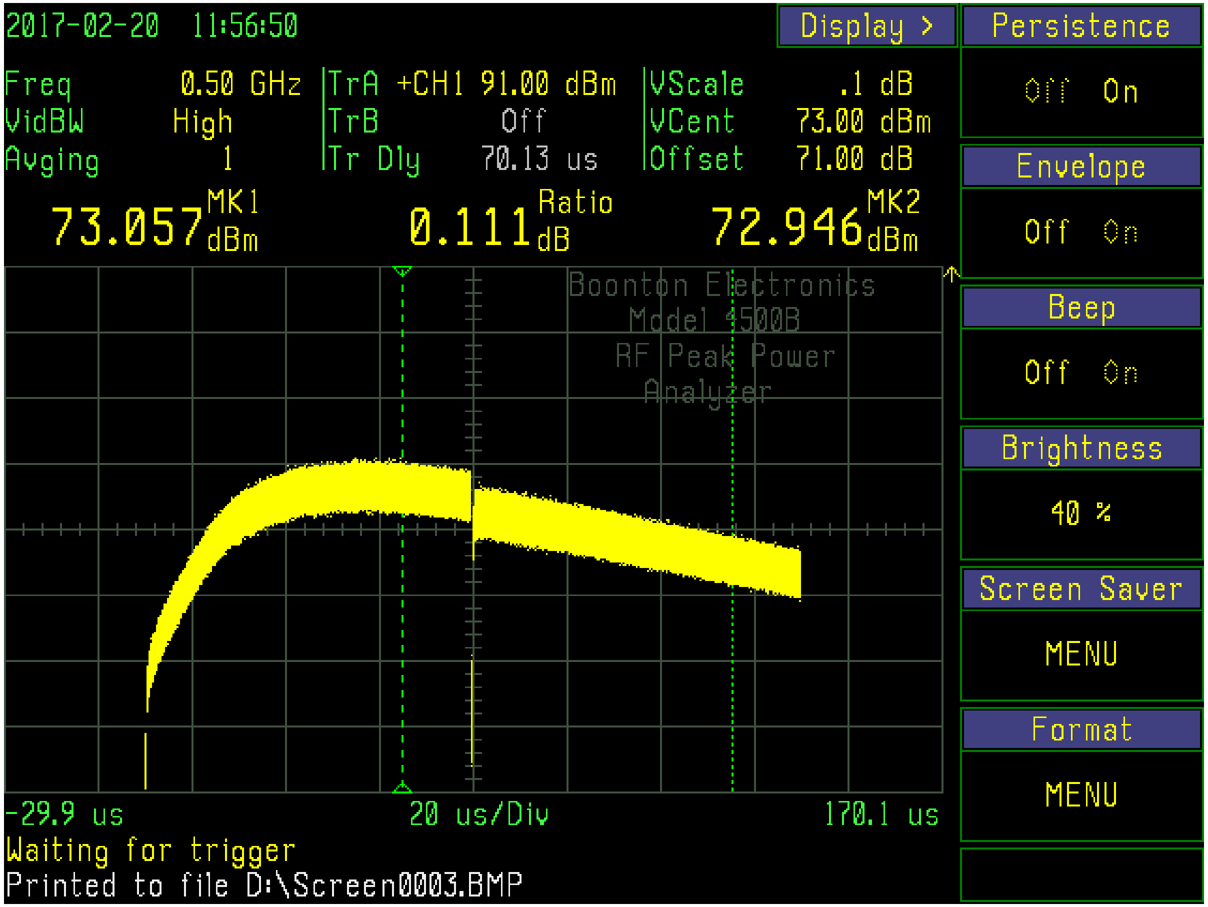


Fig.1. Amplifier temporal stability over 9000 samples (30 min run time) as measured on peak power analyzer kept on persistence mode. Stability is around +/- 0.05dB.

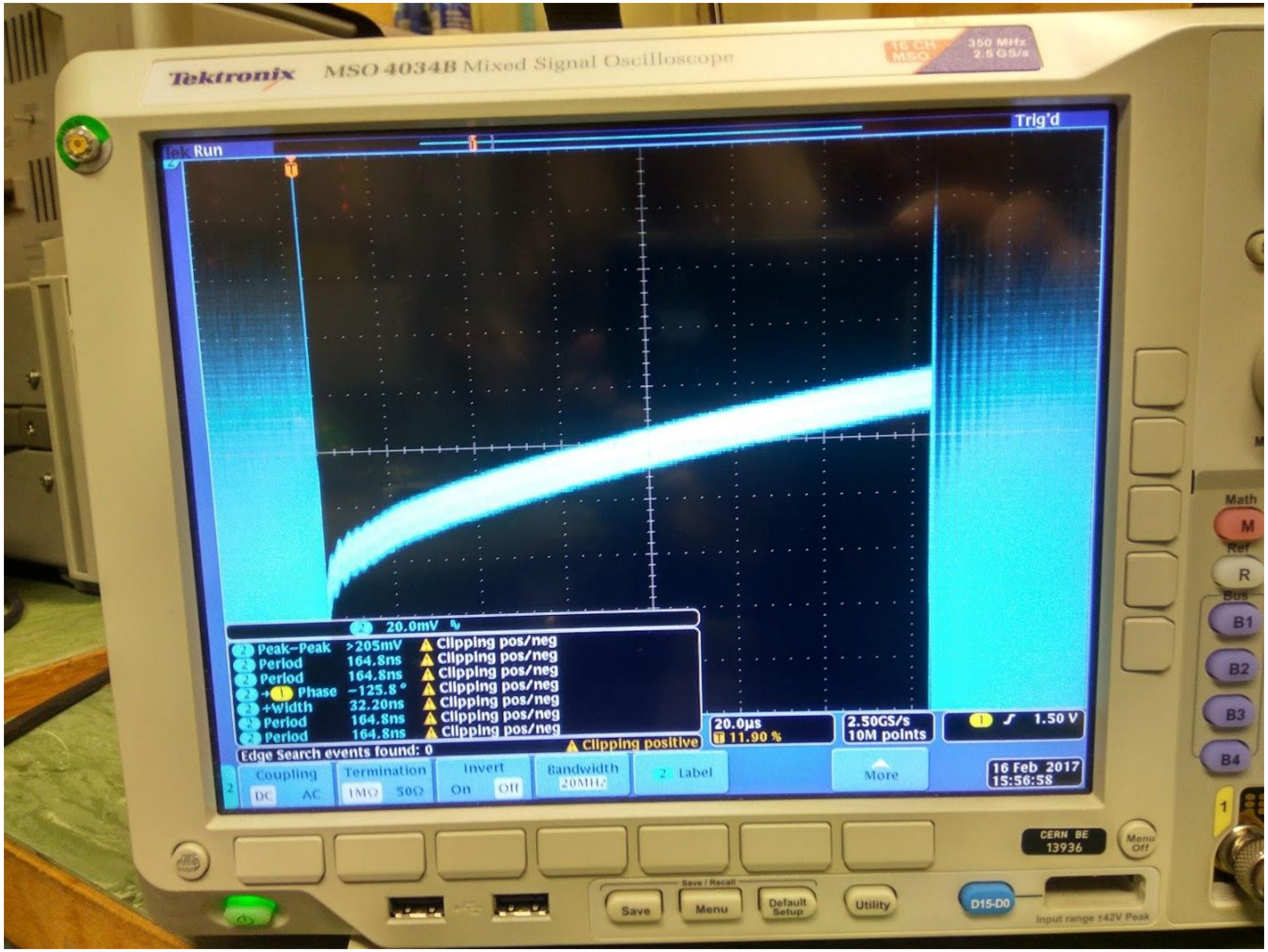
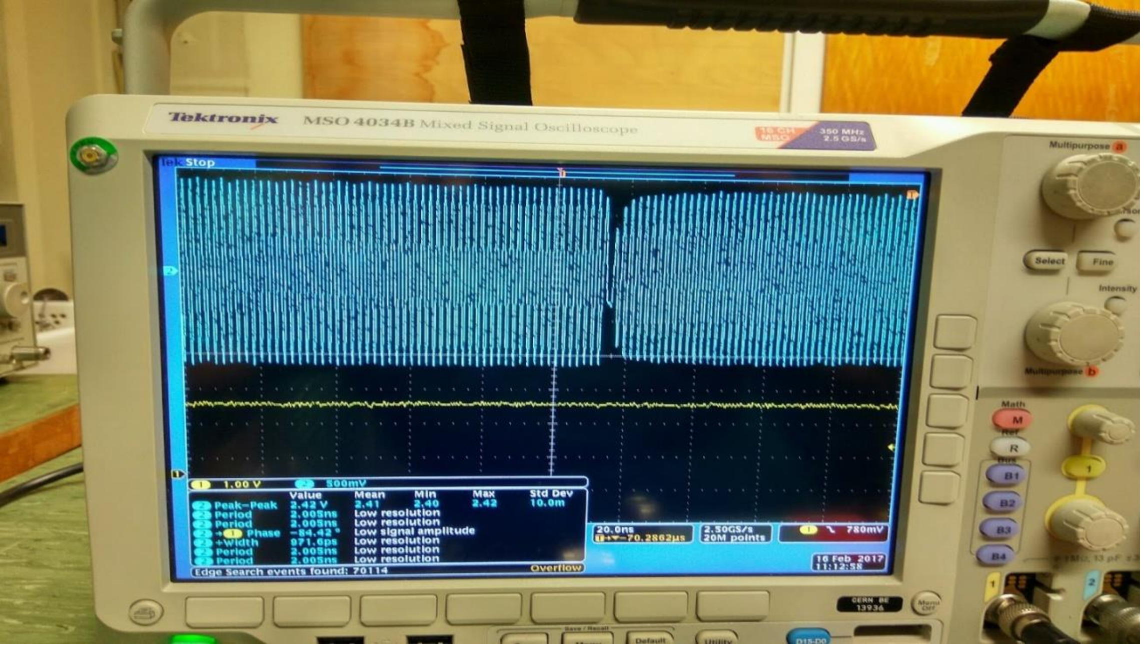


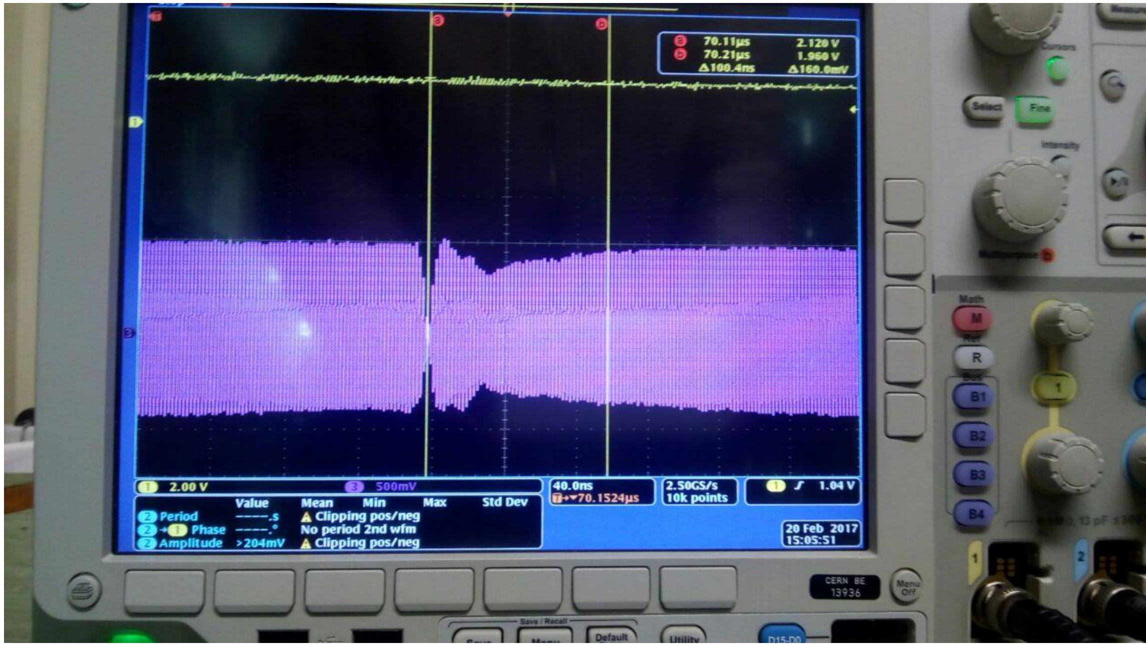
Fig.6. Amplifier phase stability over 1500 samples (5 min run time) as measured on a Tektronix MSO kept on persistence mode. The CRO scale is 20mV/division corresponding to 2 deg/div. The stability is found to be within +/- 1degree.

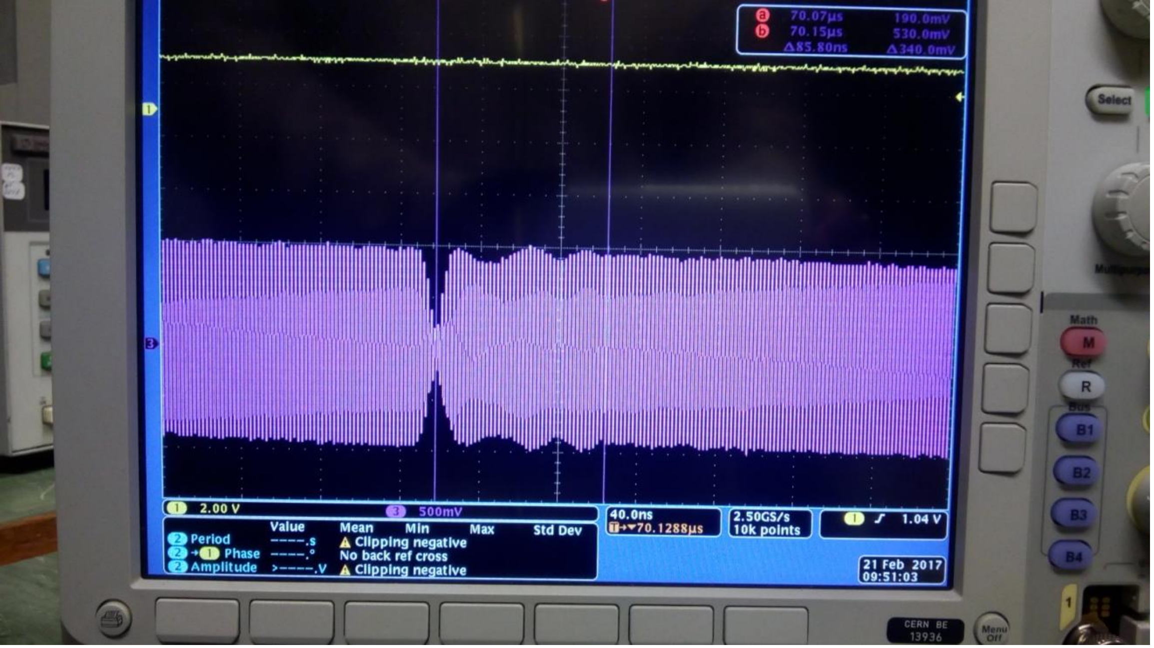


Phase switched Input signal as seen on a CRO. Time scale is 20ns/Div. The 180 degree phase switching is obtained by using a switch and two different paths.

Amplifier response during phase switching

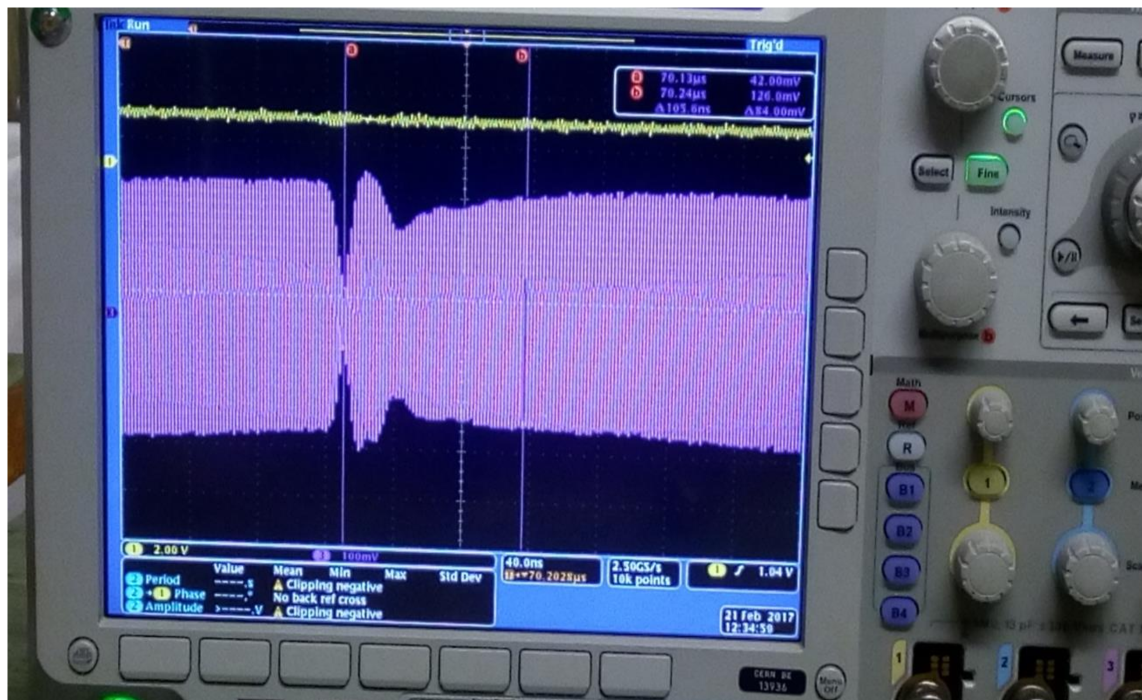
Output power as seen on CRO time scale 40ns/div. Amplifier output stabilizes after ~ 100ns





Response of cavity to phase switched input without any amplifier as seen on CRO time scale 40ns/div output stabilizes after ~ 100ns

Response of cavity to phase switched amplifier output as seen on CRO time scale 40ns/div output stabilizes after ~ 100ns



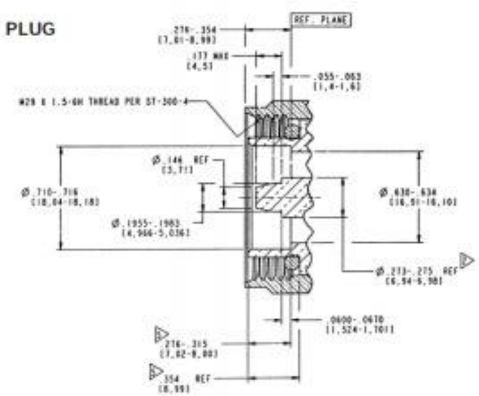
Conclusion:

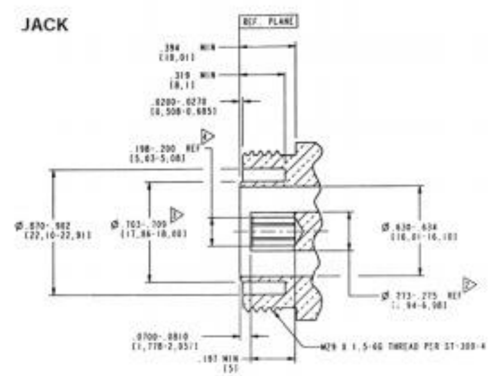
- A Prototype 20kW wide band SSPA has been designed, developed and subjected to long duration endurance testing at RRCAT, Indore, India
- Amplifier power reaches thermal equilibrium after 30 minutes and has excellent phase and amplitude stability meeting specifications.
- The desired specifications have been achieved and scope for further improvements/upgrades depending upon application to the harmonic buncher shall continue.
- 20kW SSPA system has been delivered to CERN. Some mechanical damages to the supports   was encountered during shipment. Nothing serious damage to electronics. It was repaired during Jan-Feb 2016 and amplifier was tested for full functioning. The mechanical harnessing was redone at CERN and amplifier was tested again for rated specifications during Oct 2017.
- The amplifier is stable in both phase and amplitude. Amplifier performance at CERN in conformance with that done at RRCAT.
- Tests reveal 8ns switching time for 180 deg phase switching. The response of amplifier and of cavity to phase switching needs to be further investigated and attempts needs to be done to have a faster and smoother recovery of signal after phase switching. .

THANK YOU

7/16 DIN (Deutsches Institut für Normung) output connector of SSPA

Electrical	
Impedance	50 Ohm
Frequency Range	7.0 GHz max
Voltage Rating	2.7 kv RMS
Dielectric Withstanding Voltage	4 kv RMS
VSWR	1.3 max, 0-7.0 GHz
Insulation Resistance	5000 MΩ
Environmental	
Temperature Range	-40°C to +150°C
Thermal Shock	Pass (IEC 68, part 2-14, test Na)
Corrosion	Pass (IEC 68, part 2-1, test Ka)
Vibration	Pass (IEC 68, part 2-6)



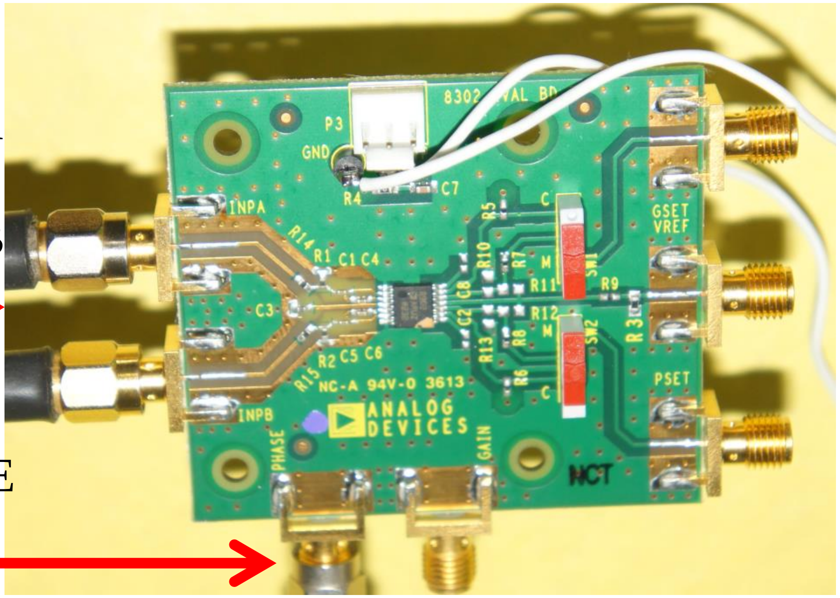


Phase card description

Analog devices make phase card (AD 8302 Eval Board) was used as phase detector for testing of the amplifier. The board recieves two inputs (INPA, INPB) and produces difference in phase of the inputs at the sma connector (PHASE), the sensitivity of the output is 10mV/degree.

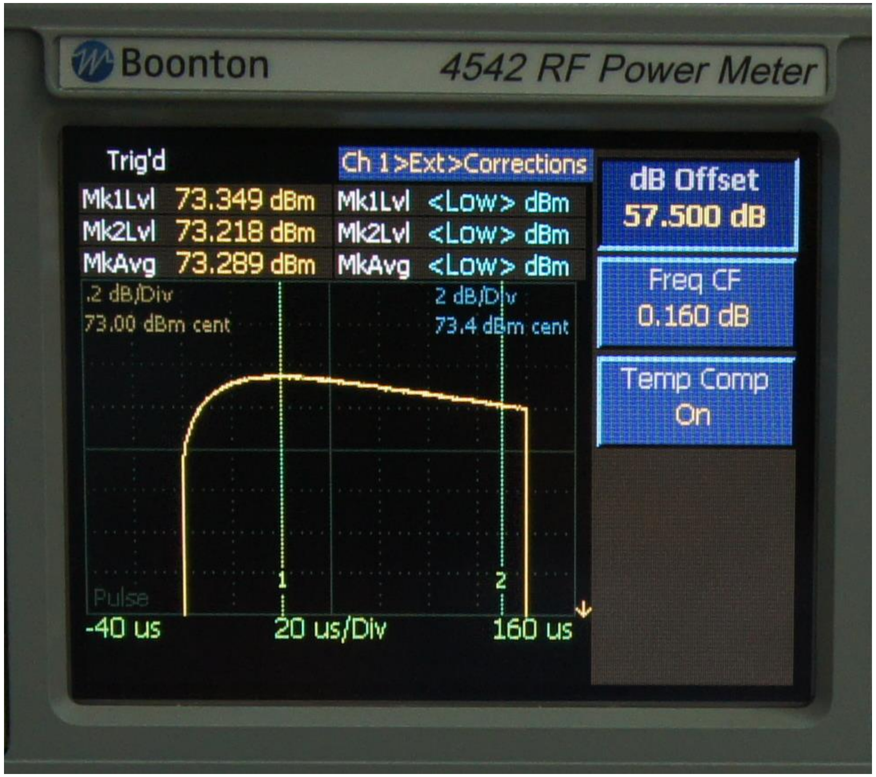
Note : without input the phase output will show a dc voltage of ~1.25V.
The card operates with +5V d.c. supply

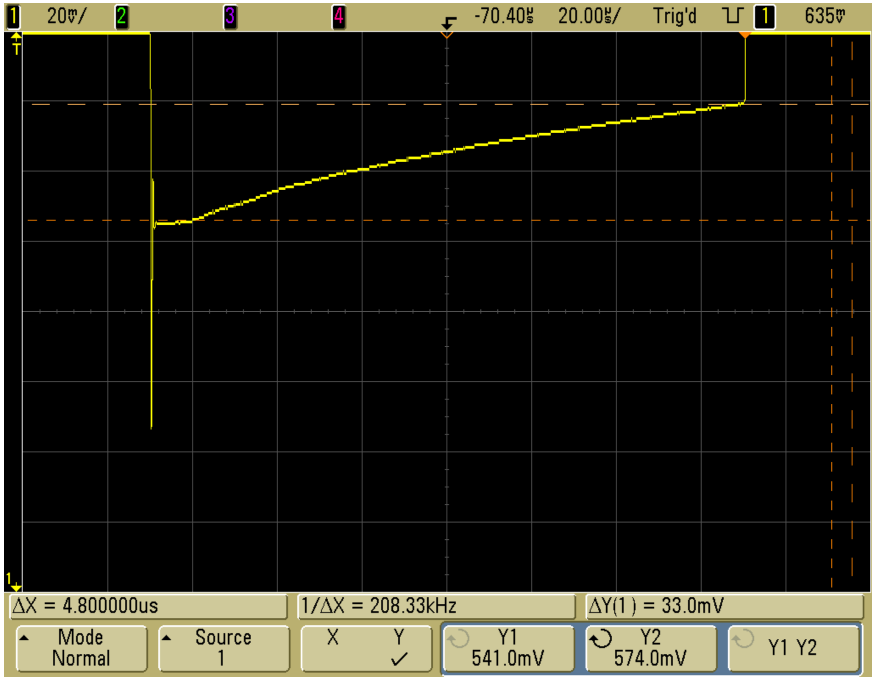
INPA
&
INPB



PHASE
O/P

AD 8302 Evaluation Board





Phase and amplitude response at Frequency 499.75 MHz, the above picture is the output of the phase card which shows the variation of the output power phase with respect to input during pulse. The lower image is of detected power at peak power analyzer. The phase card response is 10mV/degree. The two markers are set at 40 µs and 130 µs in the lower image. The phase variation in pulse is 3.3 degree and amplitude variation ~0.2dB.