



Development of Inductive Adders for CLIC DR Kickers – Status Update

J. Holma

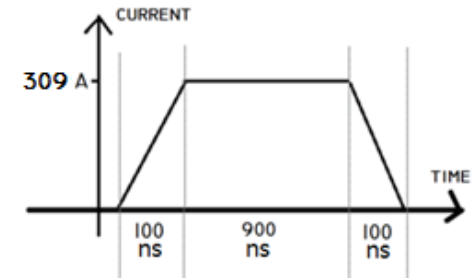
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Acknowledgement M.J. Barnes
CERN

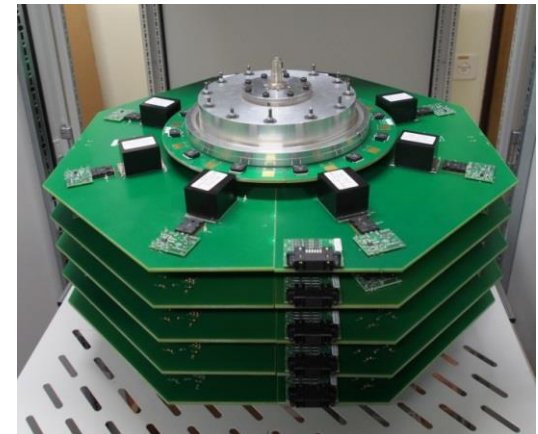
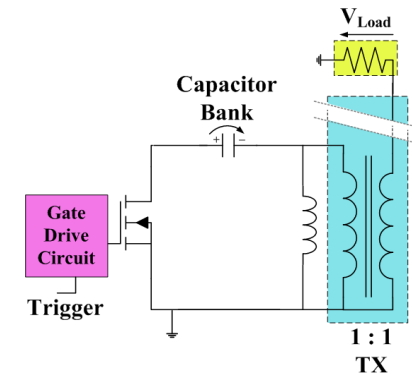


Outline

- **Background and Motivation**
 - Specifications for CLIC DR Extraction Kicker System
- **Inductive Adder Design**
 - Schematic and Features
 - Methods to Improve the Pulse Flat-top Stability
- **5-layer "Full-scale" Prototype Inductive Adder**
 - Measurements with Active Compensation of Droop and Ripple
 - Measurements with Pulse Cancelling Method
 - Measurement with a Differential Amplifier Setup
- **12.5 kV, 20-layer, Prototype Inductive Adder**
 - Initial Measurements with 10-layers Powered.
 - Required Optimised Waveform for CLIC DR Kicker System.
- **Future Work**



Ideal stripline current for 1 GHz option

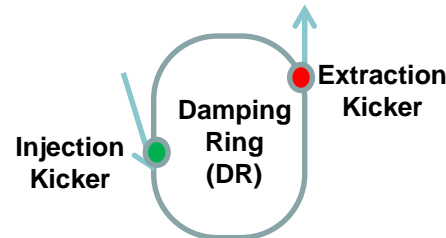




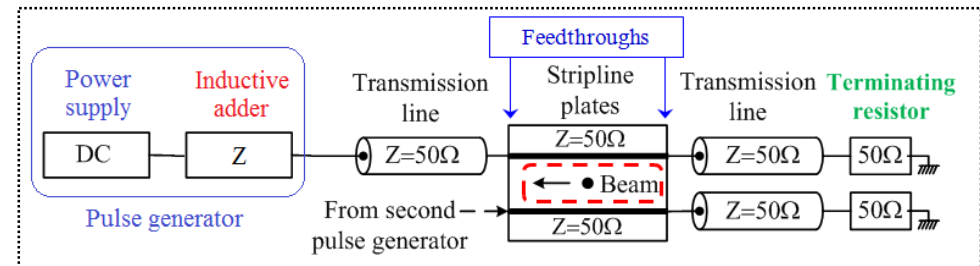
Specifications for the CLIC DR Extraction Kicker Systems

| | CLIC DR (1 GHz 2 GHz) |
|---|---|
| Pulse voltage (kV) (per Stripline) | ± 12.5 |
| Stripline pulse current [40.5 Ω load] (A) | ± 309 |
| Repetition rate (Hz) | 50 |
| Pulse flat-top duration (ns) *900 ns = 160 ns + 580 ns gap + 160 ns | ~160 ~900* |
| Flat-top repeatability | $\pm 1 \times 10^{-4}$ (± 0.01 %) |
| Flat-top stability [droop + ripple], (Inj.) per Kicker SYSTEM (Ext.) | $\pm 2 \times 10^{-3}$ (± 0.2 %) $\pm 2 \times 10^{-4}$ (± 0.02 %) |
| Field rise time (ns) | 1000 |
| Field fall time (ns) | 1000 |
| Beam energy (GeV) | 2.86 |
| Total kick deflection angle (mrad) | 1.5 (0.09 deg) |
| Aperture (mm) | 20 |
| Effective length (m) | 1.7 |
| Field inhomogeneity (%) [3.5 mm radius] [1 mm radius] | ± 0.1 (Inj.) ± 0.01 (Ext.) |

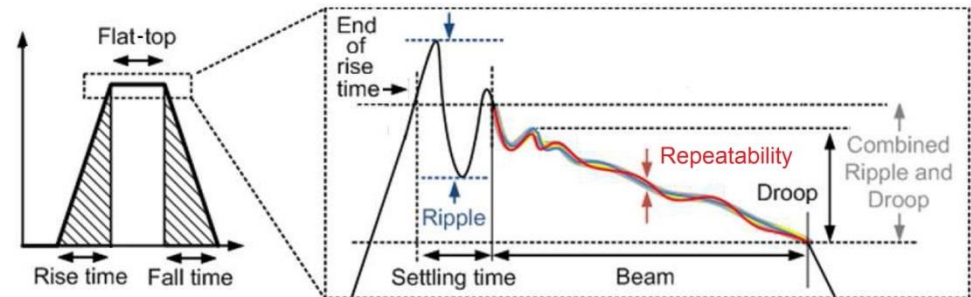
- **Extremely tight requirements for flat-top stability and repeatability!**
- **For rise/fall times, ≤ 100 ns desired.**



Damping ring kickers Prototype CLIC DR extraction kicker (Courtesy of C. Belver-Aguilar)



Simplified schematic of a kicker system

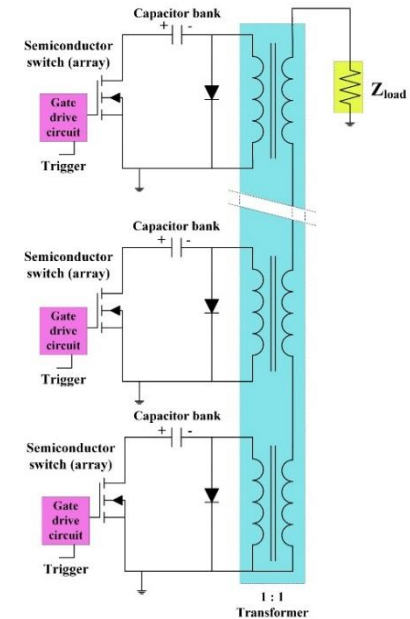


CLIC DR kicker pulse definition

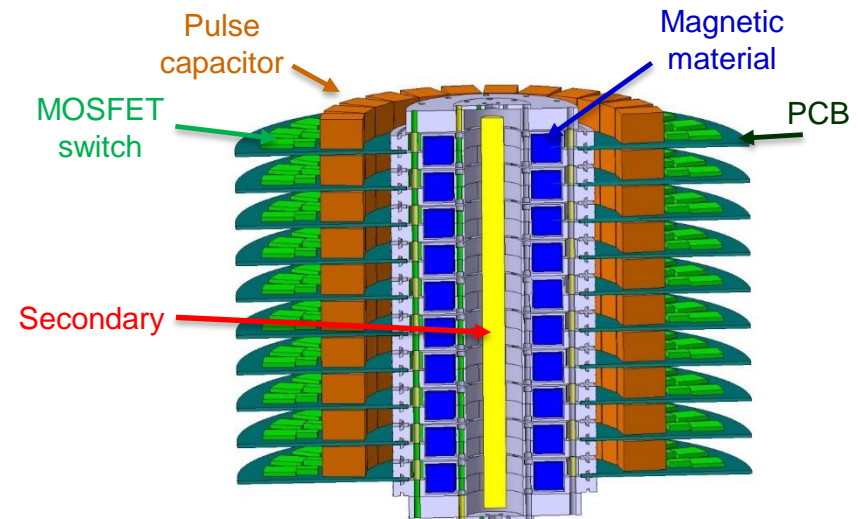


Inductive Adder

- Many primary “layers”, each with solid-state switches
- The output voltage is approximately the sum of the voltages of the primary constant voltage layers
- + Control electronics referenced to ground
- + No electronics referenced to high voltage despite the high voltage output of the adder
- + The output voltage can be modulated during the pulse with an analogue modulation layer
- + Modularity: the same design can potentially be used for kickers with different specifications (CLIC PDR & DR kicker modulators, extraction + dump kicker)
- + Redundancy and machine safety: if one switch or layer fails, the adder still gives full voltage or a significant portion of the required output pulse
- + Possibility to generate positive or negative output pulses with the same adder: the polarity of the pulse can be changed by grounding the other end of the output of the adder



Schematic of an inductive adder

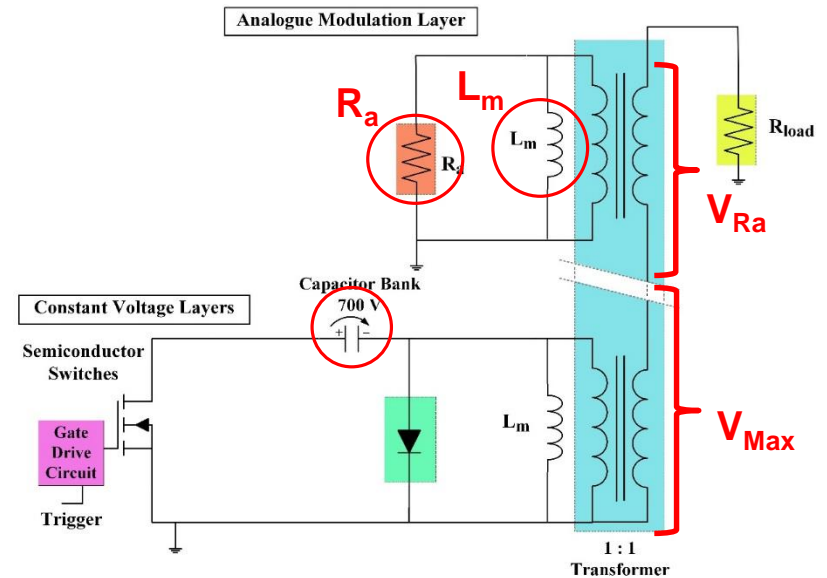
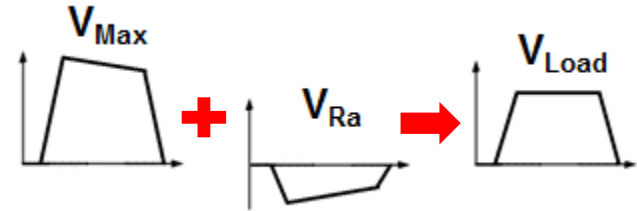


Cross-section of an inductive adder



Improving the Pulse Flat-top Stability: Passive and Active Modulation

- Droop and ripple of the output pulse of an inductive adder can be compensated with an analogue modulation layer
- In the analogue modulation layer, resistor R_a is effectively in series with the load
- The load voltage is the sum of the voltages across all of the layers.
- Two modes:
 - **Passive mode:** During the pulse, current through L_m increases, which causes current through R_a to decrease. Therefore, voltage over R_a decreases, which can compensate for a reduction (droop) in the primary voltage of the other layers.

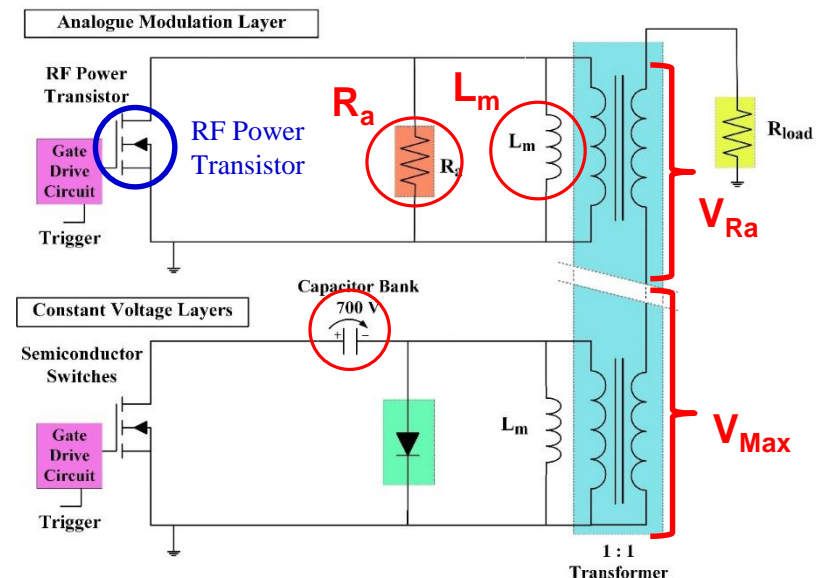
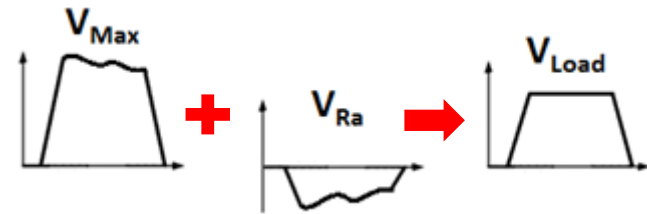


Passive analogue modulation



Improving the Pulse Flat-top Stability: Passive and Active Modulation

- Droop and ripple of the output pulse of an inductive adder can be compensated with an analogue modulation layer
- In the analogue modulation layer, resistor R_a is effectively in series with the load
- The load voltage is the sum of the voltages across all of the layers.
- Two modes:
 - **Passive mode:** During the pulse, current through L_m increases, which causes current through R_a to decrease. Therefore, voltage over R_a decreases, which can compensate for a reduction (droop) in the primary voltage of the other layers.
 - **Active mode:** A linear RF power transistor is connected in parallel with resistor R_a . The voltage across R_a can be controlled by modulating the current through the RF power transistor.



Active analogue modulation



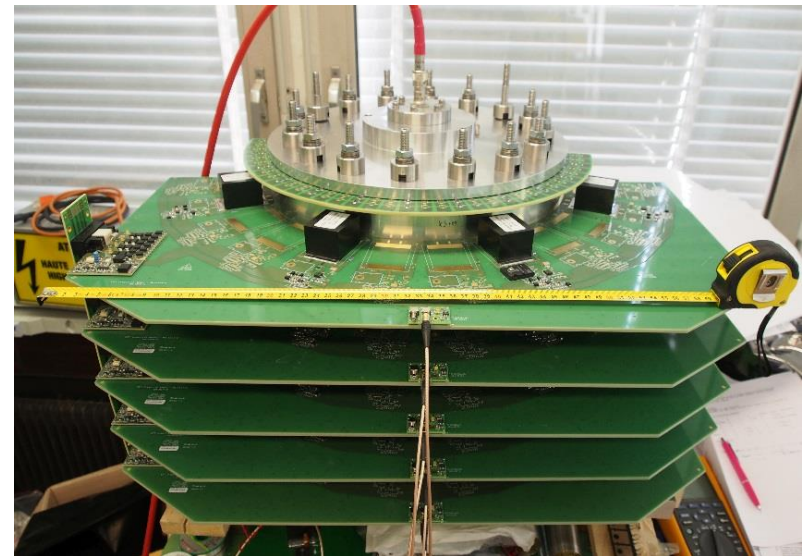
Prototype 3: the First 5 "Full-scale" Layers of the 12.5 kV, 20-layer, Inductive Adder

- 5-layers, otherwise identical design with 20-layer, 12.5 kV CLIC DR extraction kicker inductive adder.
- Specifications according to requirements for CLIC DR extraction kicker.
- Target flat-top stability ± 0.02 % for 900 ns, target flat-top repeatability ± 0.01 % for 900 ns.
- Status: Assembled and tested.

| Design Parameter | 5-Layer Full-Scale Prototype | CLIC DR Extraction Kicker Modulator |
|--------------------------------------|------------------------------|-------------------------------------|
| Output Voltage (kV) | 3.5 | 12.5 |
| Output Current | 308** | 250 |
| Voltage per layer | 700 | 700 |
| Number of layers | 5 | 20 |
| Pulse flat-top duration (ns) | 1100 | 160 – 900 |
| Pulse rise time [0.1-99.9 %] (ns) | 100 | < 1000 |
| Pulse fall time [0.1-99.9 %] (ns) | 100 | < 1000 |
| Flat-top stability (for 900* ns) | $\leq \pm 0.02$ % | ± 0.02 % |
| Flat-top repeatability (for 900* ns) | $\leq \pm 0.01$ % | ± 0.01 % |

*900 ns = 160 ns + 580 ns gap + 160 ns

**Stripline odd-mode impedance 40.5Ω



First 5 layers of the 12.5 kV inductive adder assembled at CERN



Measurements on Prototype 3: with Modulation

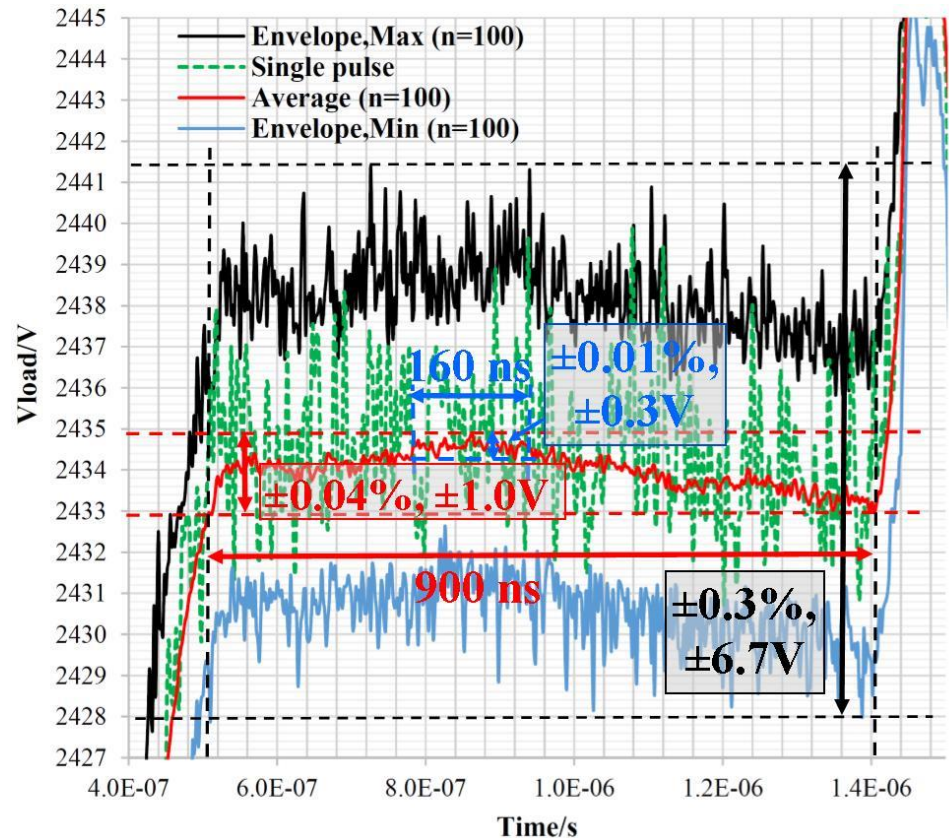
3.5 kV, 5-layer, full-scale prototype



2nd inductive adder with an analogue modulation layer only (in series with the 3.5 kV inductive adder)

Setup for the measurement:

- 5 constant voltage layers, 1 active analogue modulation layer
- 2 branches powered per layer, capacitors (24 μF /layer) initially charged to 555 V
- **Active compensation of droop (not ripple)**
- **16-bit (effective) oscilloscope**



- ⇒ Flat-top stability: $\pm 0.01\%$ ($\pm 0.3\text{V}$) over 160 ns and $\pm 0.04\%$ ($\pm 1.0\text{V}$) over 900 ns, at $\sim 2.4\text{ kV}$!
- ⇒ CLIC DR ext. kicker requirement: $\pm 0.02\%$ over 160|900* ns at 12.5 kV (*160 ns + 580 ns gap + 160 ns)
- ⇒ Min/max envelopes $\pm 0.3\%$ ($\pm 6.7\text{V}$) over 900 ns for 100 pulses, however, these are **NOT** dominated by the flat-top repeatability of the inductive adder (see next slides)!
- ⇒ CLIC DR ext. kicker requirement for flat-top repeatability: $\pm 0.01\%$ over 160|900* ns.



Measurements on Prototype 3: w/o Modulation

Setup for the measurement:

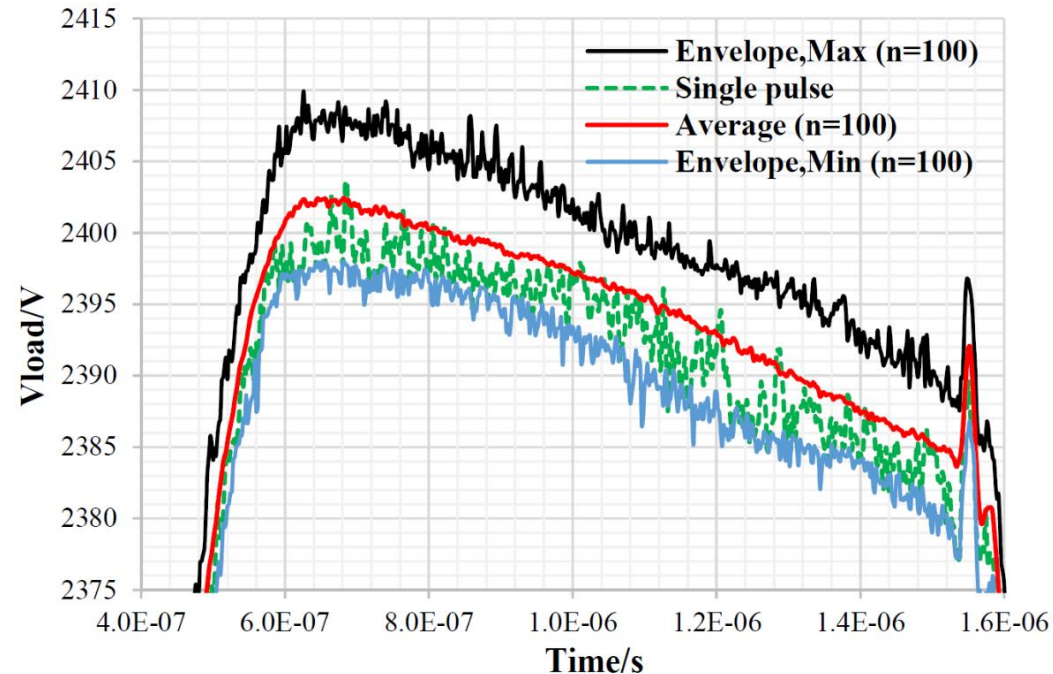
- 5 constant voltage layers
- 2 branches powered per layer, capacitors ($24 \mu\text{F}/\text{layer}$) initially charged to 500 V
- **No compensation**
- **16-bit (effective) oscilloscope**

- ⇒ Flat-top stability $\pm 0.4\%$ over 900 ns (~ 20 V droop), at ~ 2.4 kV.
- ⇒ Min/max envelopes $\pm 0.3\%$ over 900 ns, the same amplitude as with modulation (in the previous slide).

- ⇒ **In series of measurements (100, 200, ..., 500 V per layer) it was found that min/max envelopes were in all measurements $\pm 0.2\%$ of the maximum range of the channel of an oscilloscope (three different settings tried).**
 - 2 different HV power supplies tested: no effect on min/max envelopes.
 - Outputs of HV and LV power supplies filtered (CM & DM): no effect on min/max envelopes.

⇒ **Conclusion: flat-top repeatability of the inductive adder can be significantly better than the measured min/max envelopes of the direct measurement with an oscilloscope!**

- ⇒ Two other measurement techniques applied:
 - Pulse cancelling technique (difference of two pulses with opposite polarities)
 - Balanced measurement (with a differential amplifier)





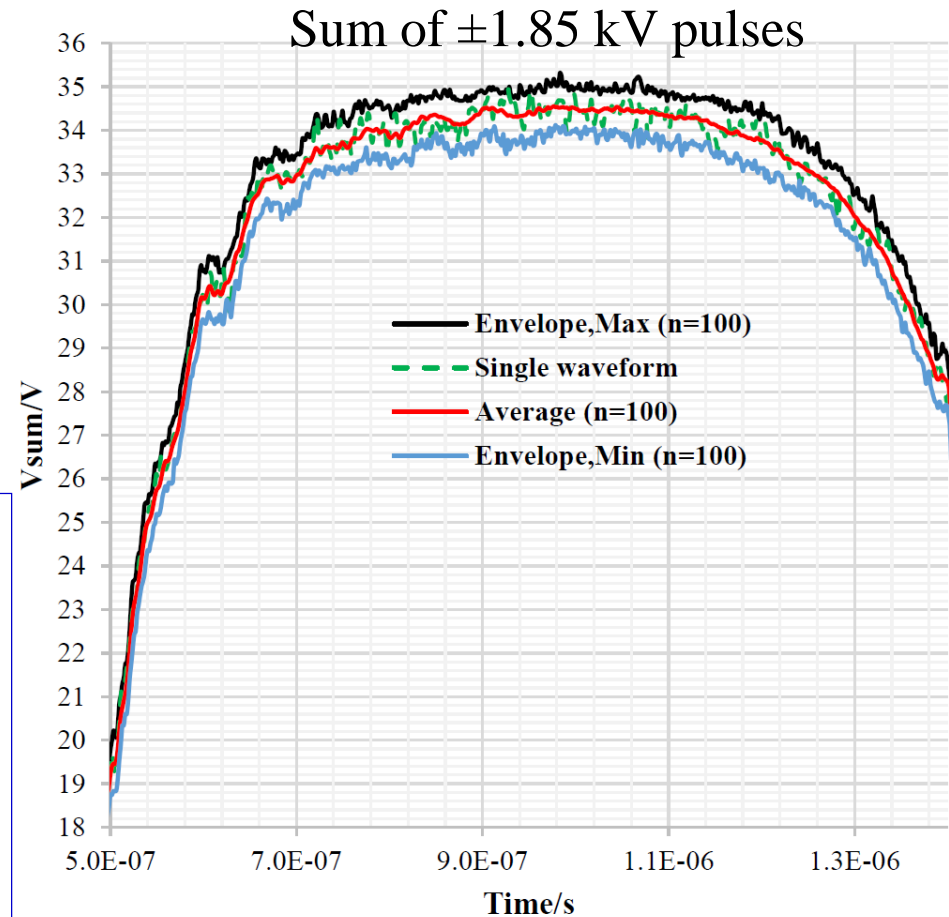
Prototype 3: Measurement with Pulse Cancelling Technique



A single current transformer to measure 2 pulses, with opposite polarities.

Setup for the measurement:

- 2 prototype inductive adders: one of the first 5-layer, 3.5 kV, prototypes and the new, full-scale, 5-layer, 3.5 kV prototype.
- 4 or 8 branches powered per layer, capacitors (24 μF pr 48 μF /layer) initially charged to 400 V
- **Output voltage of inductive adders: ~ 1.85 kV, sum voltage ~ 35 V.**
- **No Modulation**
- **16-bit (effective) oscilloscope**



- ⇒ Dynamic range of the waveform: ~ 350 V (during rise/fall times)
- ⇒ Min/max envelopes $\pm 0.2\%$ (± 0.9 V) over 900 ns: this is $\pm 0.2\%$ x range, 400 V, of the channel!
- ⇒ **The min/max envelopes were dominated by oscilloscope noise.**

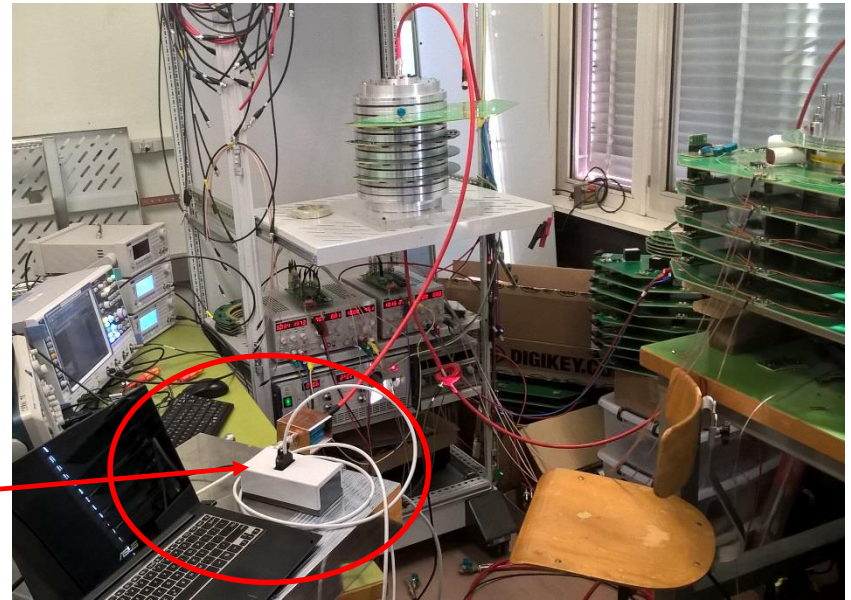


Prototype 3: Measurements with a Differential Amplifier (Balanced Measurement) Setup

Setup for the measurement:

- 5 constant voltage layers
- 1 Passive analogue modulation layer
- 4 branch powered per layer, capacitors (24 $\mu\text{F}/\text{layer}$) initially charged to 125 V
- **Passive compensation of droop**
- **Output voltage ~475 V-**
- **Output voltage measured with a differential amplifier, developed at PSI (M. Paraliev)**

Balanced measurement setup: differential amplifier with a stable DC current source for a reference and fast clamping circuit to filter input signal when it is out of dynamic range.



- ⇒ Pulse-to-pulse stability (flat-top repeatability) measured by recording a mean and standard deviation of the mean for 105 pulses, for 900 ns pulse flat-top duration.
- ⇒ **Measured standard deviation $\sigma = 0.49$ mV, $\pm 3.5 \sigma = \pm 1.7$ mV at 475 V (± 0.0004 %)**
- ⇒ **Flat-top repeatability ± 0.0004 % = ± 4 ppm, $\ll \pm 0.01$ % (CLIC DR ext. kicker requirement)**

- ⇒ Very promising results for repeatability measurement, however relatively low voltage (~475 V).
- ⇒ The balanced measurement setup was optimised for sinusoidal waveform with a fixed frequency, therefore it is not clear how accurate it is for measurements on "rectangular" pulses with fast rise times and wide bandwidth.
- ⇒ Discussion continued with PSI (M. Paraliev): possible to try another setup later this year, with more optimised design for fast rectangular pulses.

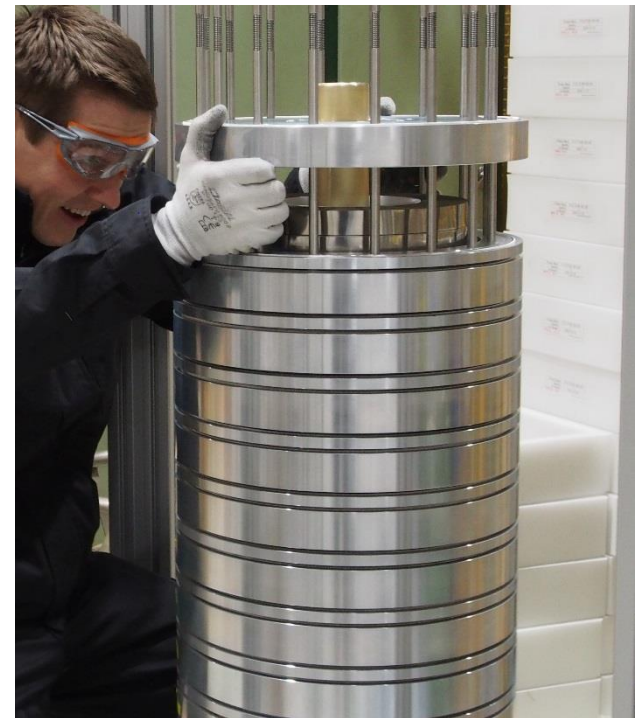


Full-scale 20-layer, 12.5 kV, Inductive Adder

- Two 12.5 kV inductive adders needed to power a stripline kicker.
- Specifications according to requirements for CLIC DR extraction kicker.
- **Target flat-top stability $\pm 0.02\%$ for 900 ns, target flat-top repeatability $\pm 0.01\%$ for 900 ns.**
- Mechanical design and PCB design compatible with 17.5 kV (to a $50\ \Omega$ load)
 - Modifications required: 8 more layers and change of the secondary (a straight rod)
 - 17.5 kV required for CLIC PDR kickers and to test a combined 12.5 kV | 17.5 kV extraction + dump kicker modulator for CLIC DRs.
- Status: the first 20-layer full-scale prototype assembled and measurements commenced.

| Design Parameter | 12.5 kV Prototype Inductive Adder | CLIC DR Extraction Kicker Modulator |
|-------------------------------------|-----------------------------------|-------------------------------------|
| Output Voltage (kV) | 12.5 | 12.5 |
| Output Current | 305* | 250 |
| Voltage per layer | 700 | 700 |
| Number of layers | 20 | 20 |
| Pulse flat-top duration (ns) | 1100 | 160 – 900 |
| Pulse rise time [0.1-99.9 %] (ns) | 100 | < 1000 |
| Pulse fall time [0.1-99.9 %] (ns) | 100 | < 1000 |
| Flat-top stability (for 900 ns) | $\leq \pm 0.02\%$ | $\pm 0.02\%$ |
| Flat-top repeatability (for 900 ns) | $\leq \pm 0.01\%$ | $\pm 0.01\%$ |

*Stripline odd-mode impedance $41\ \Omega$

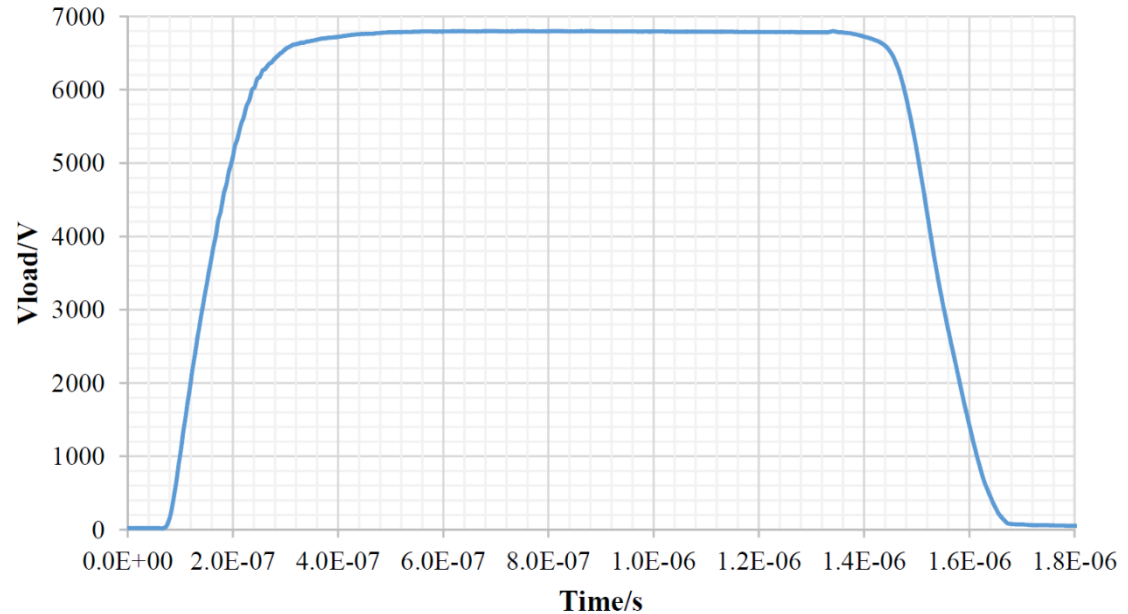
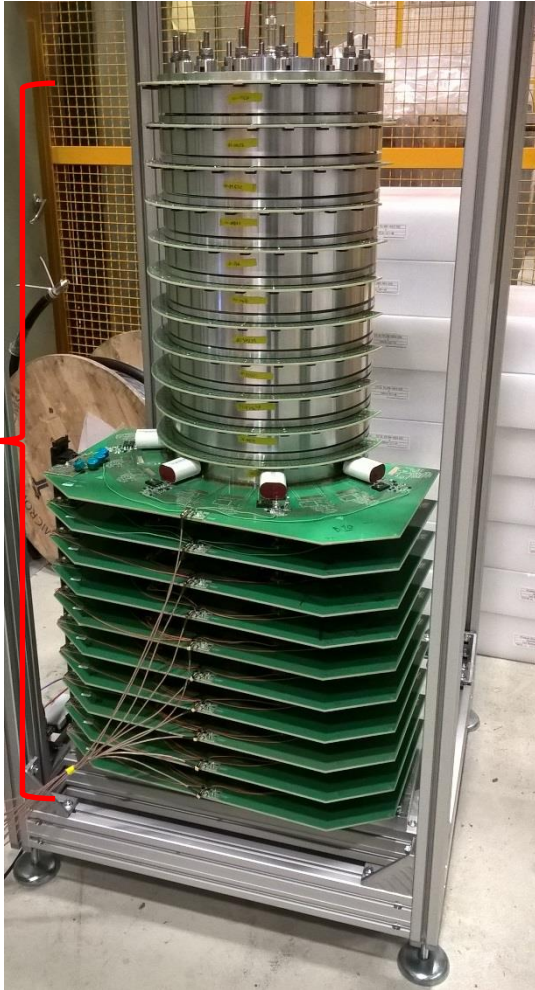


First assembly of the 20-layer, 12.5 kV, inductive adder at CERN



Initial Measurements on 20-layer Prototype

Height
120 cm



■ Setup for the measurement:

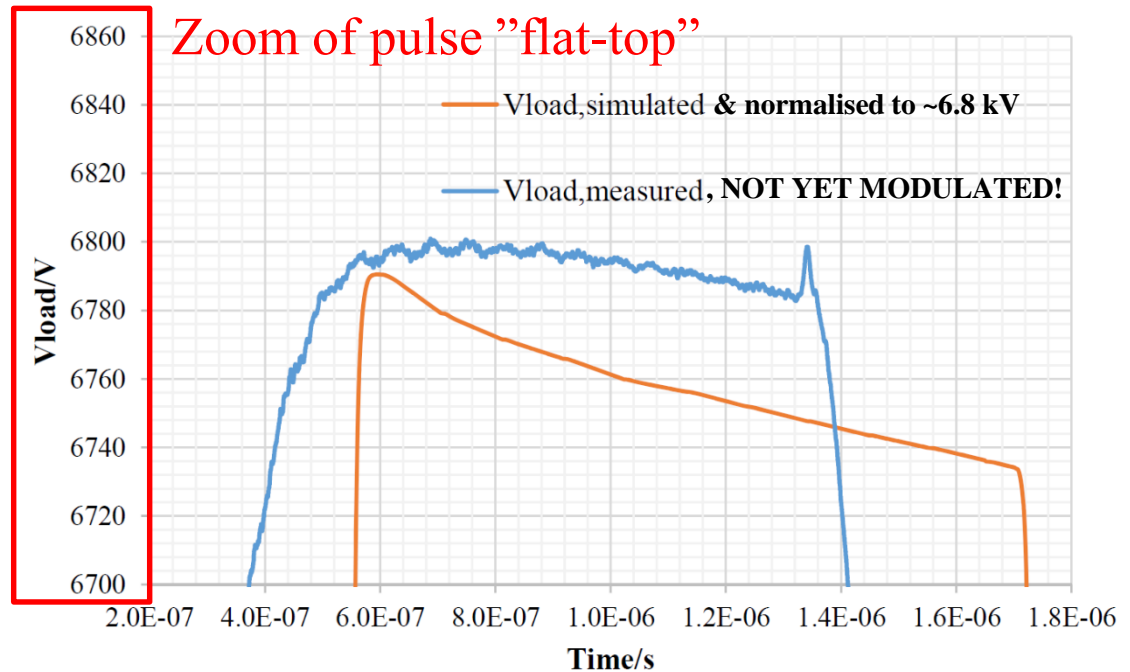
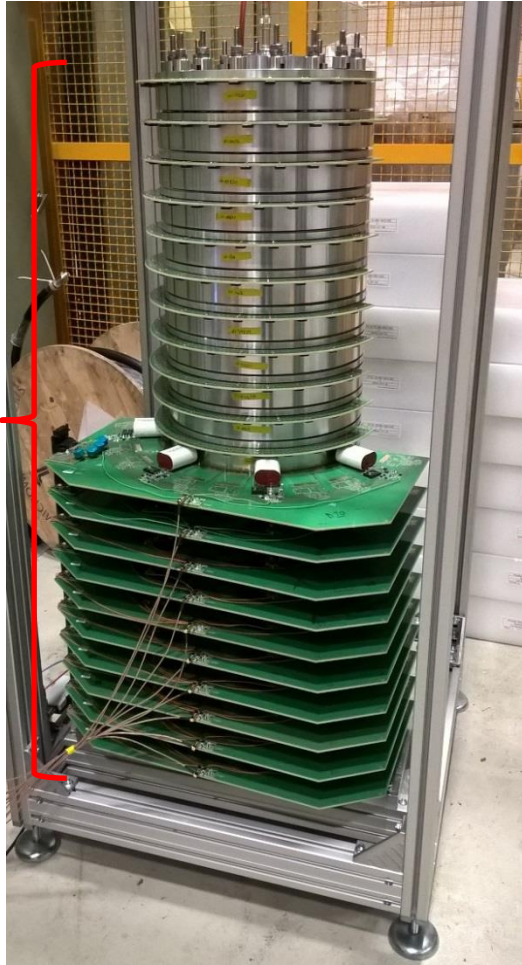
- 20-layer prototype inductive adder
- 10 constant voltage layers, with half-layer PCBs
- 4 branches powered per layer, capacitors ($48 \mu\text{F}/\text{layer}$) initially charged to 700 V.
- **No modulation applied**
- **Output voltage 6.8 kV, droop ~ 15 V for 600 ns.**

⇒ Flat-top stability w/o compensation: ± 0.1 % (± 8.0 V) over 800 ns, at 6.8 kV



Initial Measurements on 20-layer Prototype

Height
120 cm



Setup for the measurement:

- 20-layer prototype inductive adder
- 10 constant voltage layers, with half-layer PCBs
- 4 branches powered per layer, capacitors (48 μ F/layer) initially charged to 700 V.
- **No modulation applied**
- **Output voltage 6.8 kV, droop ~15 V for 600 ns.**

- ⇒ **UPDATE: The required optimal waveform for CLIC DR stripline kicker is a "controlled decay", not a "flat-top" (see talk by C. Belver-Aguilar)!**
- ⇒ **Stability and repeatability requirements remain unchanged.**
- ⇒ **According to simulations, this waveform can be generated by applying active modulation, with the same design of the inductive adder and the modulation layer as required for "flat-top".**

- **The pulse power modulators for CLIC DR kicker systems are very probably feasible with inductive adder technology.**
- As next: measurements on the 20-layer, 12.5 kV, 308 A, prototype inductive adder with **nominal specifications for CLIC DR extraction kicker** (tested up to 6.8 kV now)
 - Required "controlled decay" waveform, with stability to $\pm 0.02\%$ and repeatability to $\pm 0.01\%$ for 900 ns.
 - Active analogue modulation layer with droop and ripple compensation.
 - Revisions required for half-layer PCBs, to be finished by the end of March. New PCBs in April/May 2016.
 - Measurements with balanced measurement setup.
- Assembly of 28-layer layer prototype: combined 12.5 kV extraction kicker + 17.5 kV dump kicker prototype.
 - Mechanical parts ordered, available in April 2016.
- **Future measurements of two 12.5 kV inductive adders with a stripline kicker installed in a beamline in an accelerator test facility (at Alba Cells in Spain).**
- **Much interest for inductive adder technology at CERN, regarding e.g. FCC and PS KFA kicker systems.**



The first 20-layer inductive adder prototype at CERN



References and Bibliography

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