The CMS Tracker Upgrade for the High Luminosity LHC

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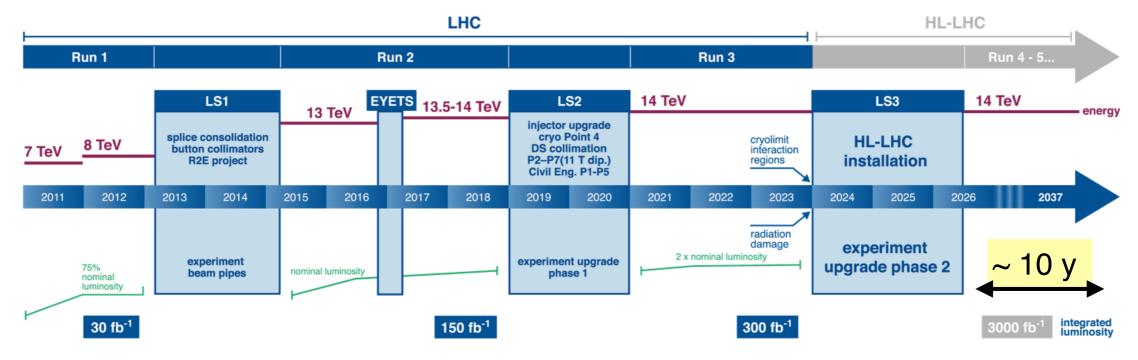
on behalf of the CMS Collaboration

EPS-HEP2019 - Ghent - 10-17 July 2019



The HL-LHC technological challenge





int. lumi 3000-4500 fb-1

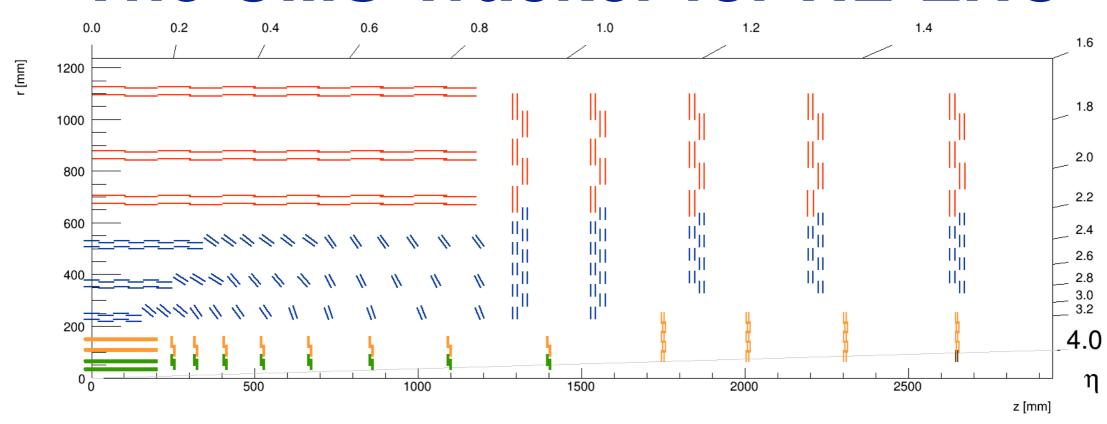
inst. lumi: 5-7.5 x 1034 cm-2s-1

→ <PU> ~ 140-200

- dose & fluence: 10 x higher
- 750 kHz L1 rate
- 12.5 μs L1 latency

The present CMS tracker cannot sustain the implied radiation levels and data rates and has to be completely replaced

The CMS Tracker for HL-LHC

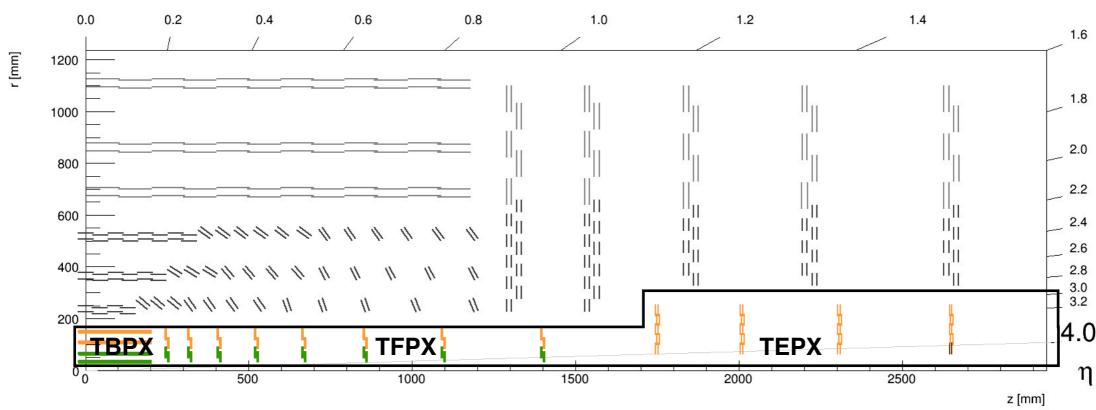


Key features:

- contribute to L1 trigger
- extended tracking coverage (up to η=4)
- high granularity and high bandwidth
 - up to 3.5GHz/cm² occupancy (first layer @ 3cm from beam line)

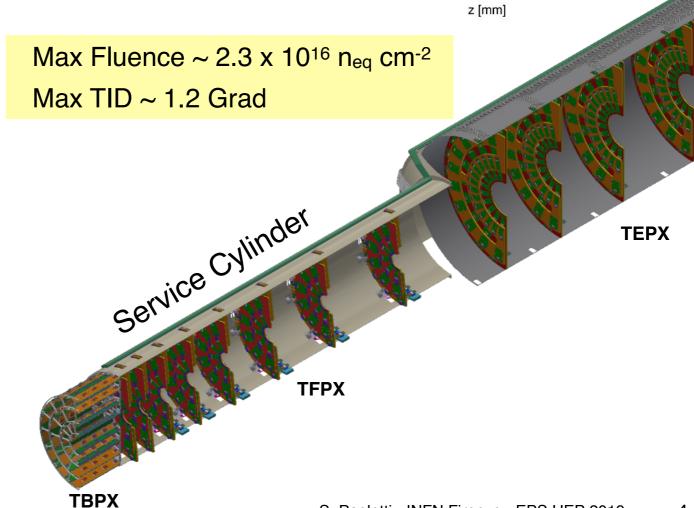
- Thin n-in-p silicon sensors
- Operation at -20 °C
- reduced material budget for improved tracking performance in high PU scenario

The Inner Tracker



Inner Tracker:

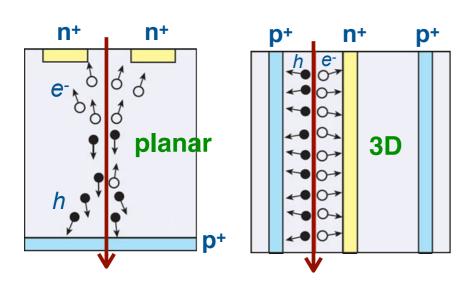
- 3900 modules, 4.9 m², 2×10⁹ pixels
- occupancy: < 0.1%
- Hybrid modules with 2 (1x2) or 4 (2x2) readout chips
- Coverage up to $l\eta l = 4.0$
- Simple mechanics:
 - can be removed for maintenance during LHC shutdowns
 - Barrel: splits in half at z~0
 - Disks: planar geometry (no turbines)



IT: Radiation hard pixel silicon sensors

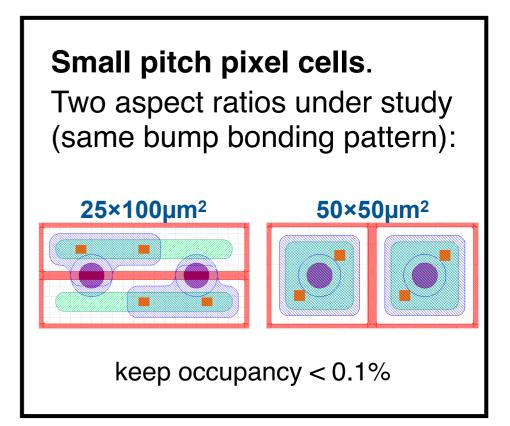
Planar thin (100-150 μ m thick) **n-in-p** pixel sensors:

- up to 0.8-1kV bias @ end of lifetime
- spark protection between r/o chip and sensor



3D sensors option for innermost layers:

- + more radiation hard
- + lower bias needed
- larger cell capacitance
- more complex fabrication



Extensive R&D still ongoing:

More in Davide Zuolo's presentation
later in this session

IT: radiation hard readout chip

- Being developed by the RD53 Collaboration
 - both ATLAS and CMS inner detectors
- 65 nm CMOS technology
- $50x50 \mu m^2$ cell size
- low-threshold (≤ 1000 e⁻)
- high hit and trigger rate:
 - 160 Mbps control & up to 4 x1.28Gbps output links
- Support for serial powering scheme
- chip size(CMS): 16.8 x 21.6 mm² (336 x 432cells).

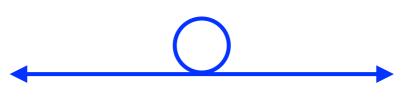
- RD53A: first prototype (~1/2 size of final chip)
- technology and design concepts demonstrated, lot of R&D performed:
 - Radiation hardness tested above 500 Mrad

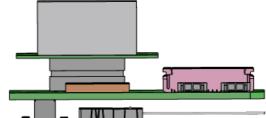


CMS r/o chip prototype submission in 2020

IT: Link to DAQ and CTRL

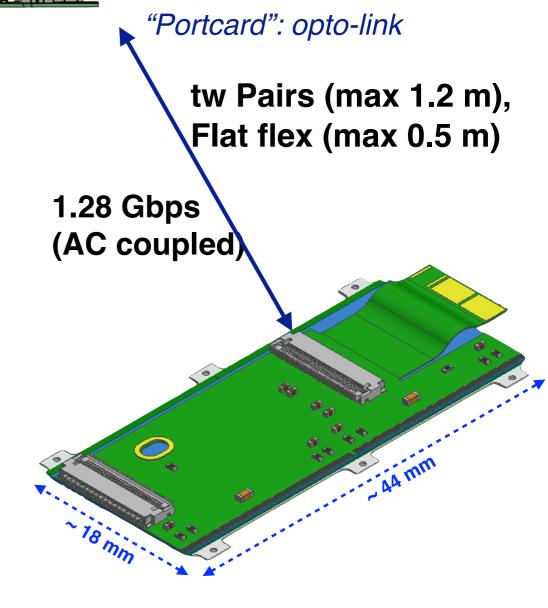
Backend electronics (DTC)



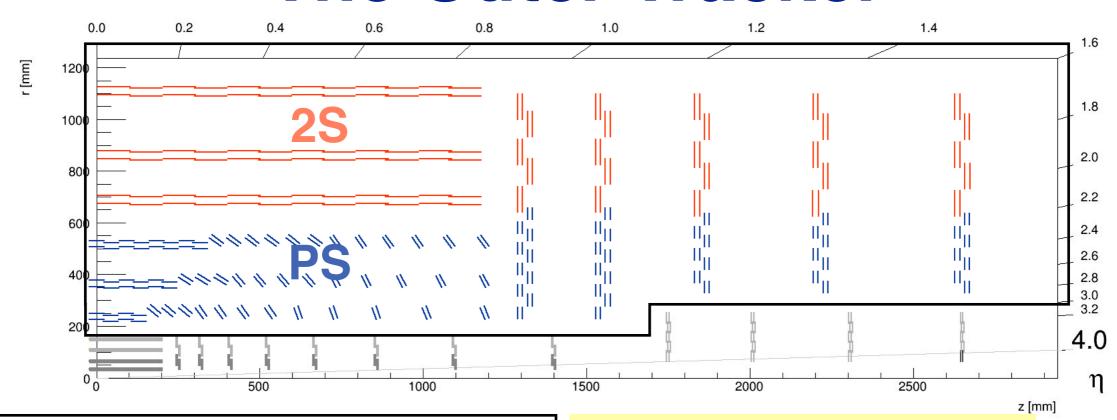


DAQ and CTRL

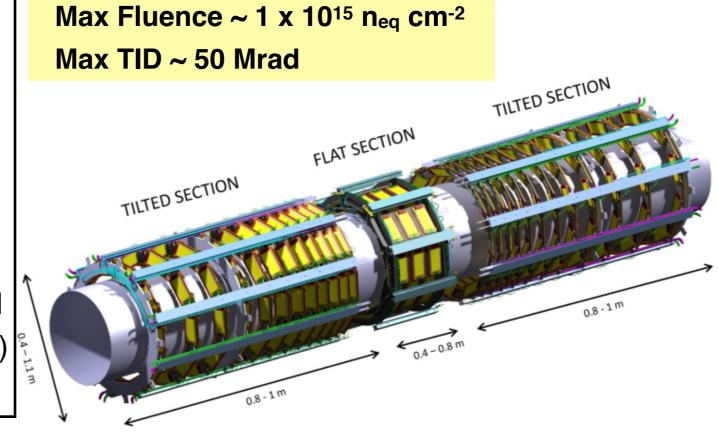
- ~ 750 opto-boards ("portcards") integrated in the Service Cylinder implement advanced optical links communicating with the DAQ and Control backend systems
- AC-coupled e-links ensure the communication between the r/o chip and the portcards:
 - Up to 6 up-links @1.28 Gb/s per module
 - One down-link @160 Mb/s per module
- A High Density Interconnect flex-circuit provides decoupling capacitors and connectors to data e-links and power
- The r/o chip is the only active component in IT modules



The Outer Tracker



- 13200 "Pt modules" (providing L1 primitives):
 - Strip-Strip (2S)
 - macroPixel-Strip (PS)
- L1 Coverage up to lηl ~ 2.5
- 192 m², 42M strips, 170M macro-pixels
- occupancy < 1%
- Innovative tilted geometry in the inner barrel
 - reduces #PS modules → (mass and cost)
 - better trigger performance



Tracking @ L1 trigger

 P_t resolution, e- γ discrimination, isolation \rightarrow better trig selectivity needed to exploit high luminosity:

- An FPGA-based "track-finder" system performs pattern recognition + track fitting
- The track finder processes "stubs" relative to tracks with P_t > 2GeV sent by the Outer Tracker

More about the HL-LHC CMS L1 trigger in the talk by Cecile Sarah Caillol tomorrow morning

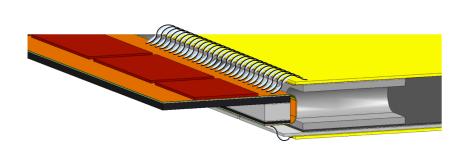
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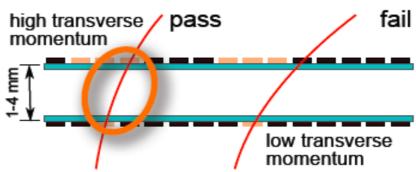
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Pt discriminating module concept:

- two silicon sensors with small spacing in a module
- one ASIC correlates data from both sensors selecting tracker "stubs"





distance depends on layer radius:

More about the HL-LHC CMS L1

trigger in the talk by Cecile Sarah

Caillol tomorrow morning

→ keep selectivity p_t >2GeV/c

Tracking @ L1 trigger

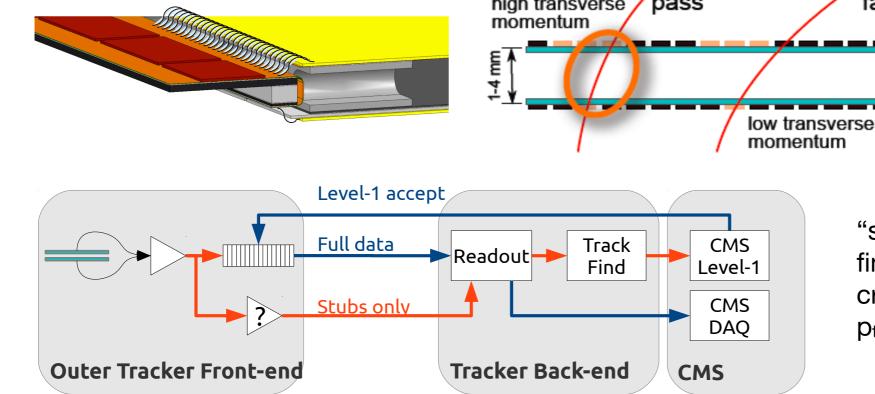
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high transverse / pass

Pt discriminating module concept:

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- one ASIC correlates data from both sensors selecting tracker "stubs"



fail

More about the HL-LHC CMS L1

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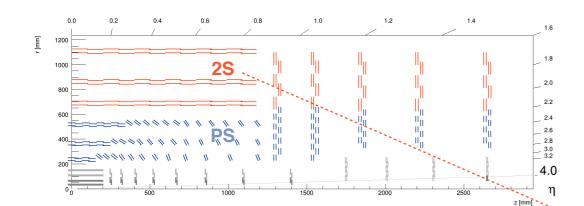
Caillol tomorrow morning

on layer radius: → keep selectivity pt >2GeV/c

distance depends

"stubs" are sent to the track finder backend, and used to create L1 track primitives with pt>2GeV/c @ 40MHz

- @ 40 MHz Bunch crossing
- @ 750 kHz CMS Level-1 trigger



Strip-Strip (2S) modules:

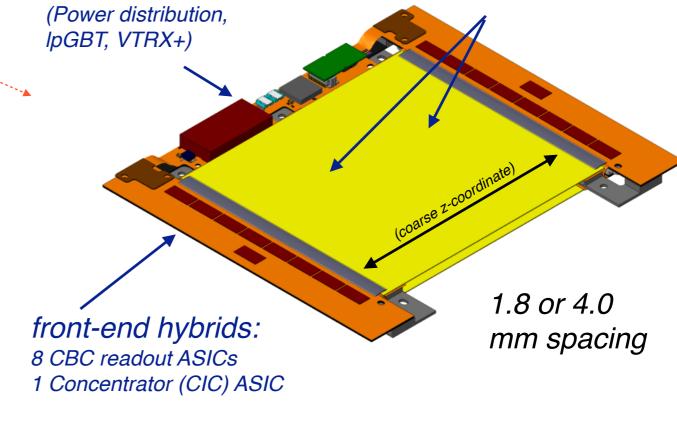
90 cm² active area 2×1016 strips $5 \text{cm} \times 90 \text{ }\mu\text{m}$ (Power distribution, lpGBT, VTRX+)

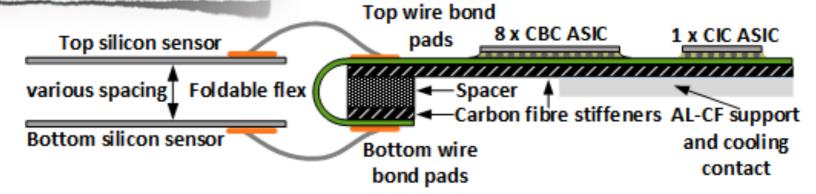
IpGBT = low-power Gigabit Transceiver
VTRx+ = Versatile Link Plus Transceiver

CBC = CMS Binary Chip

→ readout and L1 stub finding

CIC = Concentrator Integrated Circuit Receives L1 information and readout data "Data hub" to service hybrid





Each module is a functional unit individually connected to:

- backend power system
- DTC (= Data, Trigger and Control) system via advanced optical links
- no token control rings
- no intermediate power grouping

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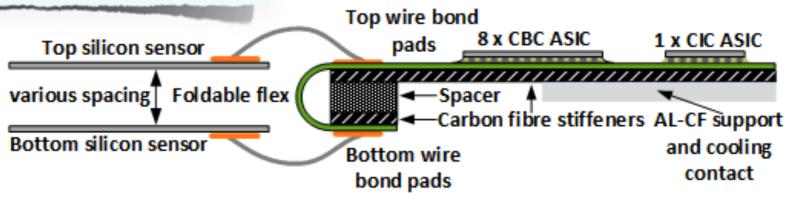
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CIC = Concentrator Integrated Circuit Receives L1 information and readout data "Data hub" to service hybrid

Strip-Strip (2S) modules: 90 cm² active area

service hybrid
(Power distribution, lpGBT, VTRX+)

2 × 1016 strips 5cm × 90 μm
(coarse ² coordinate)



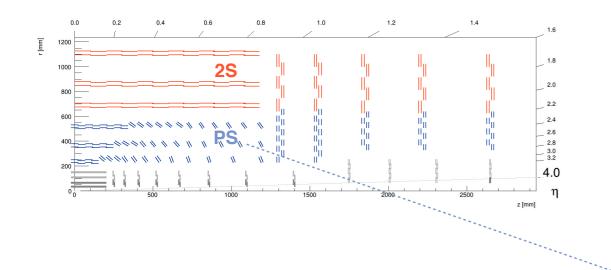
front-end hybrids:

1 Concentrator (CIC) ASIC

8 CBC readout ASICs

1.8 or 4.0

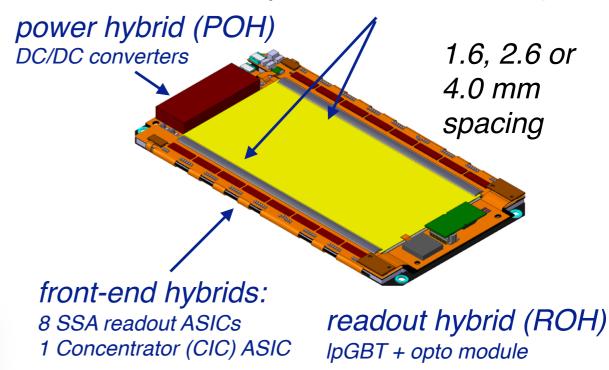
mm spacing



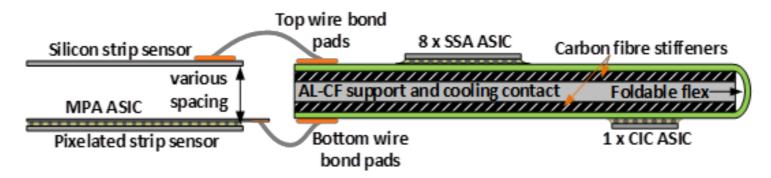
Macro Pixel-Strip (PS) modules:

45 cm² active area:

- 2 × 960 Strips 2.5 cm × 100 μm
- 32 ×960 macro-pixels 1.5 mm × 100 μm

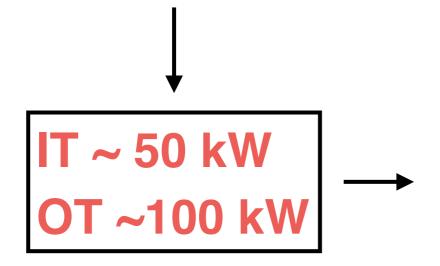


SSA = Short Strip ASIC → readout of short strip sensors **MPA** = Macro Pixel ASIC → readout of Macro Pixel sensors



- Large area + high granularity → large number of channels
- thin sensors → low signal → low threshold and low noise analogue circuits
- high data bandwidth + long (12.5 μ s) L1 latency \rightarrow high digital activity

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High Power Budget

more then 3 times the phase1 tracker

- ~ same available total cable cross section
- keeping low material budget
- delivered at ~ 1÷1.2 V

- Large area + high granularity → large number of channels
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Different power distribution strategies:

- OT: 6-11 V parallel powering with on-module conversion (rad-hard DC/DC converters)
- IT: serial powering (up to 12 modules per chain)

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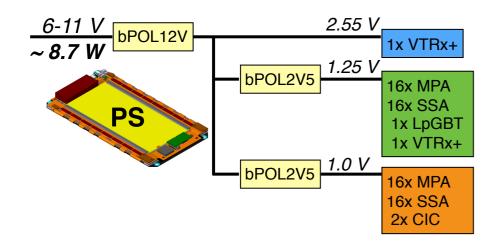
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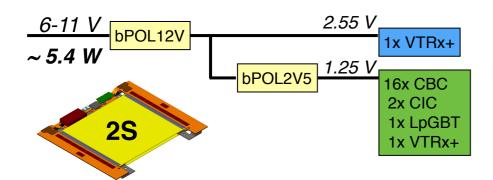
Powerful cooling system:- (4+1) x 50kW cooling plants

- based on two-phase CO₂ cooling system (-30 °C set point)
- small pipes → low material budget

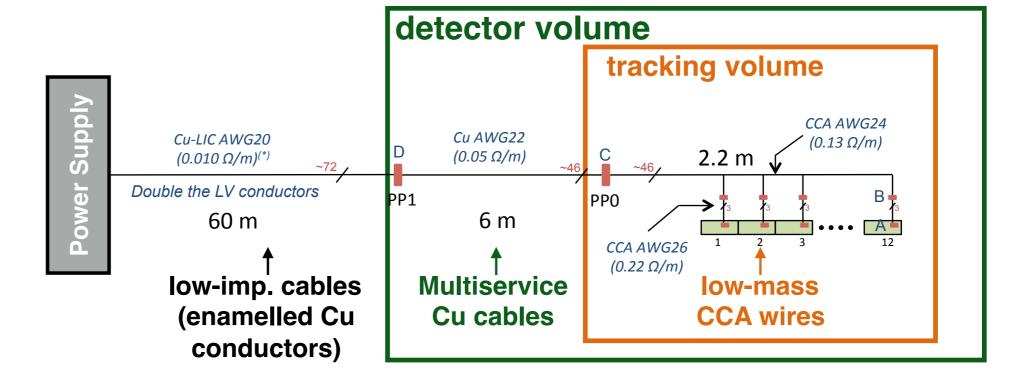


Outer Tracker Power Distribution

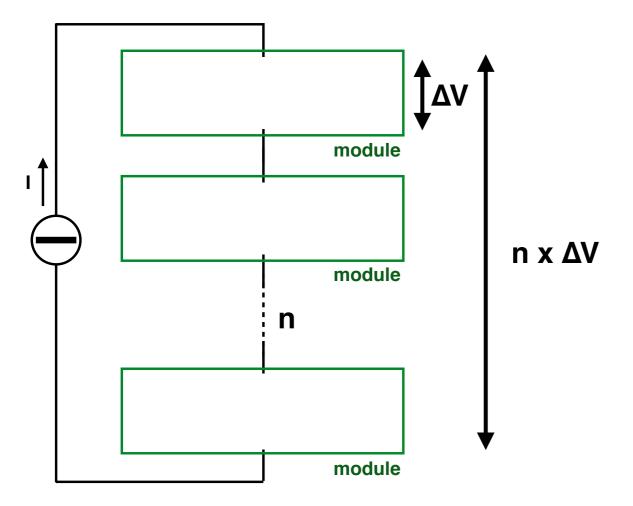




- Each module receives one LV and one HV line
- LV is converted on-module by DC/DC converters (bPOL12V, bPOL2V5)
- 13200 modules operated independently
- Power chain defined:
 - high-granularity power system
 - 12-channel modularity
 - low material budget in tracking region
 - low total resistivity essential
 - thorough study of mechanics and integration details.

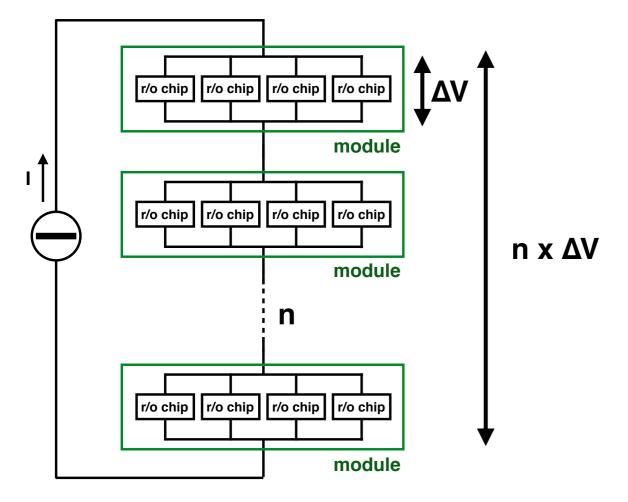


Up to 12 modules connected in one serial chain



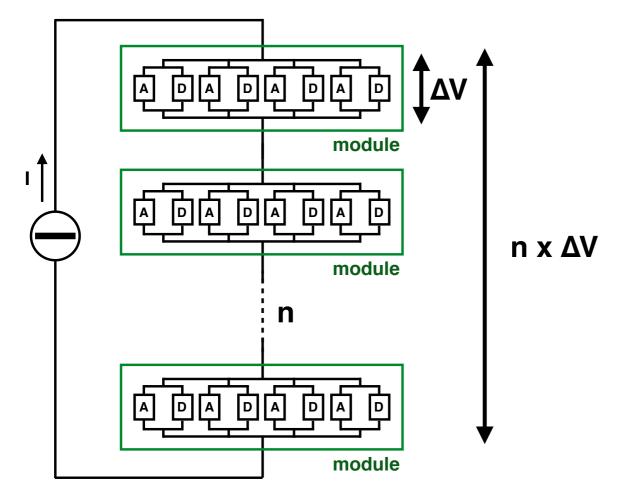
Up to 12 modules connected in one serial chain

Current is shared in parallel b/w r/o chips inside the same module



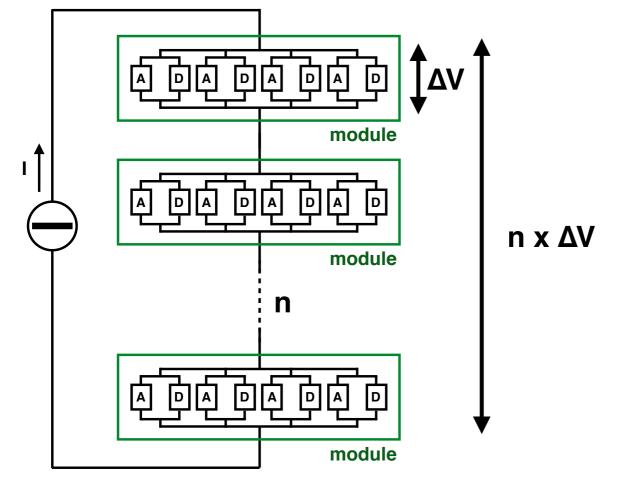
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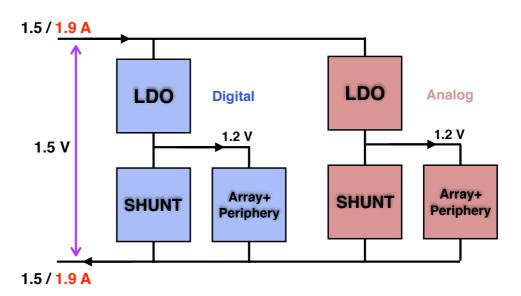
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Serial powering is supported by the r/o chip via the shunt-LDO IP block, providing:

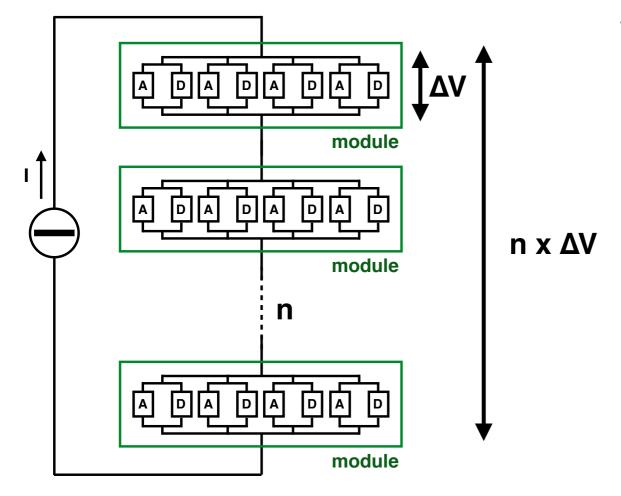
- ⇒ shunt functionality: needed to implement the serial scheme
- → LDO regulation: ensure correct voltage (~1.2V) to the electronics



- the Shunt-LDO configuration defines ΔV=f(I)
- aiming at $\Delta V \sim 1.5 \text{ V} (1.2 \text{V} + 0.3 \text{V for LDO})$
- the chain has to provide enough power for transients: considered ~ 25% current headroom w.r.t. "typical" conditions

Up to 12 modules connected in one serial chain

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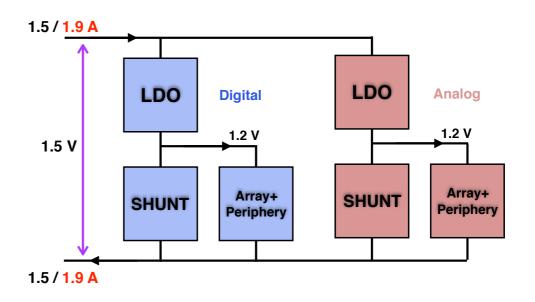


~ 500 serial chains power the full IT

- 4 A chains (2-chip modules)
- 8 A chains (4-chip modules)

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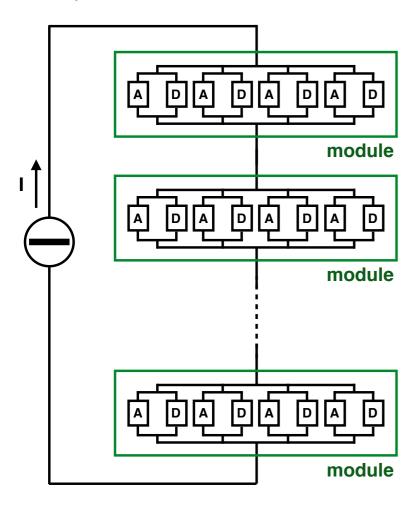
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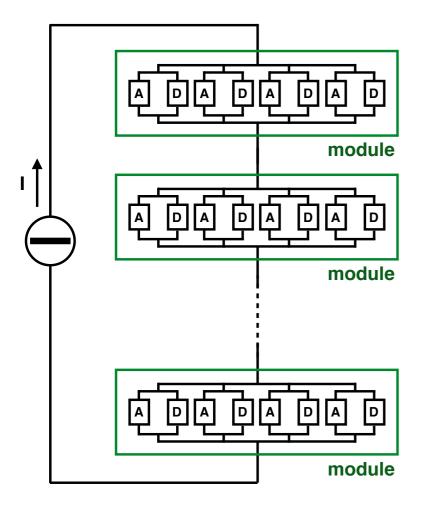
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Active R&D ongoing in ATLAS, CMS and RD53 with tests and simulations:

- Serial chain failure modes
- current sharing
- turn on procedure
- HV distribution in parallel to modules within the same serial chain
- Additional chip protection features under study

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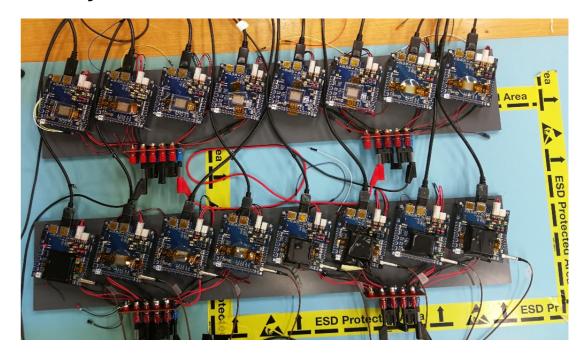
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Serial Powering concept established

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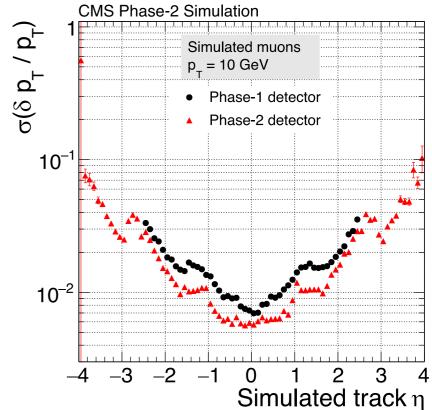
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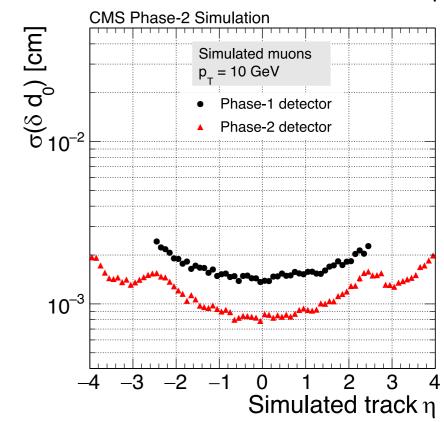


Serial chains with up to 16 RD53A chips were successfully operated in lab

Summary

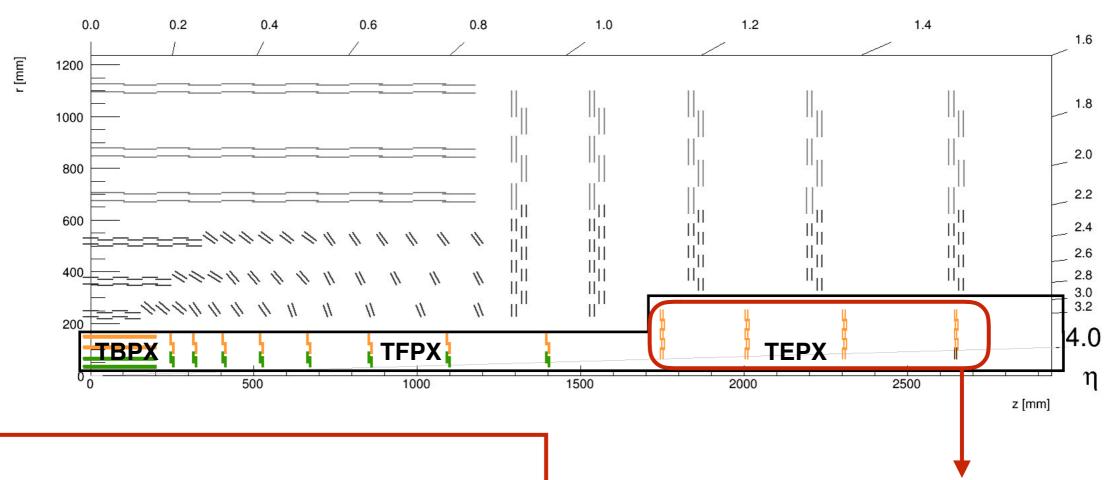
- The upgraded CMS tracker is going to be a radiationhard highly segmented detector designed to operate in the harsh HL-LHC environment and to provide:
 - excellent tracking performance
 - extended η coverage and luminosity measurement
 - L1 trigger primitives @ 40MHz
- The performance is resting on top of innovative modular, lightweight design choices and new technologies:
 - new rad-hard ASICs and optical links
 - rad-hard thin silicon sensors
 - innovative powering schemes
 - CO₂ cooling
- Mechanical layout and integration studies are advanced
- Final ASICs prototype submissions expected by 2020
- First module prototypes in 2020
- Way paved towards the new tracker operating inside CMS in 2026





Reserve

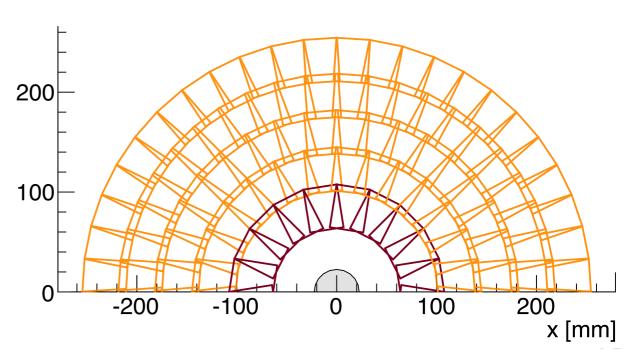
The Inner Tracker



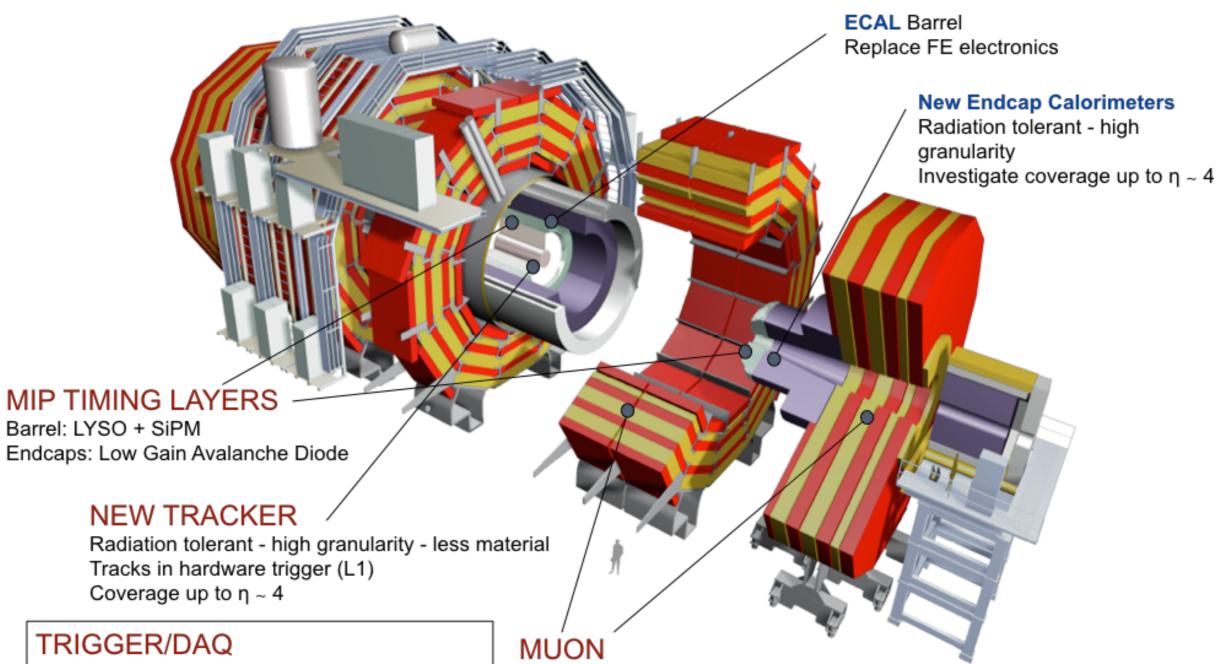
TEPX is a large and powerful luminometer:

- it receives 75 kHz extra lumi triggers (up to 10MHz full bandwidth when no data taking)
- lumi is measured via cluster counting, multihit stub counting, track counting, ...

First ring of the last disk is fully dedicated to background monitoring, with separate readout and control

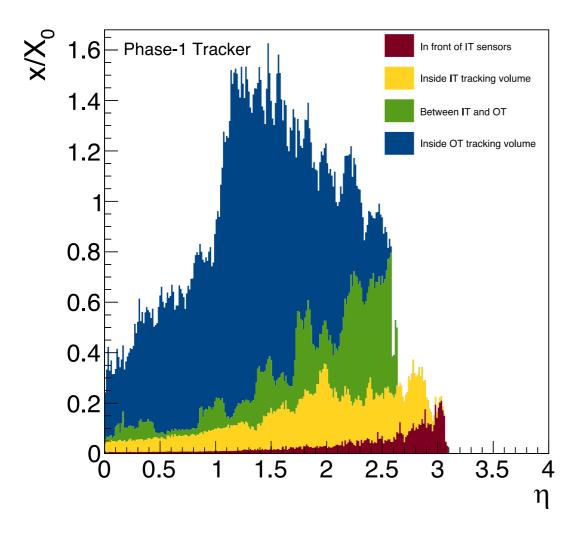


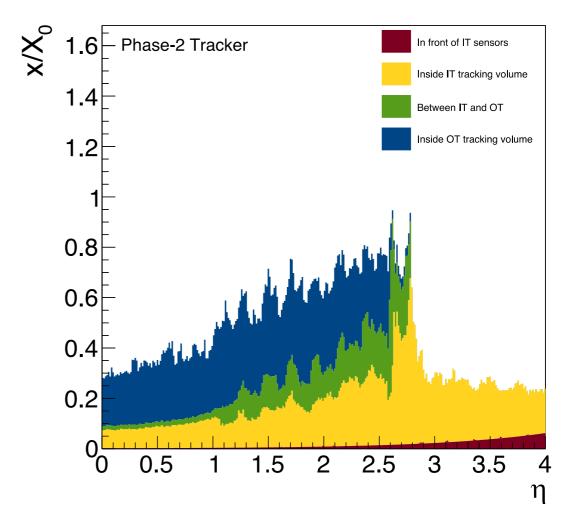
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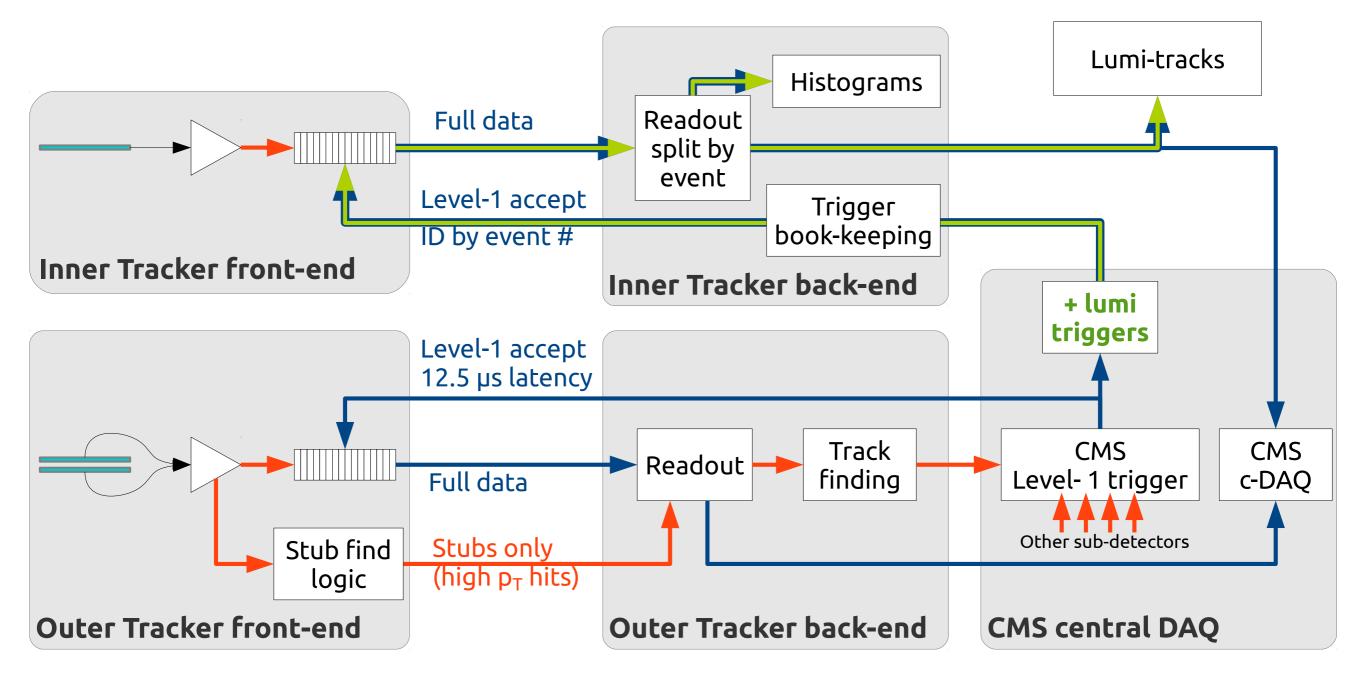


L1 (hardware) with tracks and rate ~750kHz Latency ≥ 10 µs HLT output up to 10 kHz

Replace DT FE electronics Complete RPC coverage in forward region (new GEM/RPC technology) Investigate Muon-tagging up to $\eta \sim 4$



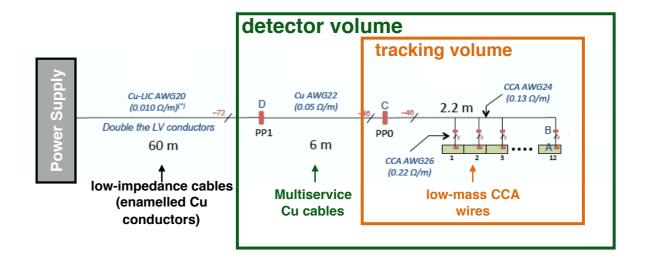




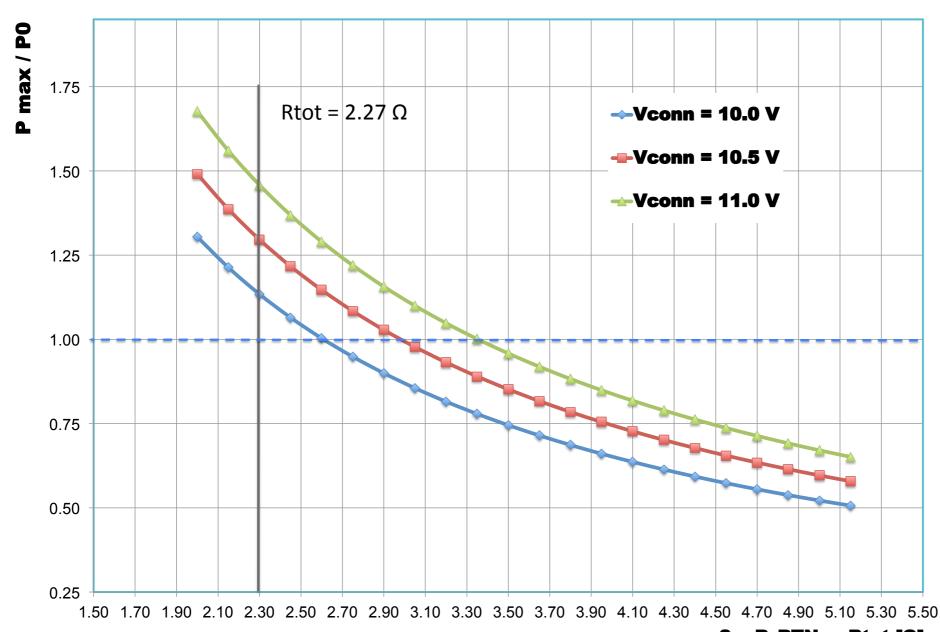
40 MHz – Real time

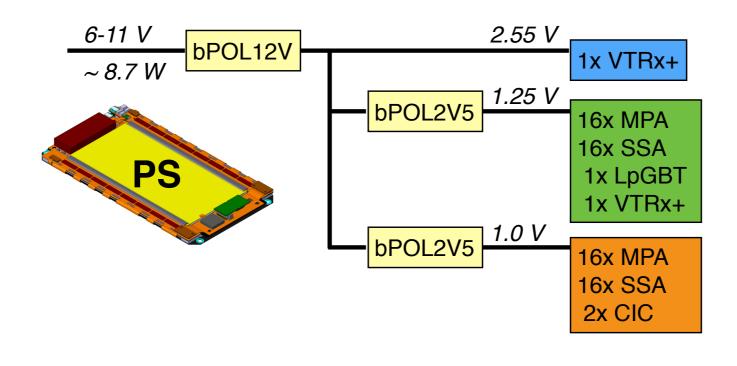
750 kHz – CMS Level-1 trigger

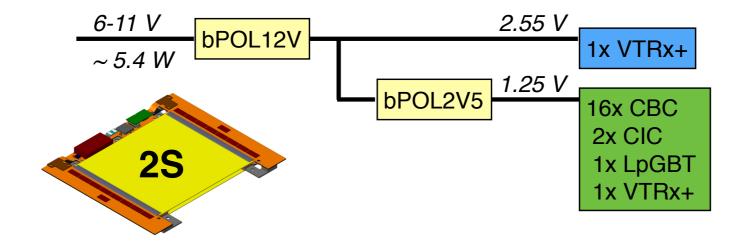
~75 kHz – Lumi-specific trigger

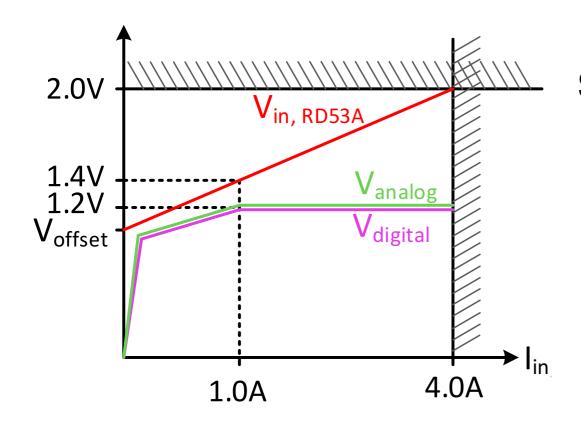


P0 = 8.7W



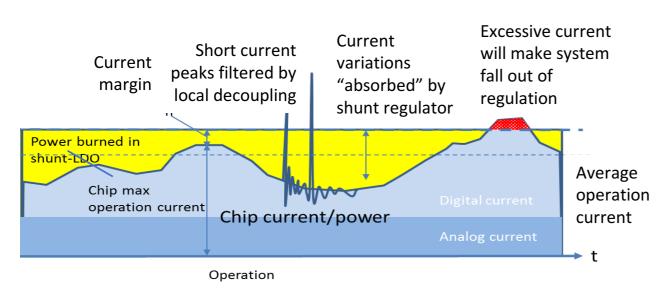


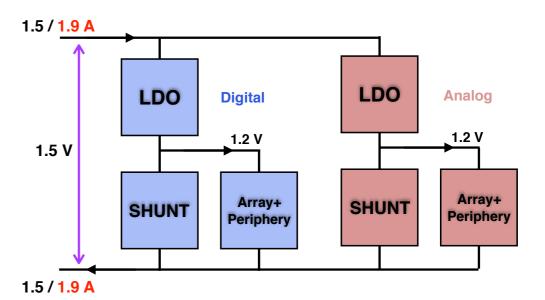


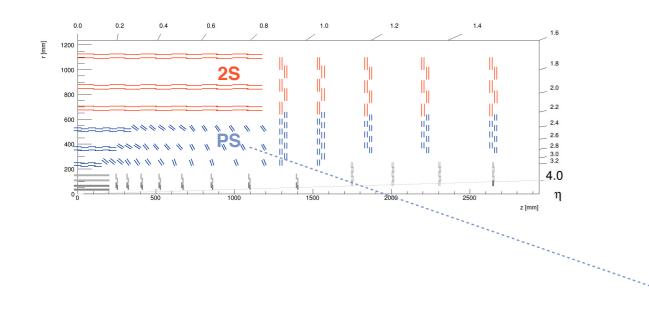


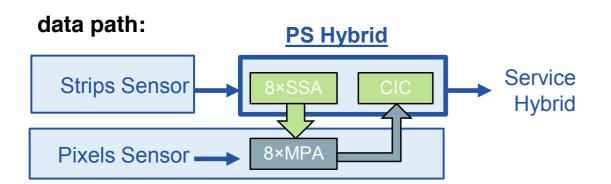
Serial Power chains are current driven:

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- aiming at $\Delta V \sim 1.5 \text{ V} (1.2 \text{V} + 0.3 \text{V for LDO})$
- the chain has to provide enough power for transients: considering ~ 25% current headroom w.r.t. "typical" conditions
 - → serial powering is intrinsically not efficient









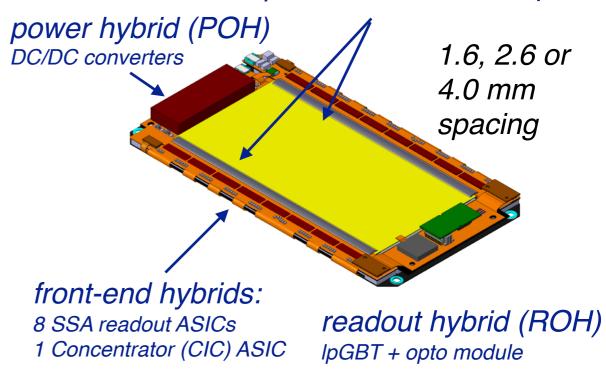
SSA = Short Strip ASIC → readout of short strip sensors

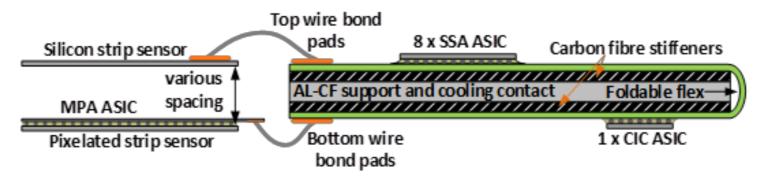
MPA = Macro Pixel ASIC → readout of Macro Pixel sensors

Macro Pixel-Strip (PS) modules:

45 cm² active area:

- 2 × 960 Strips 2.5 cm × 100 μm
- 32 ×960 macro-pixels 1.5 mm × 100 μm





Tracking at L1 trigger level (5 μ s latency)

Pattern recognition:

- Tracklet approach:
 - stubs in adjacent layers → "Tracklets"
- Hough Transformation approach:
 - Select track candidate through Hough Transform

track fitting:

- Minimize chi2 (Kalman Filter)
- Remove duplicate

