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New Level-1 jet feature extraction modules for ATLAS phase-I upgrade

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After the second long-shutdown, in 2021, the LHC will be a new machine in many respects and produce collisions with a center-of-mass energy at or near 14 TeV. The instantaneous luminosities can be expected to reach 3x10ˆ34 cmˆ-2sˆ-1, which is three times the original design value. The mean number of interactions per bunch crossing is expected to go up to 80. To meet these challenges of this high-luminosity environment, the ATLAS detector will have several major upgrades to be installed during Long Shutdown 2 (Dec. 2018 to Feb. 2021). As a part of the updates, the Level-1 calorimeter trigger will be upgraded to exploit the finer granularity data by using a new system of feature extraction (FEXs) modules, which each reconstructs different physics objects at Level-1.

The Jet FEX (jFEX) is one of three FEXs and has been conceived to identify small/large area jets, large-area tau leptons, missing transverse energy and the total sum of the transverse energy. The use of the latest generation Xilinx Field Programmable Gate Array (FPGA), the UltraScale+, was dictated by the physics requirements which include substantial processing power and large input bandwidth, up to 3Tb/s, within a tight latency budget less than 390 ns. The jFEX board is characterized by a modular design that makes it possible to optimize within the limited space of an ATCA board a large number of high-speed signals. To guarantee the signal integrity, the board design has been accompanied by simulation of the power, current and thermal distribution. The printed circuit board has a 24-layer stack-up and uses the MEGTRON6 material, commonly used for signal transmission above 10 Gb/s.

The talk will focus on the technological aspects of the jFEX board, reporting on the simulation studies and on the design solutions of the board. Two jFEX prototypes and one preproduction module have been produced and being tested at CERN with other systems, these test results will be presented. The firmware implemented on the trigger board will be illustrated in connection with the FPGA performance and board power consumption. The whole jFEX system, consisting of 6 boards, will be produced by the end of 2019 to allow the installation and commissioning the full system in time for the LHC restart at the beginning of 2021.

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