Contribution ID: **155** Type: **Parallel talk**

ATLAS Level-0 Endcap Muon Trigger for HL-LHC

Friday, July 12, 2019 10:45 AM (15 minutes)

The design for the Level-0 endcap muon trigger of the ATLAS experiment at High-Luminosity LHC (HL-LHC) and the status of the development are presented. HL-LHC is planned to start the operation in 2026 with an instantaneous luminosity of 7.5 x 10^34 cm^-2s^-1. In order to cope with the proton-proton collision rate higher than that of LHC, the trigger and readout system needs to be replaced. The new Level-0 endcap muon trigger system is required to reconstruct muon candidates with an improved momentum resolution to suppress the trigger rate with keeping the efficiency. That can be achieved by combining the signals from various subdetectors, thin gap chambers, resistive plate chambers,
micromesh gaseous detectors, and scintillator-steel hadronic calorimeters, to form more offline-like tracks. The combined muon track reconstruction was demonstrated with Monte-Carlo simulation
samples produced with the condition at HL-LHC. The efficiency was estimated to be greater than 90%, a few percents higher than the current system. The trigger rate was evaluated with proton-proton collision data taken with random trigger overlaid to account for a pileup of 200, which is expected at HL-LHC. The obtained value for momentum threshold of 20 GeV, primary threshold assumed for single muon trigger, is about 30 kHz, which constitutes only about 3% of the assumed total Level-0 trigger rate of 1 MHz. Hardware implementation is planned with ATCA blades. Each blade is designed to have a Virtex UltraScale+ FPGA with about hundred pairs of transceivers, which can be used to receive detector signals, and with huge memory resources suited for track reconstruction. The track
reconstruction is based on a pattern matching algorithm using the detector hits and the predefined lists of hits corresponding to tracks. A memory resource UltraRAM integrated into the FPGA is exploited to store the predefined lists of hits. Initial test with the evaluation kit VCU118 showed high efficiency and angular resolution better than the requirement with reasonable memory resources. The bit error ratio of the data transmission with GTY transceivers was evaluated with transfer rates up to 25 Gbps.
The power consumption of a hundred pairs of transmitter and receiver of GTY running with 10 Gbps, which is an average transfer rate assumed for the system, was evaluated to be about 30 W.

Primary author: AOKI, Masato (High Energy Accelerator Research Organization (JP))

Presenter: ASADA, Haruka (Nagoya University (JP))

Session Classification: Detector R&D and Data Handling

Track Classification: Detector R&D and Data Handling