## **EPS-HEP2019**



Contribution ID: 211

Type: Poster

## The ATLAS Level-1 Topological Processor: experience and upgrade plans

Monday 15 July 2019 19:40 (20 minutes)

During Run-2 the Large Hadron Collider (LHC) has provided, at the World's energy frontier, proton-proton collisions to the ATLAS experiment with high instantaneous luminosity (up to 2.1x10<sup>34</sup> cm-2s-1), placing stringent operational and physical requirements on the ATLAS trigger system in order to reduce the 40 MHz collision rate to a manageable event storage rate of 1 kHz, while not rejecting interesting collisions.

The Level-1 trigger is the first rate-reducing step in the ATLAS trigger system with an output rate of up to 100 kHz and decision latency of less than 2.5 µs. Until the end of 2018, an important role was played by the Level 1 Topological Processor (L1Topo). This innovative system consists of two blades designed in AdvancedTCA form factor, mounting four individual state-of-the-art processors, and providing high input bandwidth and low latency data processing. Up to 128 topological trigger algorithms can be implemented to select interesting events by applying kinematic and angular requirements on electromagnetic clusters, hadronic jets, muons and total energy reconstructed in the ATLAS apparatus. This resulted in a significantly improved background event rejection rate and improved acceptance of physics signal events, despite the increasing luminosity. The L1Topo system has become more and more important for physics analyses making use of low energy objects, commonly present in the Heavy Flavour or Higgs physics events for example.

In this presentation, an overview of the L1Topo architecture, simulation and performance results during Run-2 is discussed alongside with upgrade plans for the L1Topo system to be installed for the future data taking that will start in 2021.

Author: STOCKTON, Mark (CERN)

Presenter: ALDERWEIRELDT, Sara (CERN)

Session Classification: Wine & Cheese Poster Session

Track Classification: Detector R&D and Data Handling