Single Event Effects in the ATLAS IBL Frontend ASICS at LHC

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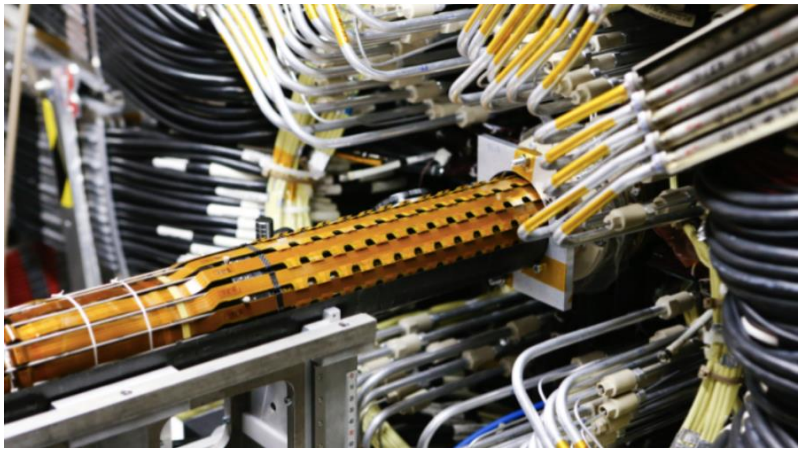
Outline

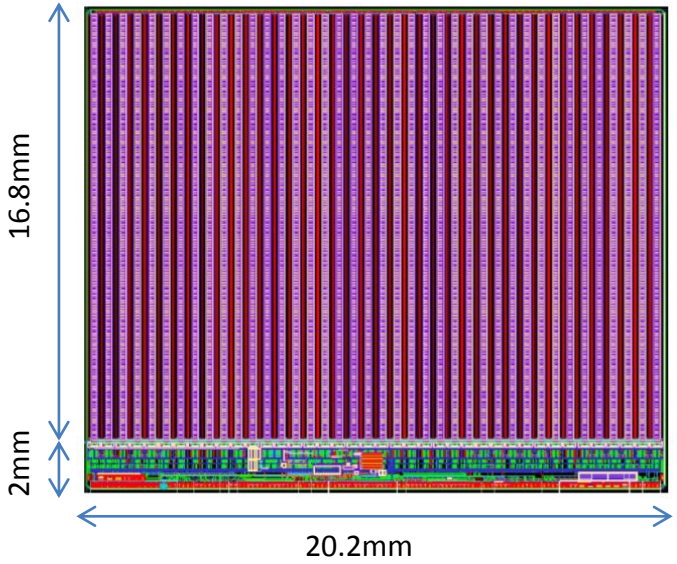
- IBL and the FE-I4 chip
- Single Event Effects observed in FE-I4 global and pixel memory bits
- Memory bit flips rate measurements
- Bits recovery strategies and tests
- Conclusions

Insertable B-Layer (IBL) and FE-I4



- **IBL: The innermost layer of ATLAS Pixel Detector**
  - 14 staves placed around the beam pipe
  - 32 chips on each stave

- **FE-I4 chip**
  - New front-end chip developed for IBL
  - 130 nm CMOS technology
  - 80×336 pixels (26880 pixels)
  - Pixel size: 250×50 μm^2



FE-I4 Config. Registers

Two types of configuration memory

Global registers

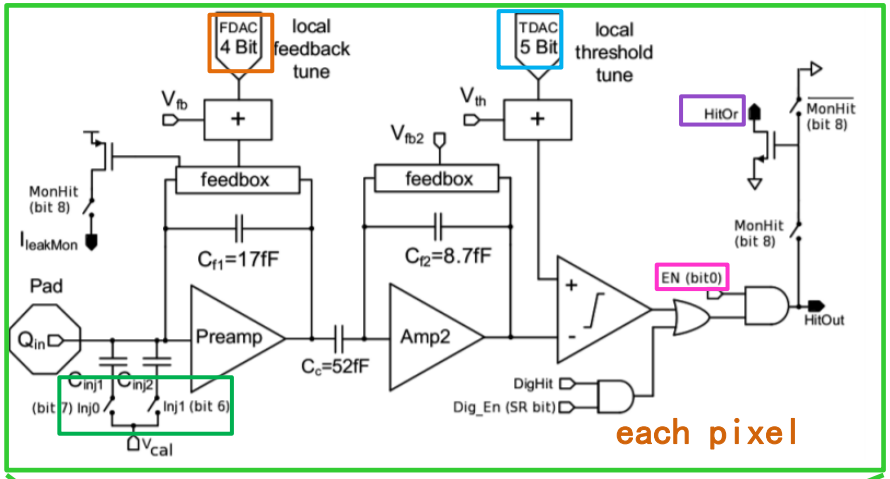
- **in periphery set the chip threshold and Time over Threshold (ToT)**
  - ToT ∝ charge
- 32 registers of 16 bits

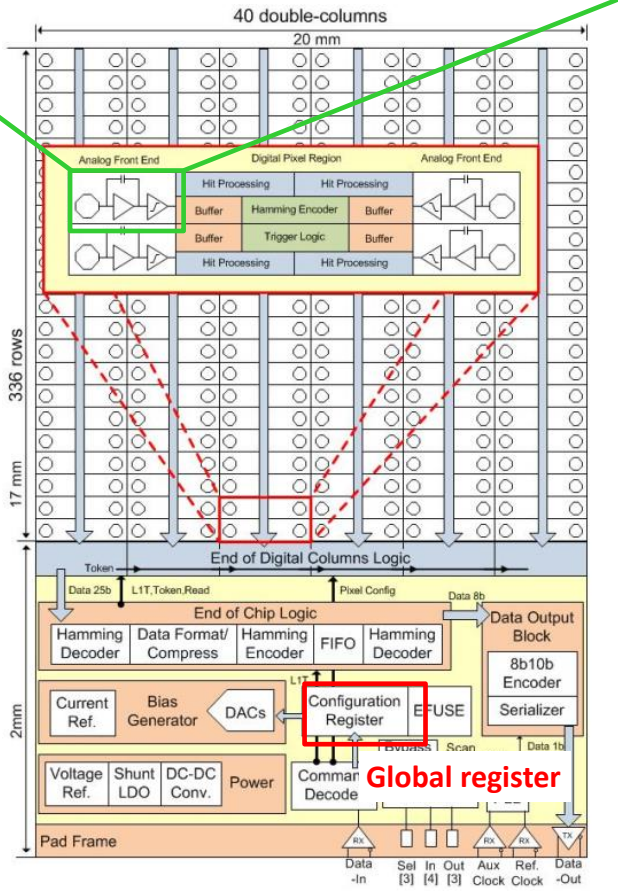
Local registers

- **in each pixel for fine tuning of threshold (5-bit TDAC) and ToT (4-bit TDAC)**
- pixel enable (1-bit), charge injection capacitor choice (2-bit), readout of discriminator(1-bit)
- 13-bits memory per pixel

Critical to be stable in operation

BUT, vulnerable to the Single Event Effects (SEE)





Single Event Upset/Transient

Operation of electronics must contend with both radiation damage from integrated dose and instantaneous Single Event Effects (SEE).

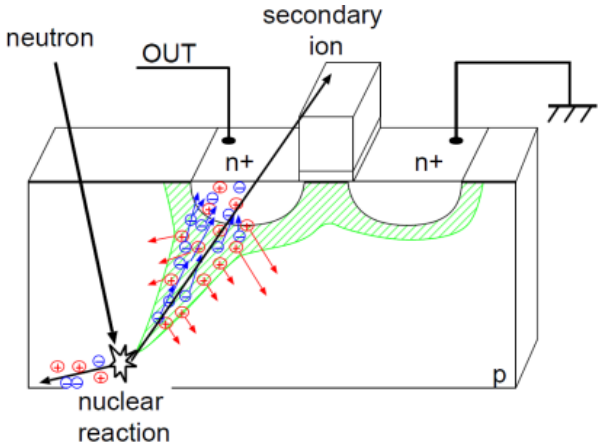
Single Event Upset (SEU)

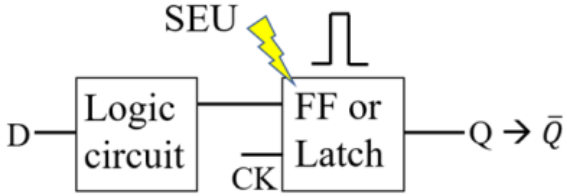
- **A sufficiently large amount of charge flips the state of memory bit**

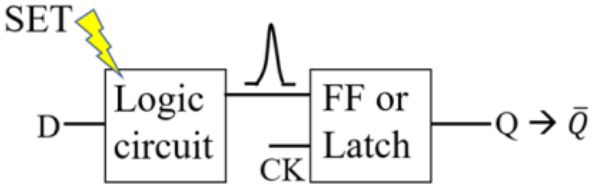
Single event Transient (SET)

- **A glitch travels through combinational logic and is captured into storage element**
- Glitch on the “LOAD” line of register

Memory corruption leads to detuning or disabling of the pixels

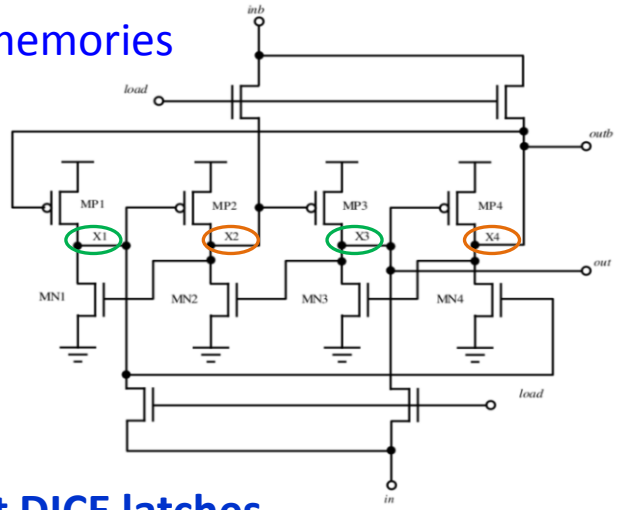




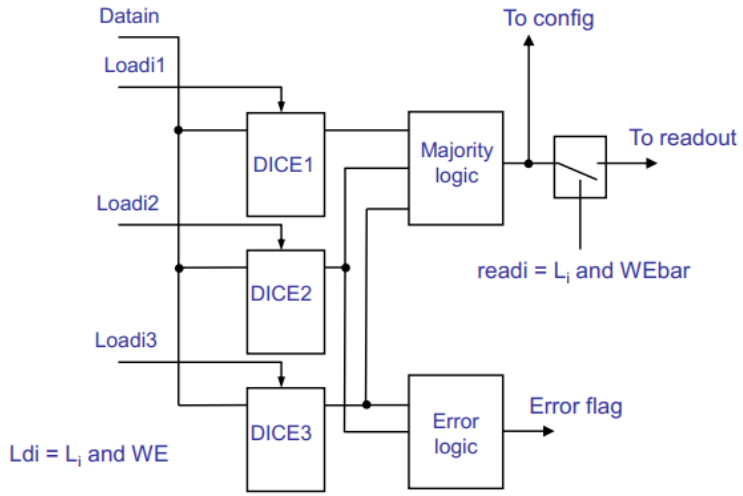


RadHARD Configuration Memory

- **Dual Interlocked CEll (DICE) latch** based configuration memories
  - Cross coupled inverter latch structure
  - This SEU-hardened latch reduce the SEU rate, but do not completely eliminate it.



- **Pixel memory bits** are configured by **single DICE latch**
- **Global memory bits** are configured by **triple redundant DICE latches**

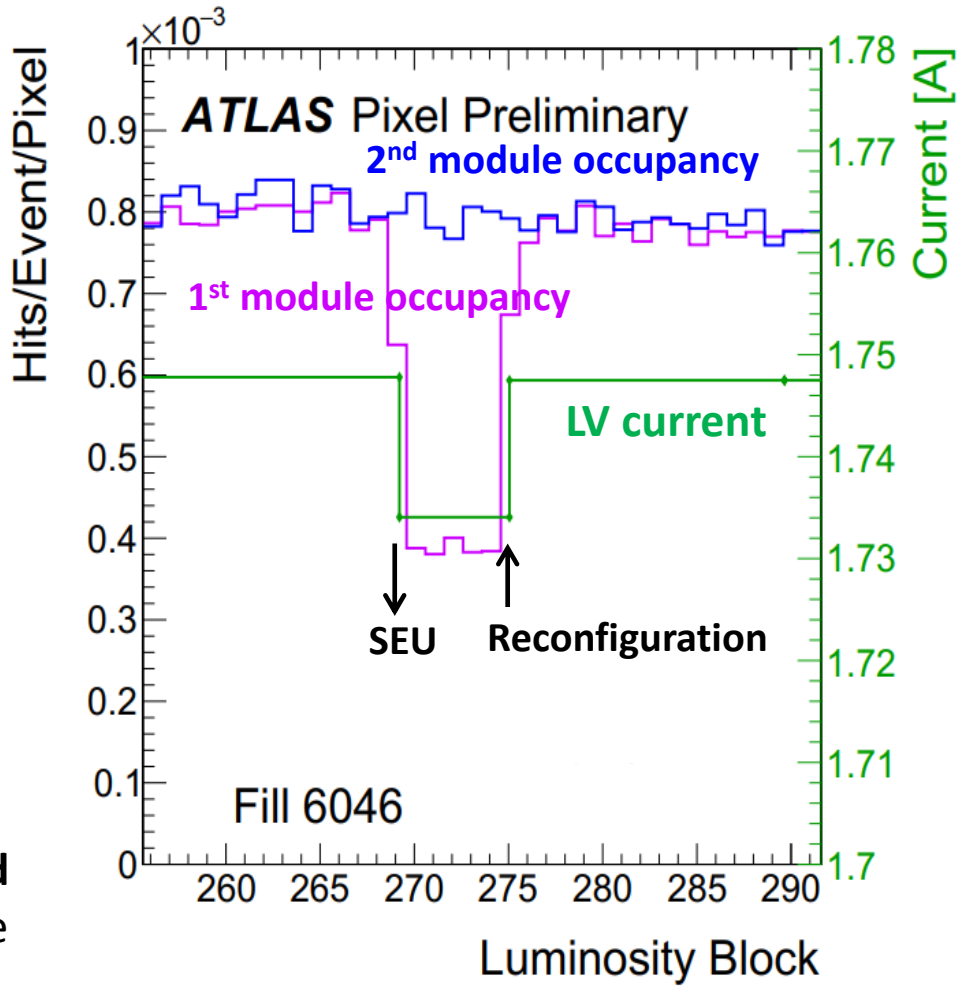


Inside pixel no space for triple DICE latches
→ Single DICE latch for pixel memory bits

- **Single Event Effects observed in FE-I4 global and pixel memory bits**
- Memory bit flips rate measurements
- Bits recovery strategies and tests
- Conclusions

SEEs in Global Memory Bits

- **SEEs in global register has a strong impact on module operation**
  - Affecting the entire chip
- **Drop in both Low Voltage (LV) current and hit occupancy**
  - SEE in one out of two DAQ modules that are served by the same LV channel
  - **A full chip reconfiguration recovered** the initial module occupancy and the LV current consumption

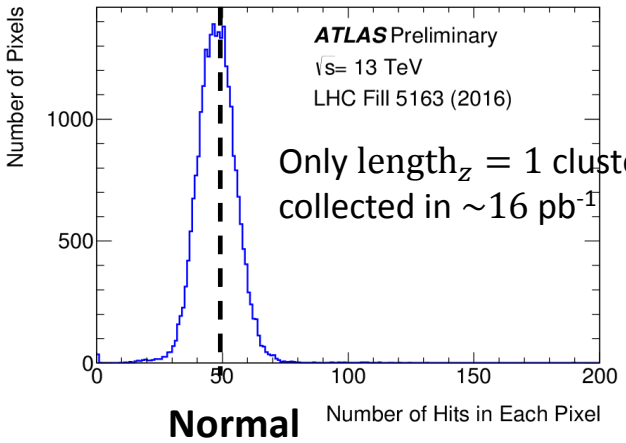


SEEs in Pixel Memory Bits – Noisy Pixels

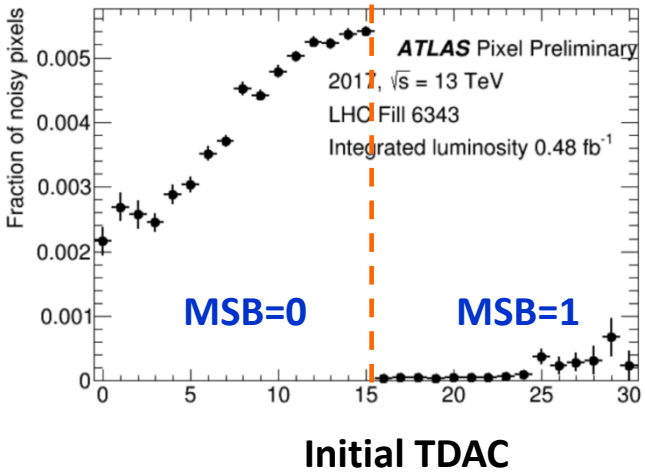
- **The bit-flip of 5-bit threshold DAC (TDAC) decreases the threshold →making pixel noisy.**

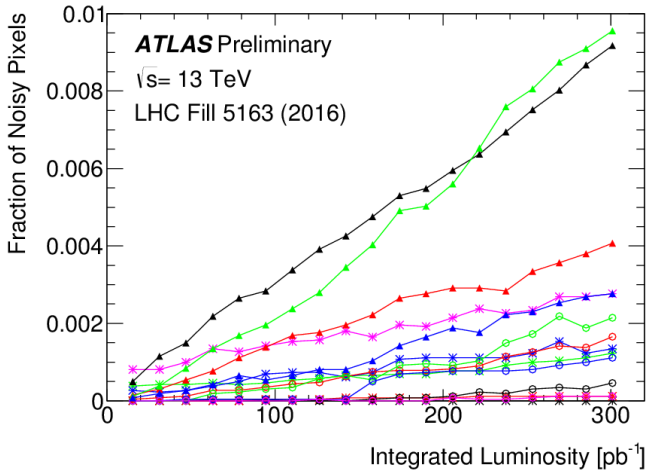
$$< \mathbf{hits} >_{\mathbf{pixel/16pb^{-1}}} = 47$$

Noisy pixel: $< \mathbf{hits} >_{\mathbf{pixel/16pb^{-1}}} > 300$



- **Bit-flip of the most significant bit (MSB) from 0 to 1 is the main cause of noisy pixels.**
  - Pixels with MSB=0 have a larger probability going noisy
  - More pixels go noisy along data taking due to the accumulation of ionizing radiation



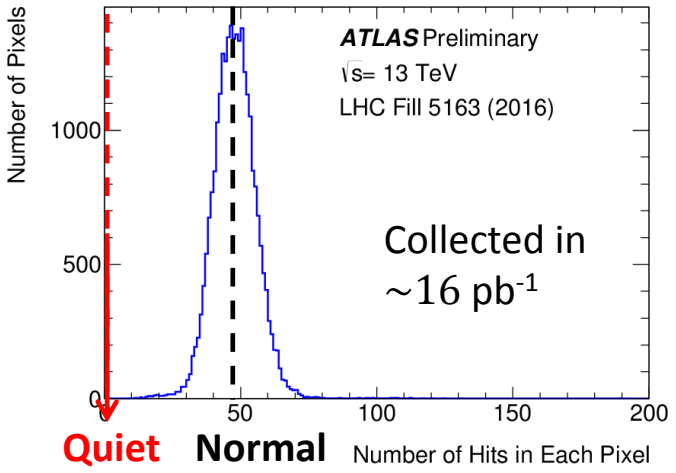


SEEs in Pixel Memory Bits – Quiet Pixels

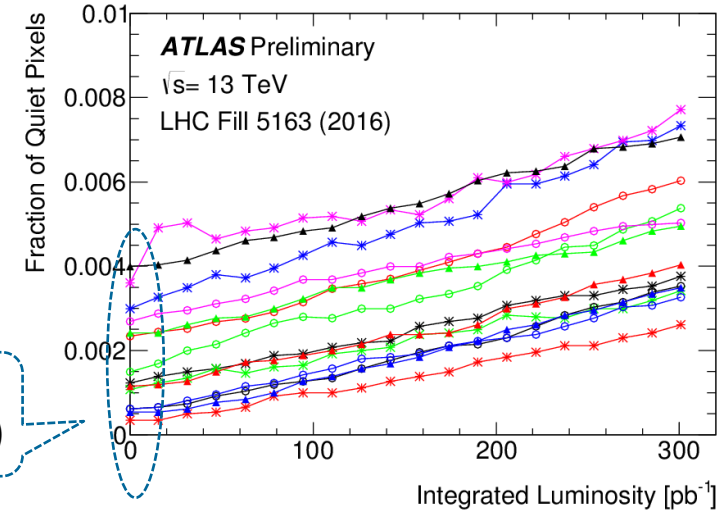
- Most of the pixels ($> 99.5\%$) are enabled at the start of the data taking.
- **1→0 transition of the enable-bit makes a pixel quiet.**

$$< \mathbf{hits} >_{\mathbf{pixel/16pb^{-1}}} = \mathbf{47}$$

Quiet pixel: $< \mathbf{hits} >_{\mathbf{pixel/16pb^{-1}}} = \mathbf{0}$



- **Number of quiet pixels linearly increase with integrated luminosity**
  - Similar behavior of different modules at the same η

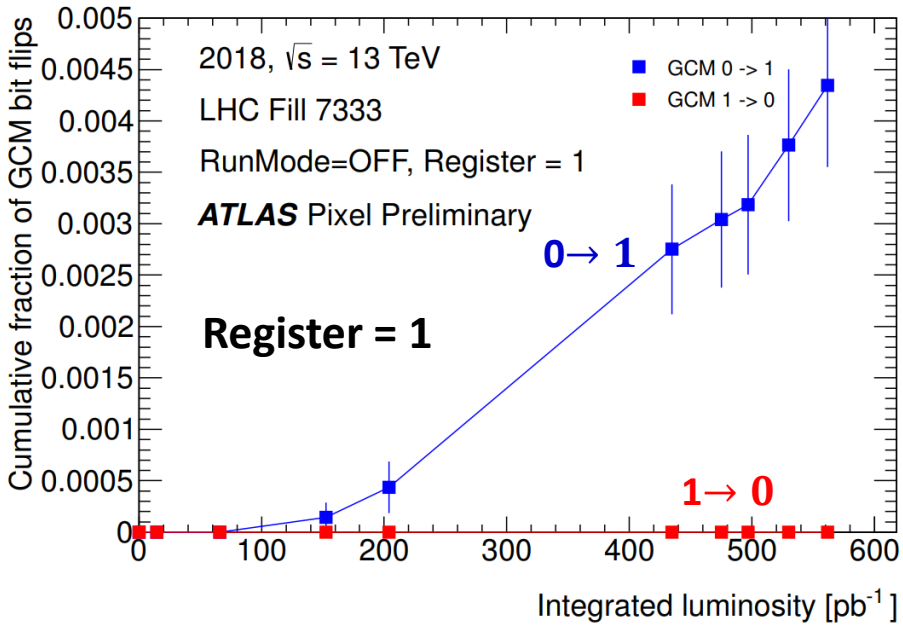


pixels disabled from the start of the data taking (masked, disconnected bumps, digital/analog dead…)

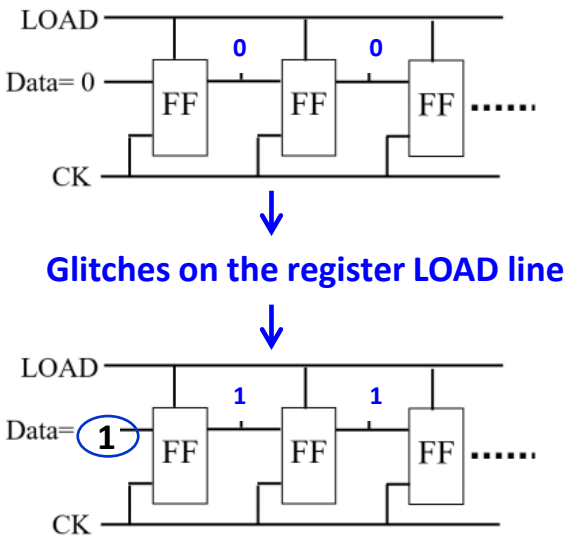
- Single event effects in FE-I4 global and pixel memories
- **Memory bits flip rate measurements**
- Bits recovery strategies and tests
- Conclusions

SEU/SET Rate in Global Memory Bits

- **FE-I4 has a functionality to read back the global and pixel registers.**



- **Fake "LOAD" signals load the register value to the storage element**



- **Register were always "1" during this test, this favors 0→1 transitions.**
- **Low rate 1→0 flips are due to real memory SEU** (triple DICE latches).

SEU/SET Rate in Pixel Memory Bits

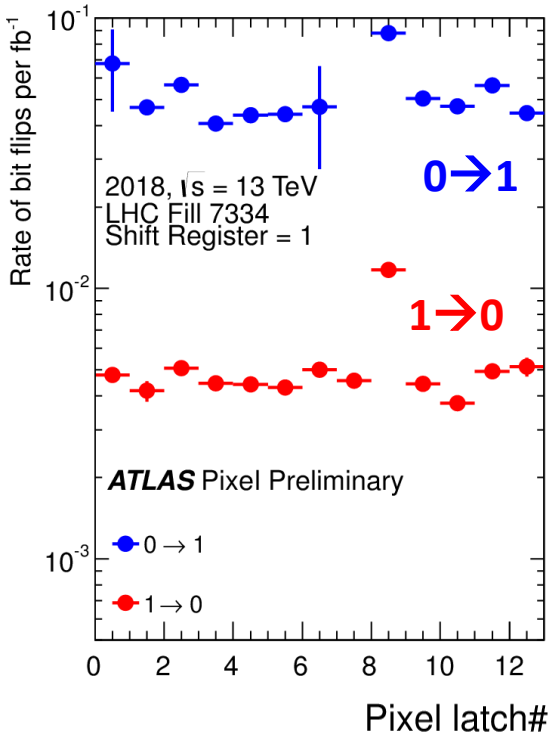
- Memory read-back measures the flips of any one of the 13 configuration bits in each pixel.
- **Average rate of bit flips per fb^{-1}** (from special test fill)

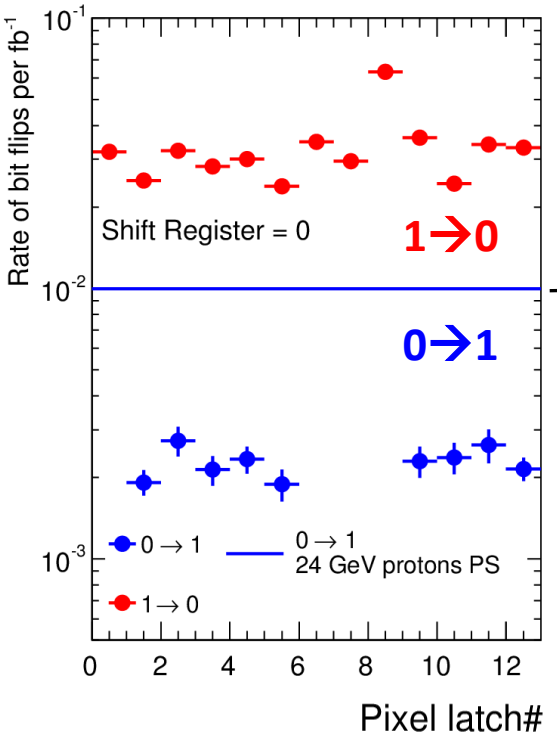
Shift Register = 1

Shift Register = 0

Glitches on the SR "LOAD" line

Real memory SEU



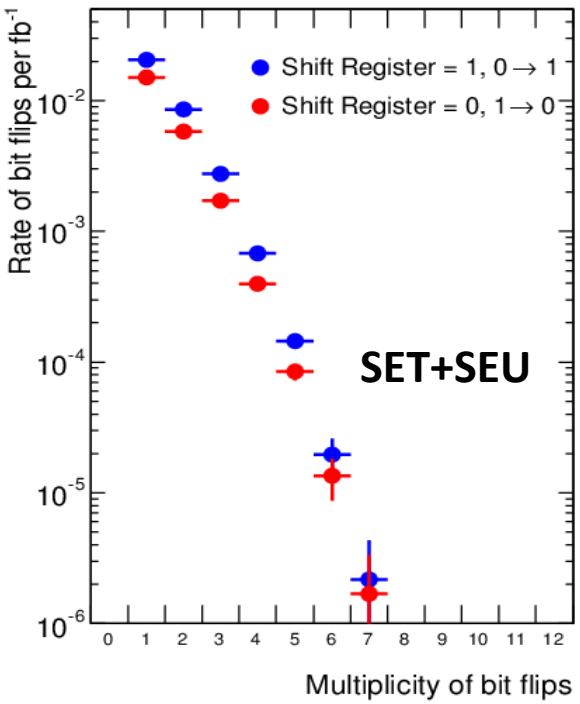


→ **0→1 from beam testing** (shift registers are not refreshed)

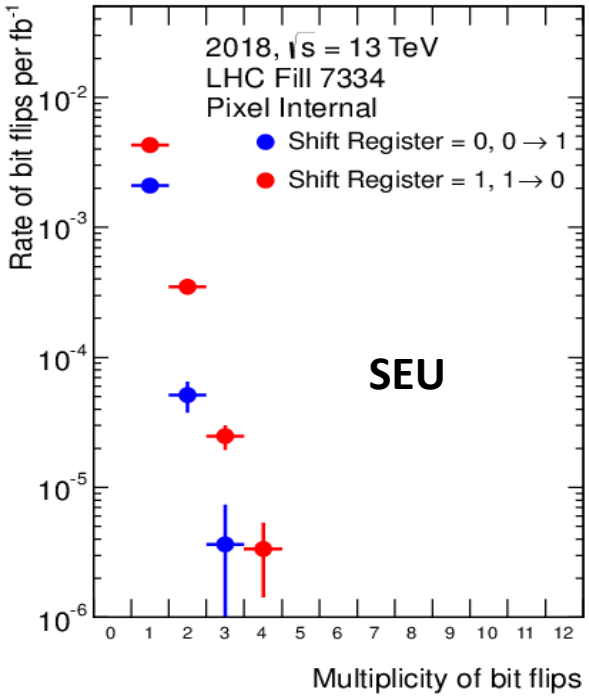
Rate of multiple bit flips

- SETs in the LOAD line of the DICE latch dominate the memory bit flips.
- **Multiple bit flips in one pixel is a sign of glitch on the common LOAD line**

- **SR opposite to the memory content**



- **SR same as the memory content**

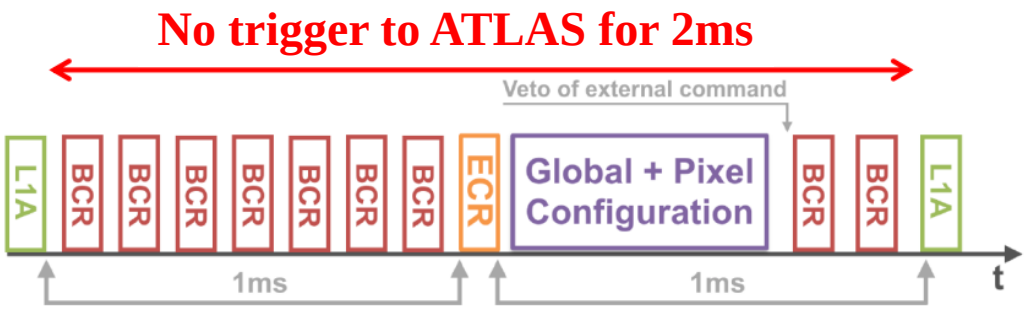


- Peak at one bit flip per pixel → **glitch on the LOAD line mainly related to individual latch**
- Different 0→1 and 1→0 rates due to the use of **different chips on slightly different locations**

- Single event effects in FE-I4 global and pixel memories
- Memory bit flips rate measurements
- **Bits recovery strategies and tests**
- Conclusions

Recovery of the bits flipped by SEEs

- Every 5s, the ATLAS central trigger processor sends an Event Counter Reset signal (ECR) inside a 2ms window w/o triggers, to re-synchronize the entire readout chain.



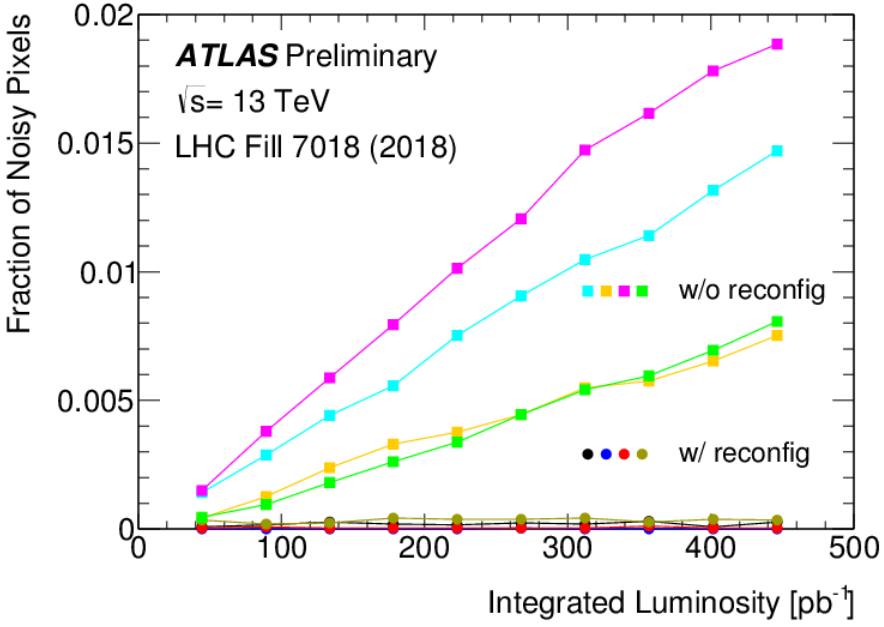
Reconfiguration performed inside 1ms out of 2ms ECR window → NO extra busy time

- **Global registers of all IBL chips reconfigured every 5s since August 2017.**
- **Pixel registers of all IBL chips reconfigured every 11 minutes (Not applied yet, but tested in one fill in 2018)**
  - There is not enough time in one ECR window to reconfigure all pixel registers.
  - **3 memory bits of one double column inside each ECR window.**

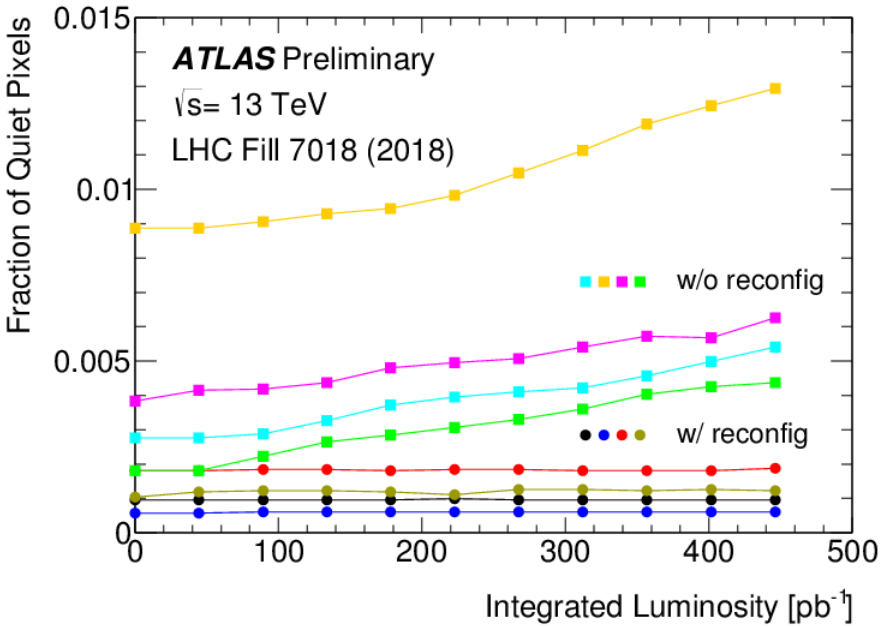
Testing the recovery of the bits flipped by SEEs

- The automatic pixel reconfiguration has been tested in fill 7018
- **Only 4 chip rings are reconfigured, the others are not and used as reference.**

Fraction of noisy pixels



Fraction of quiet pixels



- **More pixels go to noisy or quiet along data taking due to SEEs in modules w/o reconfiguration.**
- **In modules reconfigured every 11 minutes, the fraction of noisy or quiet pixels is more stable.**

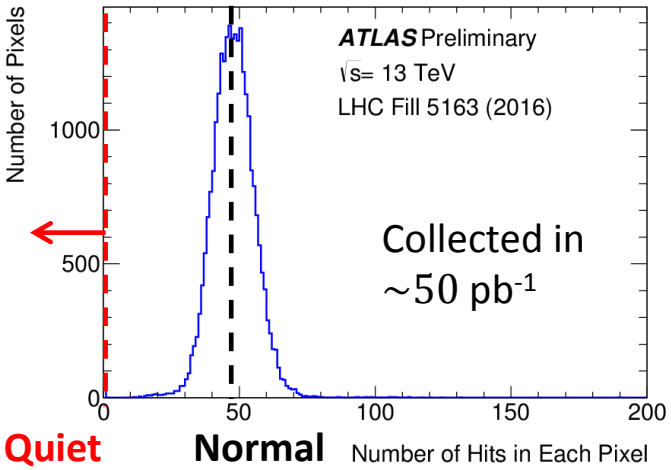
Conclusions

- Both global and pixel registers of FE-I4 chips are affected by SEU/SET
- The bit flip rate has been measured with various strategies.
- Pixel memory read-back results confirms that **the bit flips are dominated by SET** that create fake “LOAD” signals.
- The bit-flip multiplicity study indicates that **the glitch on the LOAD line is mainly related to single DICE latch**
- **Bits recovery strategy has been verified and will be fully deployed in Run3**

An ATLAS Pixel Paper is being prepared.


Thank You!

How to identify quiet/noisy pixels?



Noisy

- *Occupancy of each pixel in the first 16 pb^{-1} data in one 3D module*
- *Only clusters the length of which along z is one pixel are used due to the lack of the pixels information of other clusters.*
- *The average occupancy of one pixel in 16 pb^{-1} data of this fill is about 50.*

Noisy pixels

- *The probability of a normal pixel firing more than 300 times in 16 pb^{-1} data is* 3.1×10^{-127}.

Quiet pixels

- *The probability of a normal pixel never firing in 16 pb^{-1} data is* 1.9×10^{-22}.

Puzzling noisy pixels

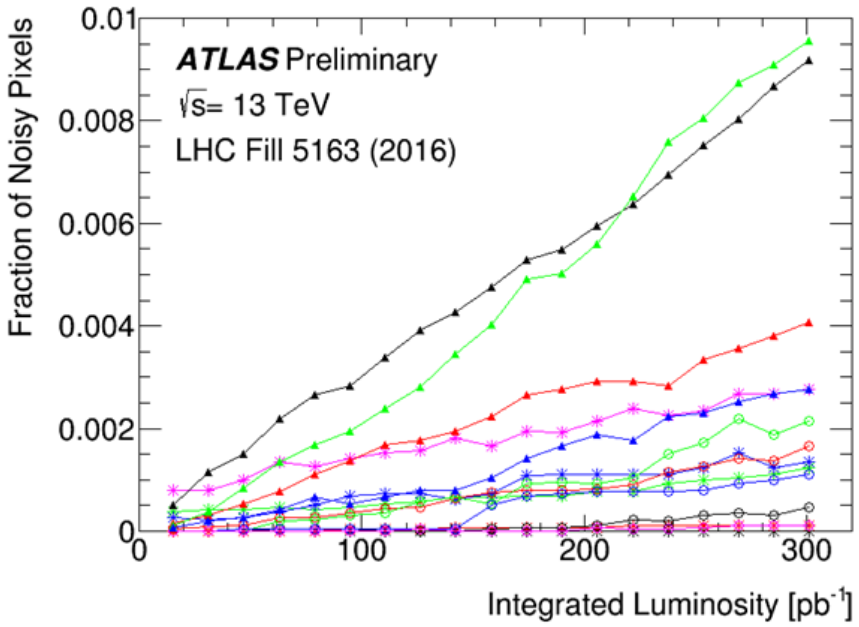
Threshold in each pixel

$$= f(\text{VthinAlt\_Coarse}) + f(\text{VthinAlt\_Fine}) + f(\text{TDAC}*\text{TdacVbp})$$

two 8-bit global registers for adjustment of global threshold

5-bit pixel register

8-bit global register sets the step size of TDAC

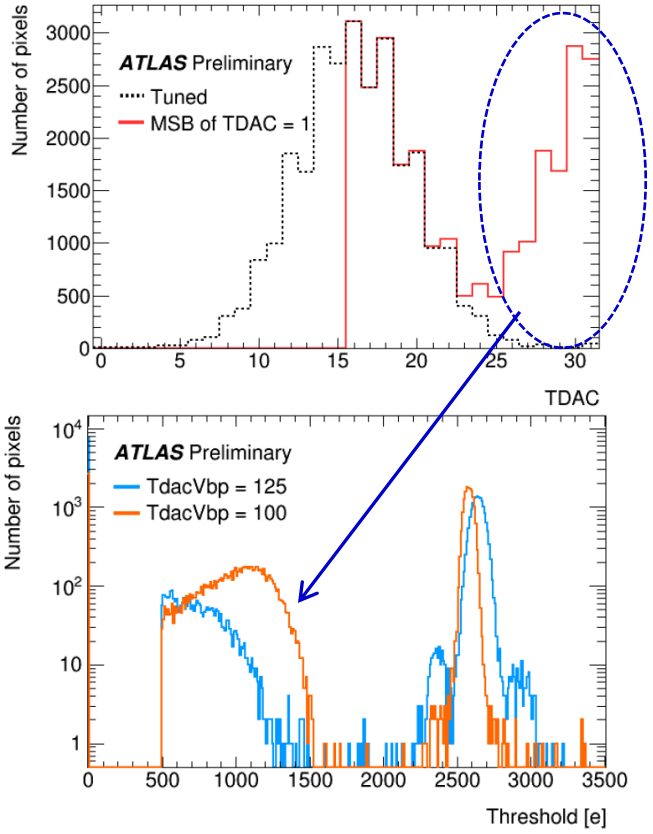


Confirmed: The noisy pixels are due to threshold decrease caused by the 0→1 bit-flip of TDAC.

Mimic of an SEU on the 1st bit of TDAC

- An individual FE−I4 chip tuned with a target threshold of 2500e

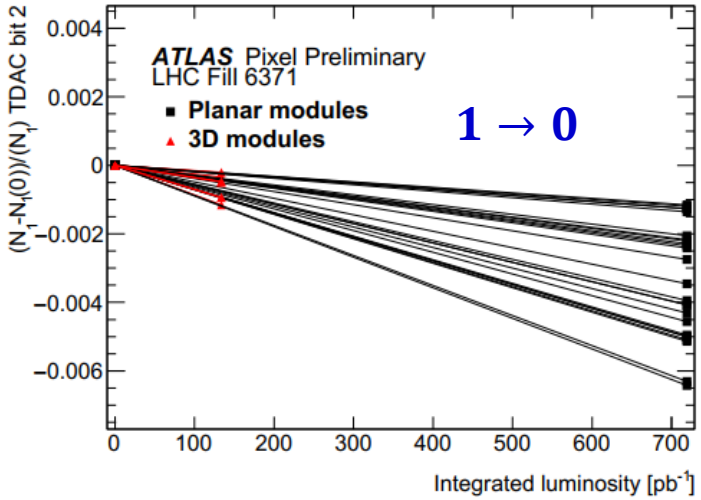
1st bit 0→1 transition lowers the pixel threshold



Read back of pixel memory

- **FE-I4 has a functionality to read back the pixel memory.**
- **Read-back cannot be performed while a FE receives triggers**. → only 2 read-backs for planar modules
  - The intermediate point is from 3D modules which are not taking data.
- **Fraction of pixels in which bit state flip depends on SEU cross section and luminosity**

$$\frac{N_1(0) - N_1}{N_1} = \sigma_{1\to0} \cdot \mathcal{L}$$



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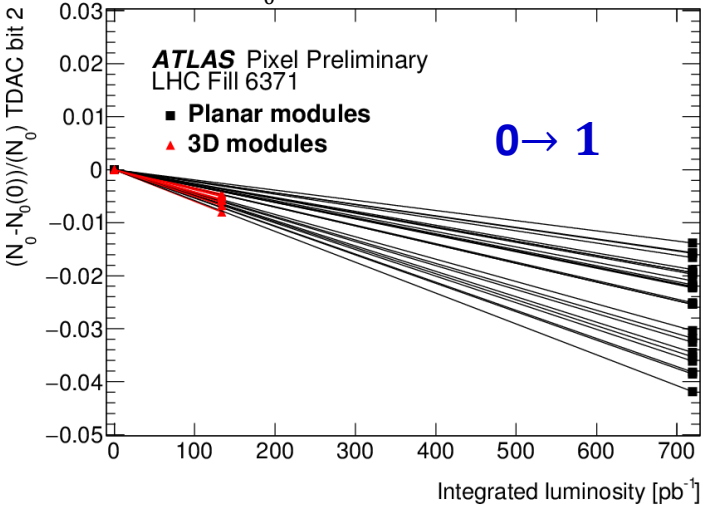
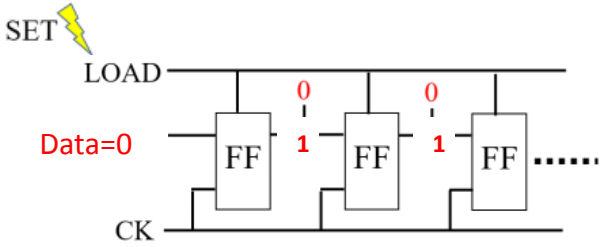
$$\frac{N_0(0) - N_0}{N_0} = \sigma_{0\to1} \cdot \mathcal{L}$$



- **0→1 is much larger than 1→0** : **glitches on the SR "LOAD" line**
- The polarity of the transition depends on the actual values stored in SR. The last bit (out of 13 bits) loaded into SR is the output enable bit.
- As the enable bit is usually 1, this favors 0→1 transitions.



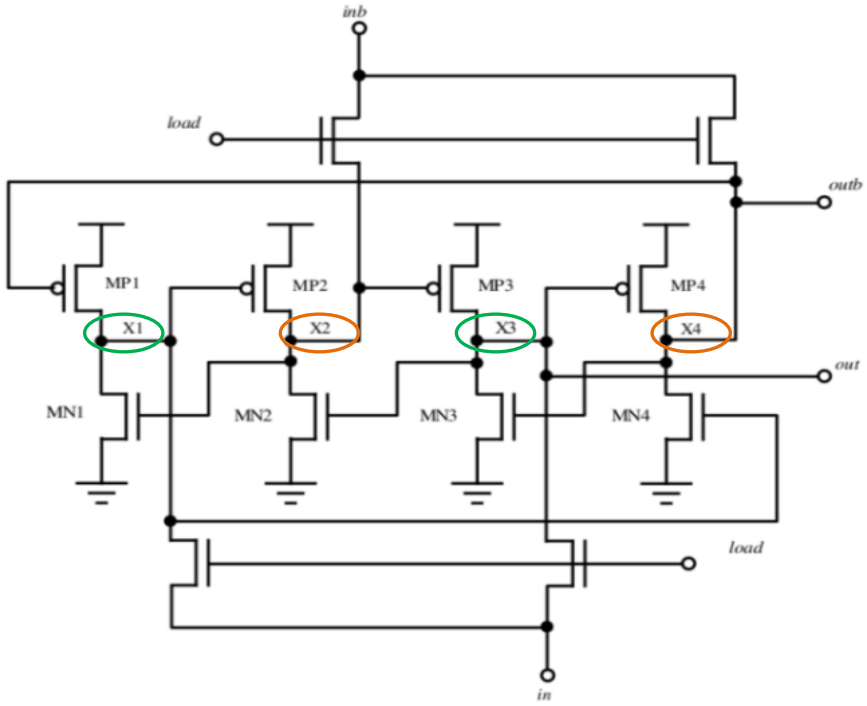
Dual Interlocked CEll

The threshold energy deposition for producing SEUs (at *Ipin* = 100 µA) is 2.3 MeV.

two orders of magnitude higher than

The energy deposited in the depleted depth of the *p-i-n* diode by a minimum ionizing particle (MIP) at normal incidence is 6 keV.

- 4 nodes storing data as 2 pairs of complementary values.
- Assume a positive upset pulse on the node X1 → MP2 is blocked & MN4 will propagate a negative pulse to X4 blocking MN3 → Nodes X2 and X3 have conserved the true information



Enable bit flips

Conventional method: **Beam testing @2012**

- Before the installation of IBL
- 1st measurement of SEU in FE-I4 using 24 GeV proton beam @CERN

$$\sigma_{SEU} = \frac{N_{firing-pixels}}{\Phi \cdot N_{all-pixels}} = 1.1 \cdot 10^{-15} cm^2$$

For the LHC data taking period corresponding to 1 fb^{-1} the predicted flow of hadrons with energy above 20 MeV with PYTHIA/FLUKA simulations in the extreme outside 3D sensor IBL module is $\Phi = 0.91 \times 10^{13}$ hadrons (T>20 MeV) cm^{-2} [9]. The SEU cross section is calculated to be $1.1–2.2 \times 10^{-15} cm^2$. This is at the same order of magnitude as the test beam result.

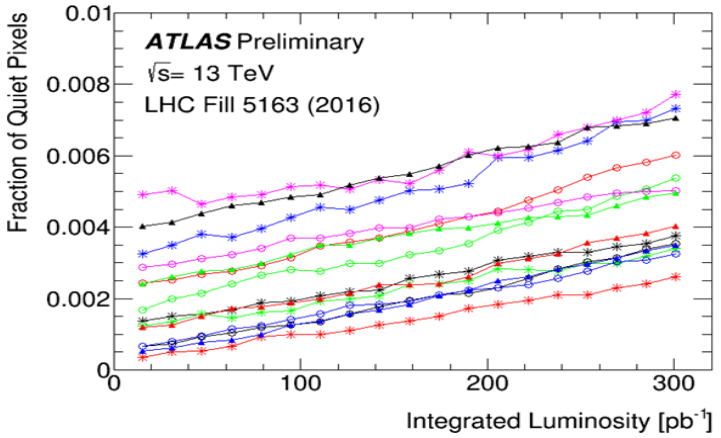
Developed new method analyzing cluster data

- **1→0 transition of the enable bit makes a pixel quiet.**

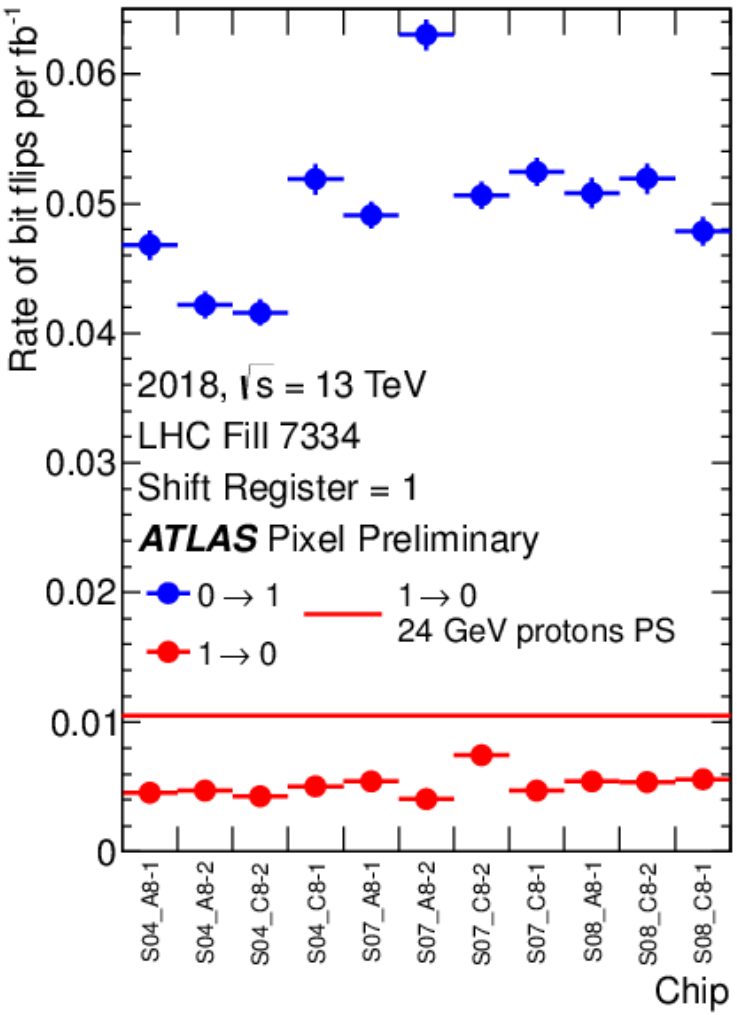
$$\sigma_{SEU} = \frac{N_{errors}}{\Phi \cdot N_{latches}} = \frac{p_1 \cdot \mathcal{L}}{\Phi} = 0.6 \sim 1.2 \cdot 10^{-15} cm^2$$

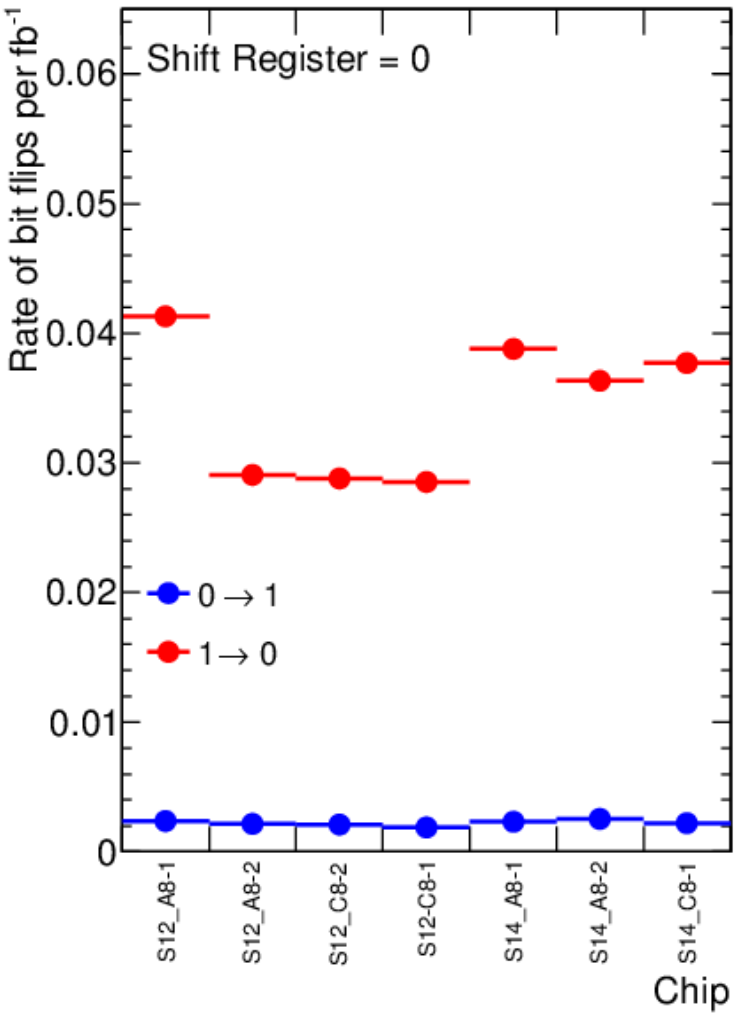
(consistent with beam testing result)

- **The only method which could measure SEU rate in operation**



Pixels masked before data taking

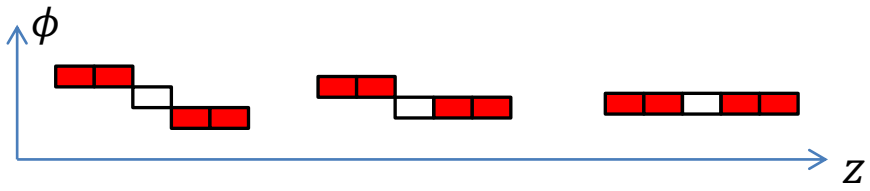

Rate of bit flips per fb^{-1}
0.06
0.05
0.04
0.03
0.02
0.01
0
2018, $\sqrt{s}$ = 13 TeV
LHC Fill 7334
Shift Register = 1
ATLAS Pixel Preliminary
0 → 1
1 → 0
1 → 0
24 GeV protons PS
S04_A8-1
S04_A8-2
S04_C8-2
S04_C8-1
S07_A8-1
S07_A8-2
S07_C8-2
S07_C8-1
S08_A8-1
S08_C8-2
S08_C8-1
Chip


Rate of bit flips per fb^{-1}
0.06
0.05
0.04
0.03
0.02
0.01
0
Shift Register = 0
0 → 1
1 → 0
S12_A8-1
S12_A8-2
S12_C8-2
S12-C8-1
S14_A8-1
S14_A8-2
S14_C8-1
Chip

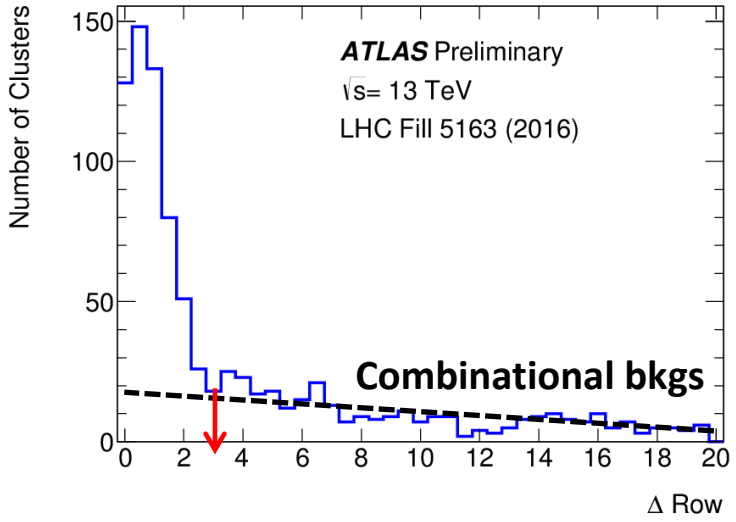
SEEs in pixel memory bits – Broken clusters

- **The quiet pixels cause clusters broken.**

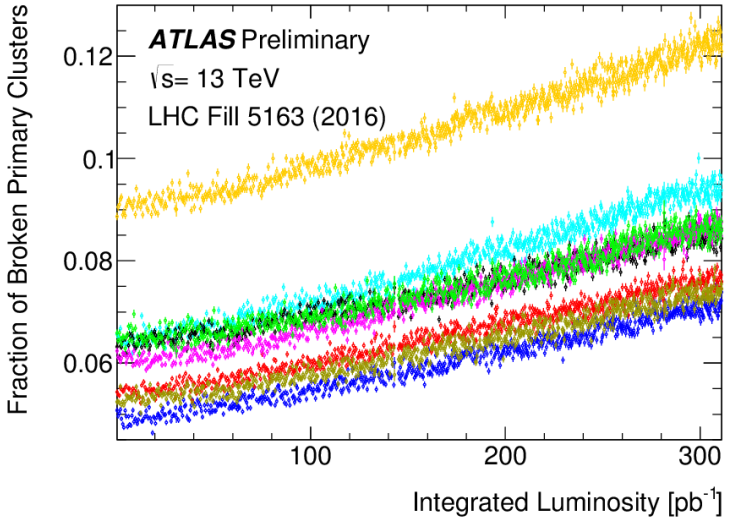
Broken clusters: two clusters with 1-pixel gap along z direction and Δrow ≤3



Δrow = center-to-center cluster distance along the azimuthal direction

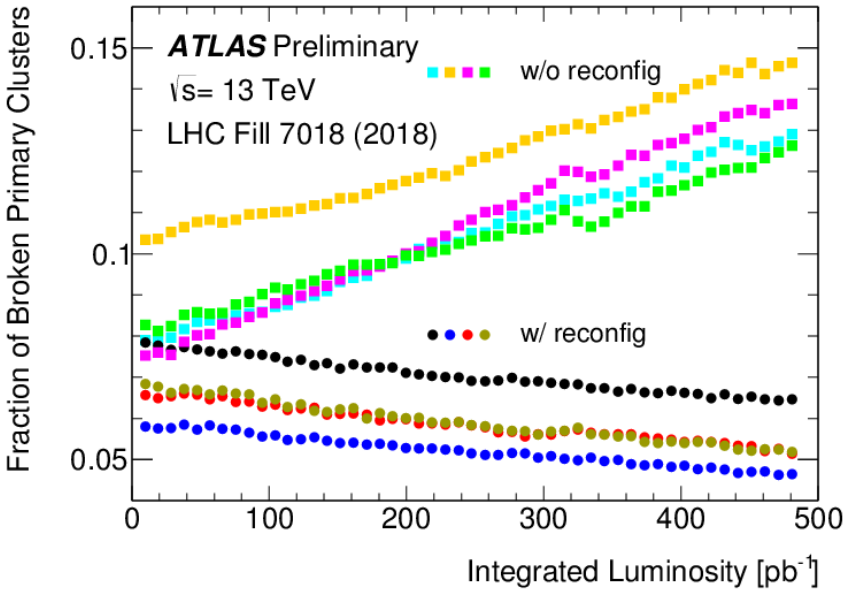


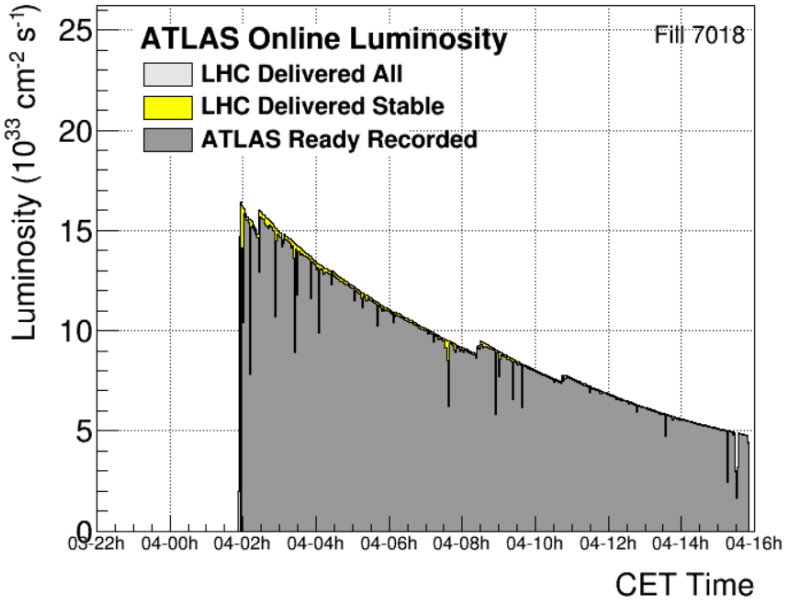
- **More broken clusters (more quiet pixels) along data taking due to the accumulation of ionizing radiation.**



Testing the recovery of the bits flipped by SEEs (2)

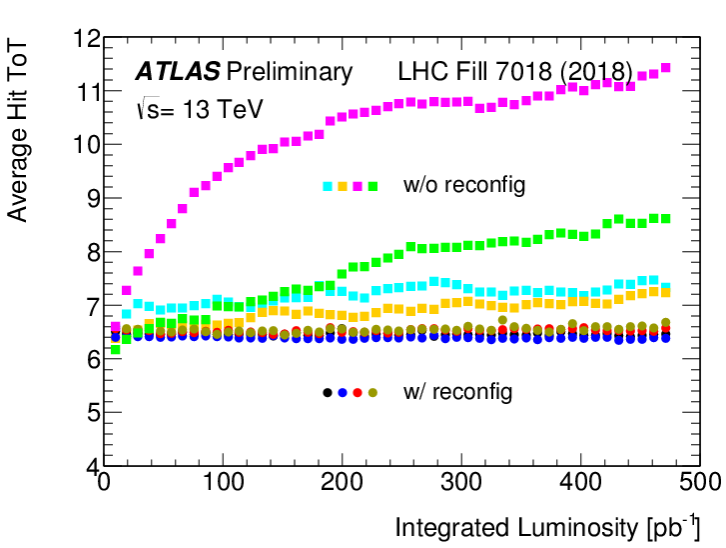
- **Fraction of broken clusters**
  - **Modules w/o (w/) reconfiguration show increase (decrease) of broken clusters**
  - More reconfigurations happened in bins where the instant luminosity is lower (More time is needed to take the same amount of luminosity)



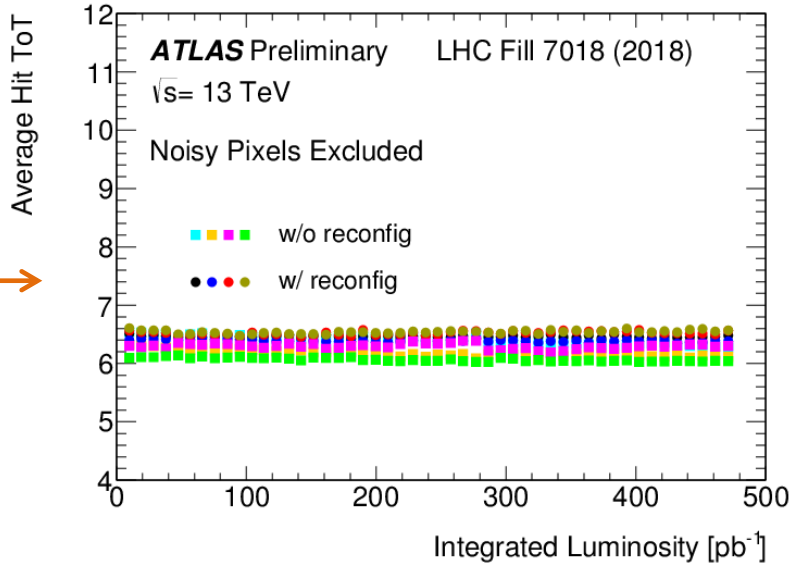


Testing the recovery of the bits flipped by SEEs (3)

- **Time over Threshold (ToT)** of the pixel hits
  - The average hit ToT increases in modules w/o reconfiguration because more pixels go noisy.



Noisy pixels excluded



- **The effect of the ToT increase is almost fully correlated with noisy pixels caused by SEU in TDAC MSB, NOT with detuning of pixel due to SEU in FDAC**

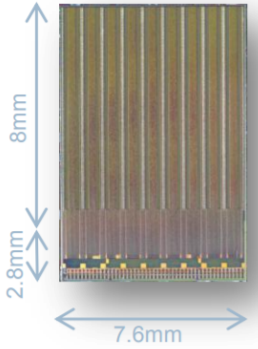
Beam, SEE type	Transition	SR value	Rate per fb^{-1} [%] (stat./syst.)	Cross-section 10^{-15} cm^2
LHC: mainly SEU	$0 \rightarrow 1$	0	$0.22 \pm 0.01 \pm 0.09$	0.24 ± 0.13
LHC: mainly SEU	$1 \rightarrow 0$	1	$0.46 \pm 0.01 \pm 0.19$	0.51 ± 0.26
LHC: mainly SET on LOAD line	$1 \rightarrow 0$	0	$3.07 \pm 0.02 \pm 0.80$	3.39 ± 1.34
LHC: mainly SET on LOAD line	$0 \rightarrow 1$	1	$4.68 \pm 0.03 \pm 1.21$	5.16 ± 2.04
24 GeV protons Mostly SEU with some SET admixture	$0 \rightarrow 1$	0	n.a.	1.10

Table 1: Summary of measured rates and SEE cross sections.

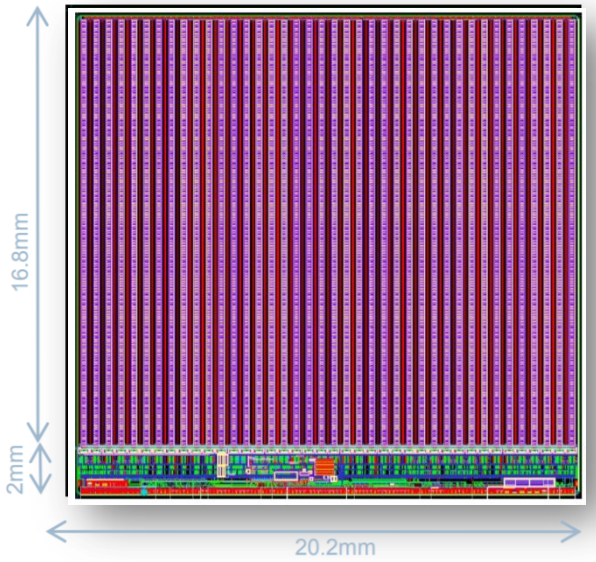
FE-I4 read out chip

FE-I3

- **Used in other pixel layers**



- Digital processing is in periphery area



FE-I4

- **New digital architecture**
  - **Local "in-pixel" storage**
- Most digital processing is in the pixel matrix
- **Allows for high hit rate and smaller periphery area**

Generation	FE-I3	FE-I4	
Feature Size [nm]	250	130	More radiation tolerant
Pixel Size [μm^2]	50×400	50×250	40% smaller pixel size
Pixel Array	18×160	80×336	
Chip Size [mm^2]	7.6×10.8	20.2×19.0	Bigger chip size
Active Fraction	74%	89%	
Output Data Rate [Mb/s]	40	160	Higher data rate