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OT-µDTC, a test bench for testing CMS Outer Tracker Phase-2 module prototypes

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The CMS Phase-2 Outer Tracker (OT) will be built by using two types of modules (strip-strip modules and pixel-strip modules) both consisting of two silicon sensors with a few millimeter separation. To read out the two types of modules four OT specific custom made chips are required: CBC (CMS Binary Chip [1]), SSA (Short Strip ASIC [2]), MPA (Macro Pixel ASIC [3]) and CIC (Concentrator Integrated Circuit [4]). The CBC and MPA (with SSA input) chips perform a spatial correlation between the hits on the top and bottom sensor to provide data ('stubs') on particles with high transverse momentum. This stub data is sent to CIC, which selects stubs with high transverse momentum. The output stub data from CIC is sent at bunch-crossing rate and the data will be used in the L1 trigger system of CMS. On a reception of a trigger the front-end chips respond by outputting the full event information. A module will thus provide two types of data: synchronous stub data and asynchronous full event data.

All these ASICs need to be qualified; first on stand-alone single-chip carriers, and then on prototype read-out hybrid circuits equipped with different types of ASICs operating together. A firmware project, so called µDTC, was set-up to handle these data streams using a µTCA compatible Advanced Mezzanine Card for generic data acquisition/control applications (the FC7).

This poster will describe the data path of the outer tracker modules, give an overview of the available prototypes, and explain the structure of the firmware framework. Finally, results obtained using this test bench during test beams and lab tests will be presented.

[1] Cussans et al., "Tests with the CMS Binary Chip (CBC)", 2012 JINST 7 C03016 [2] Caratelli et al., "Short-Strip ASIC (SSA): A 65nm Silicon-Strip Readout ASIC for the Pixel-Strip (PS) Module of the CMS Outer Tracker Detector Upgrade at HL-LHC", PoS(TWEPP-17)031 [3] Ceresa et al., "Design and simulation of a 65 nm Macro-Pixel Readout ASIC (MPA) for the Pixel-Strip (PS) Module of the CMS Outer Tracker Detector at the HL-LHC", PoS(TWEPP-17)032 [4] Scarfi et al., "A System-Verilog Verification Environment for the CIC Data Concentrator ASIC of the CMS Outer Tracker Phase II Upgrades", PoS(TWEPP2018)097

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