

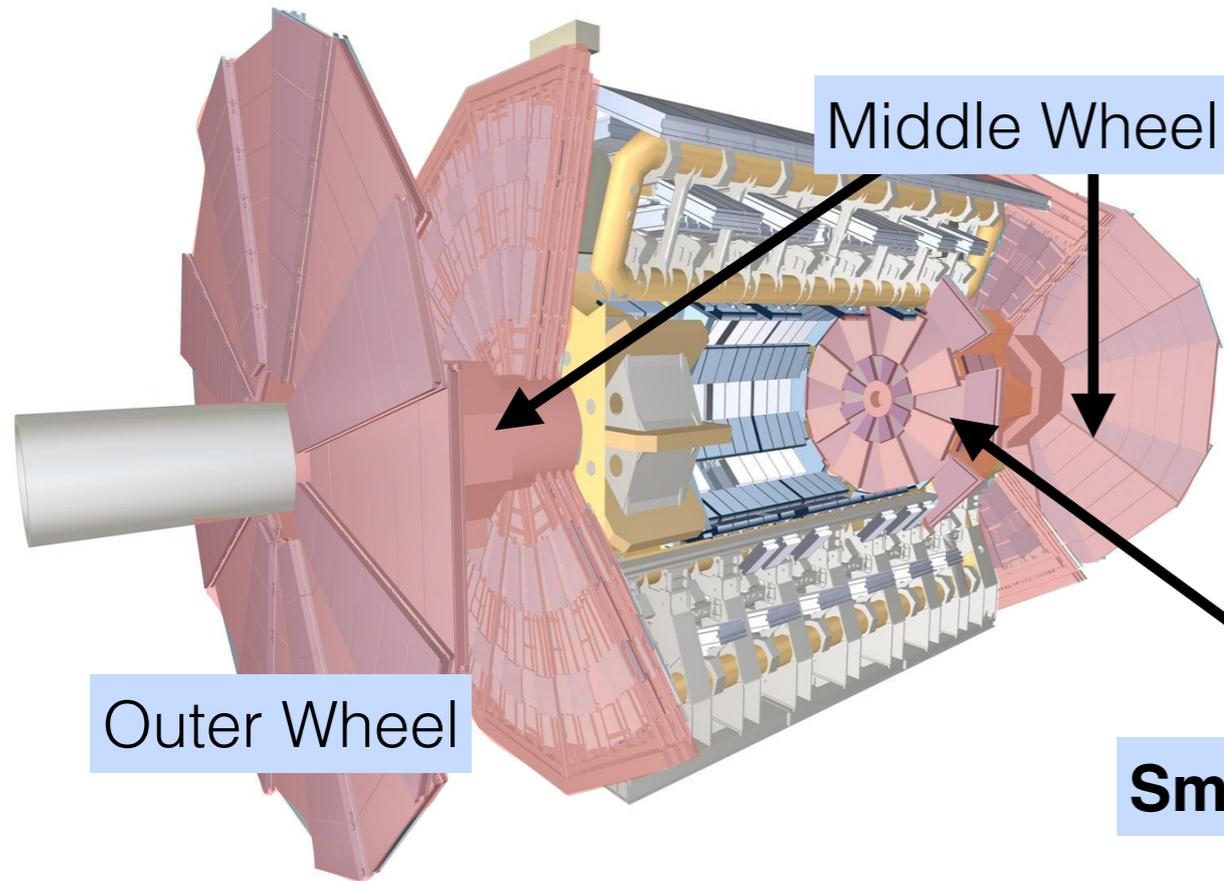
FRONTEND AND BACKEND
ELECTRONICS FOR THE
ATLAS NEW SMALL WHEEL
UPGRADE

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HARVARD UNIVERSITY

EPS-HEP 2019

ON BEHALF OF THE ATLAS MUON COLLABORATION

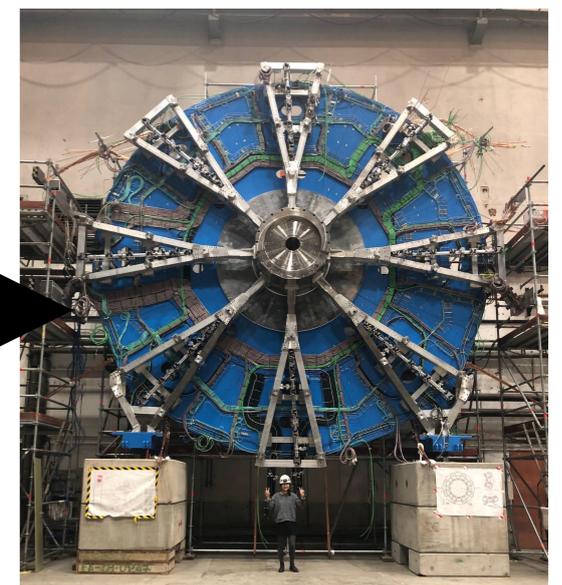
UPGRADING THE ATLAS MUON DETECTOR



- The High Luminosity Large Hadron Collider will have 2-4x larger peak instantaneous luminosity compared to LHC Run 2
- Run 3 will have a factor of $\sim 1.5x$ increase in instantaneous luminosity

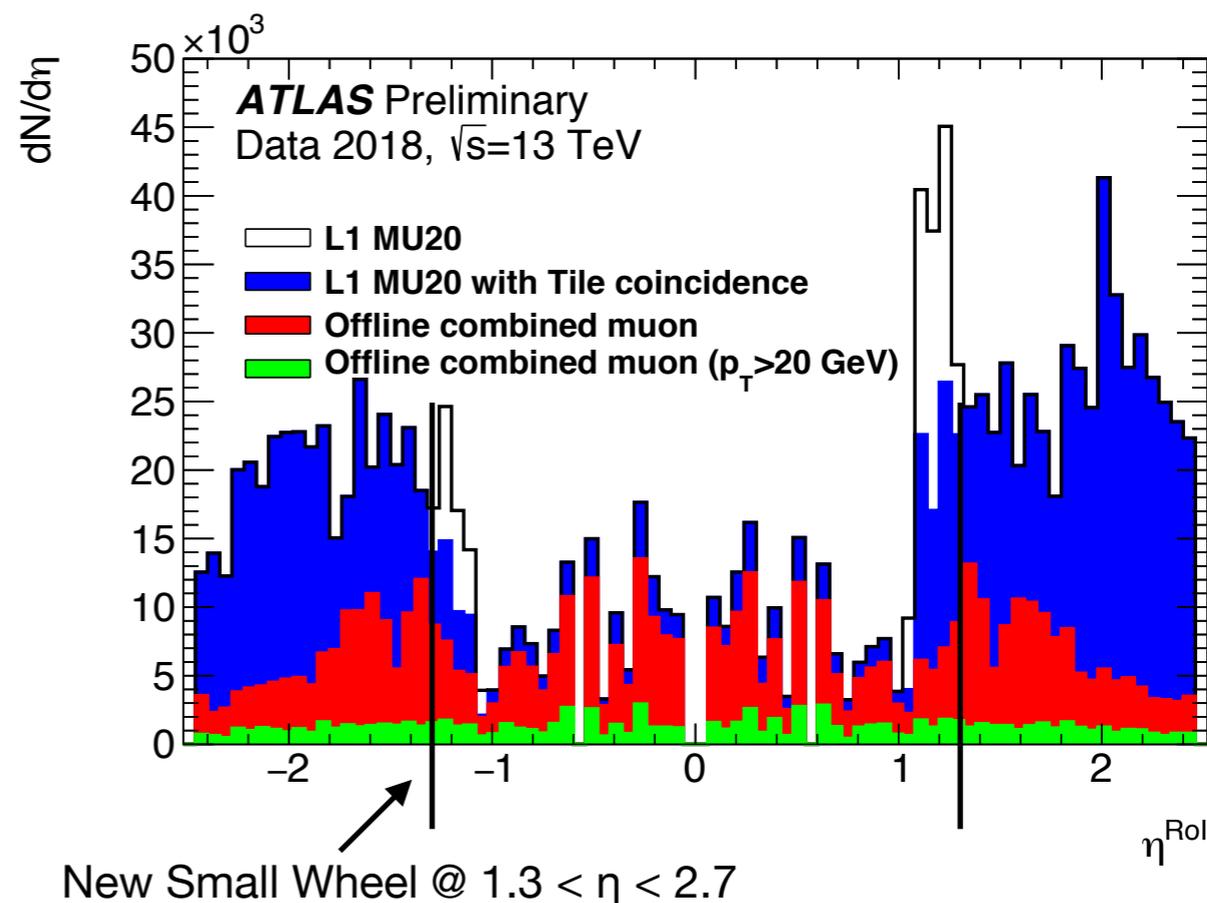
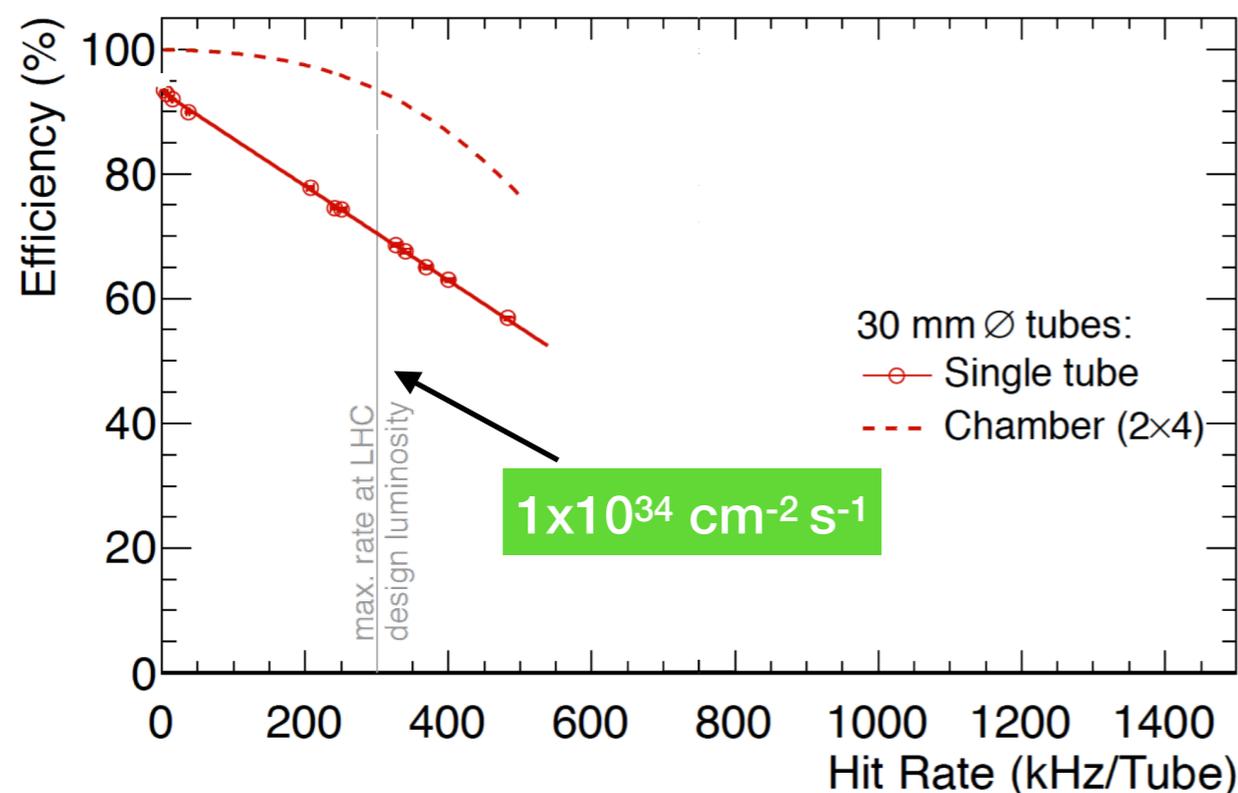
- The **New Small Wheel (NSW)** upgrade will replace the Small Wheel of the current ATLAS Muon Spectrometer to handle large particle rates
- Important for Run 3, vital for HL-LHC

Small Wheel



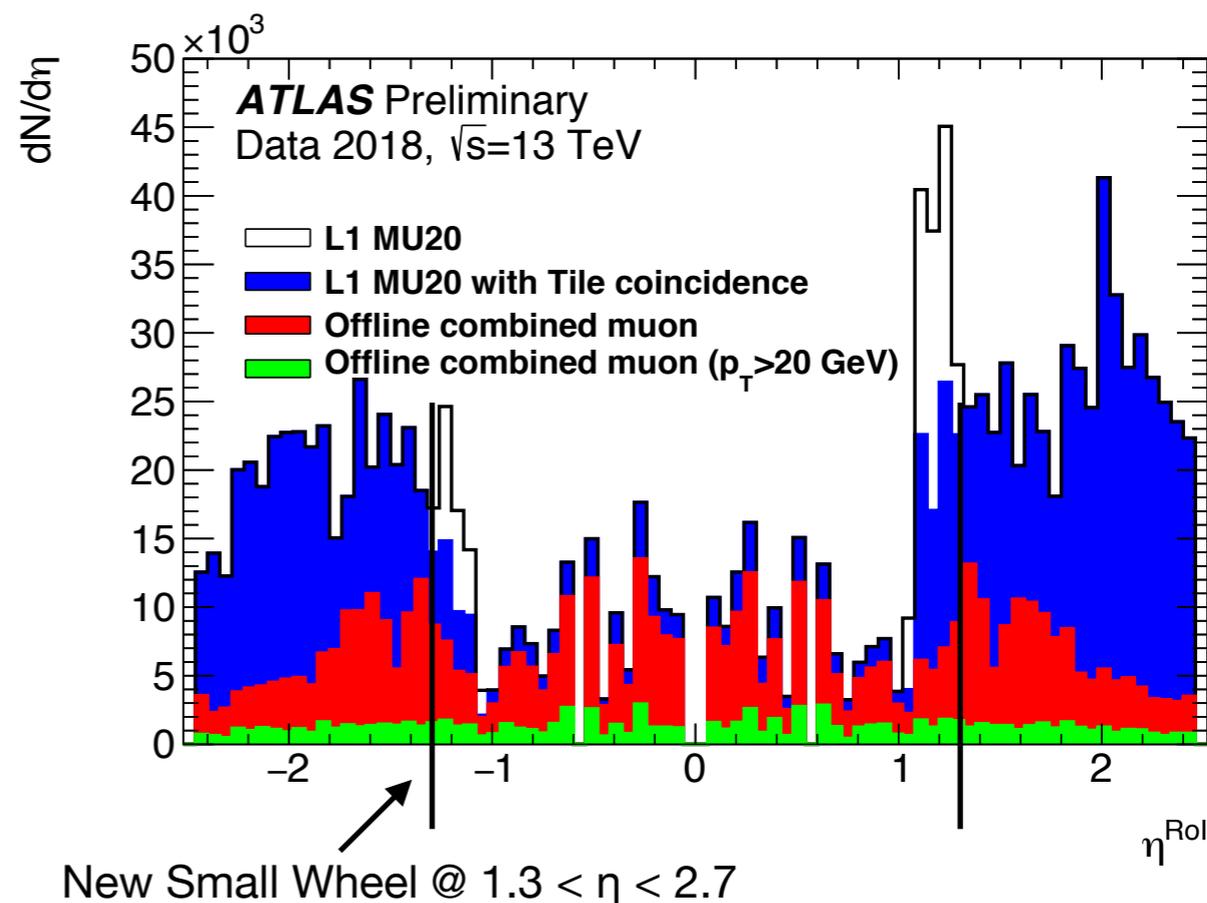
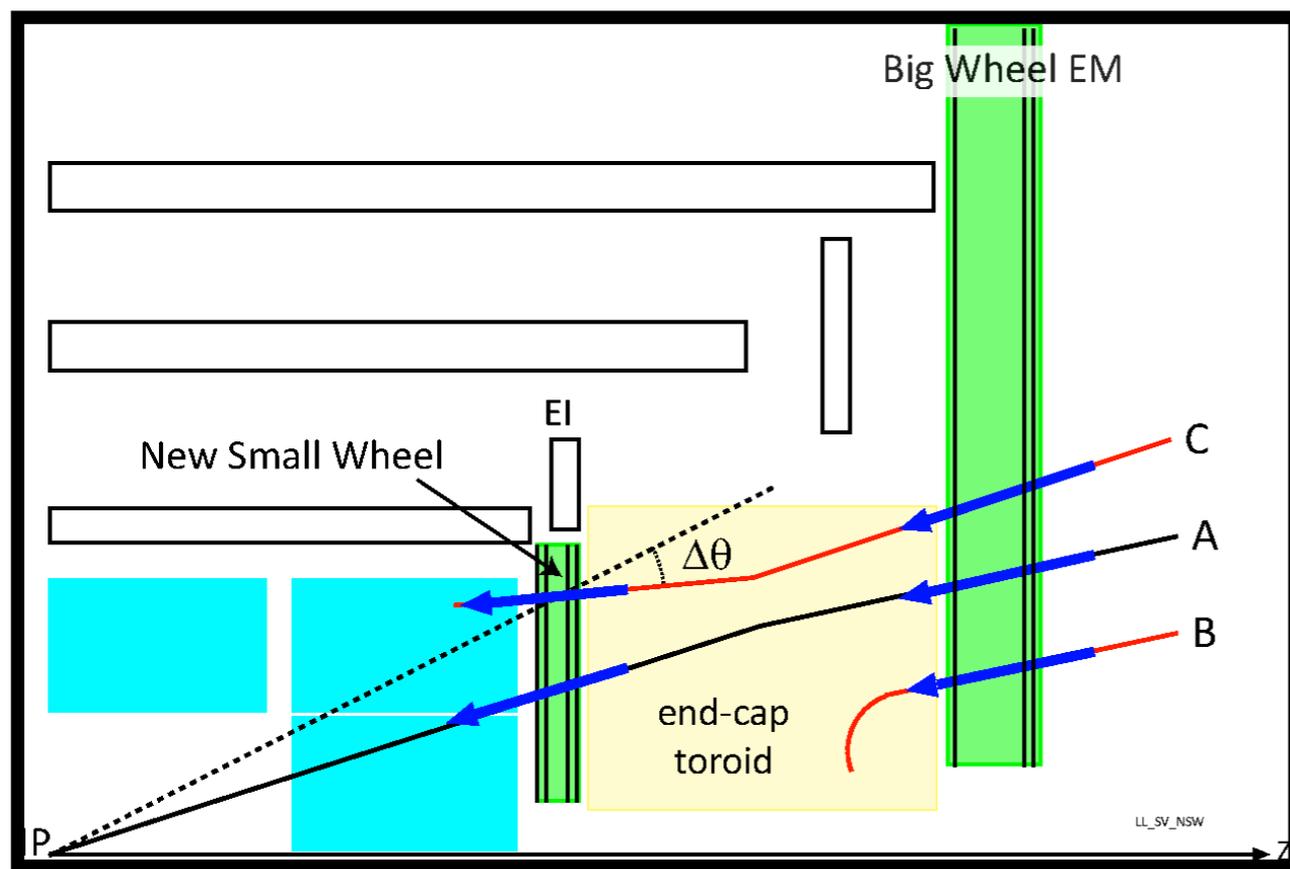
New Small Wheel mechanical structure

WHY DO WE NEED AN UPGRADE?



- **Tracking:** Monitored Drift Tubes will lose efficiency at high hit rates due to higher instantaneous luminosity
- **Triggering:** Lowest unprescaled muon trigger is dominated by fake muons in the endcap region

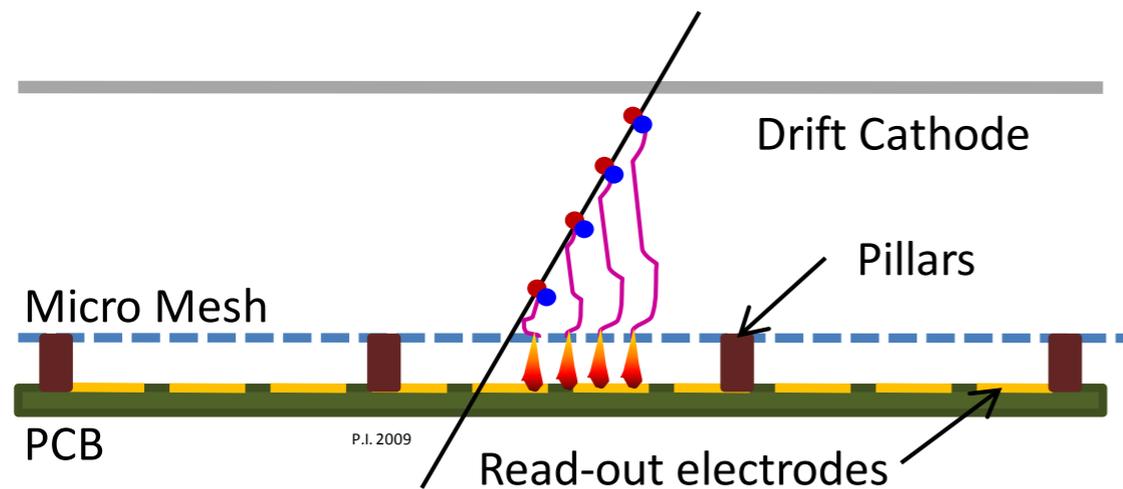
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NEW SMALL WHEEL UPGRADE

Micromegas (MM) detector

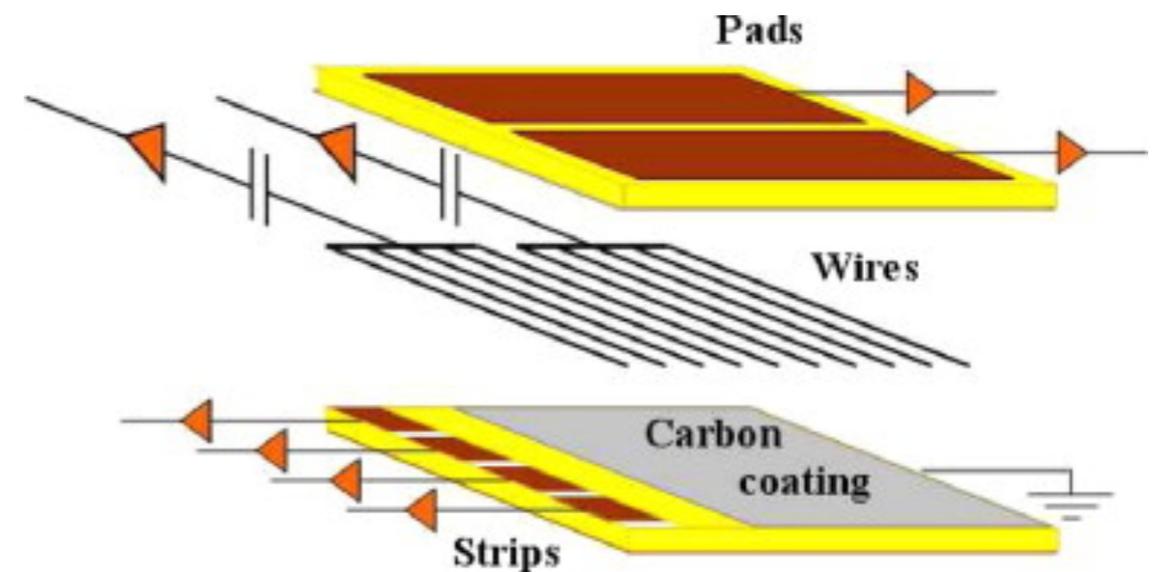


- **Precision tracking**

- **small strip pitch** (~425-450 microns compared to current 3 cm drift tube)
- **short drift time** (~100 ns compared to ~750 ns for drift tubes)
- fine pitch and fast drift time allow MM to handle high particle rates

also provides a trigger signal!

small strip Thin Gap Chambers (sTGC)



- **Fast triggering**

- **small strip pitch** (3.2 mm) compared to TGC wire groups (~10-50 mm) —> ~ 2 mrad trigger track resolution
- **high efficiency** under tests with γ irradiation of 20 kHz/cm²
- will **reduce** the Level 1 lowest unprescaled **muon trigger rate** by > ~ 7x

also used in tracking!

NEW SMALL WHEEL ELECTRONICS

- A combination of custom **frontend** and **backend** boards + chips are needed!
- Need to handle the MM and sTGC readout and trigger paths

Micromegas
Frontend Board



Address in Real Time
Data Driver Card

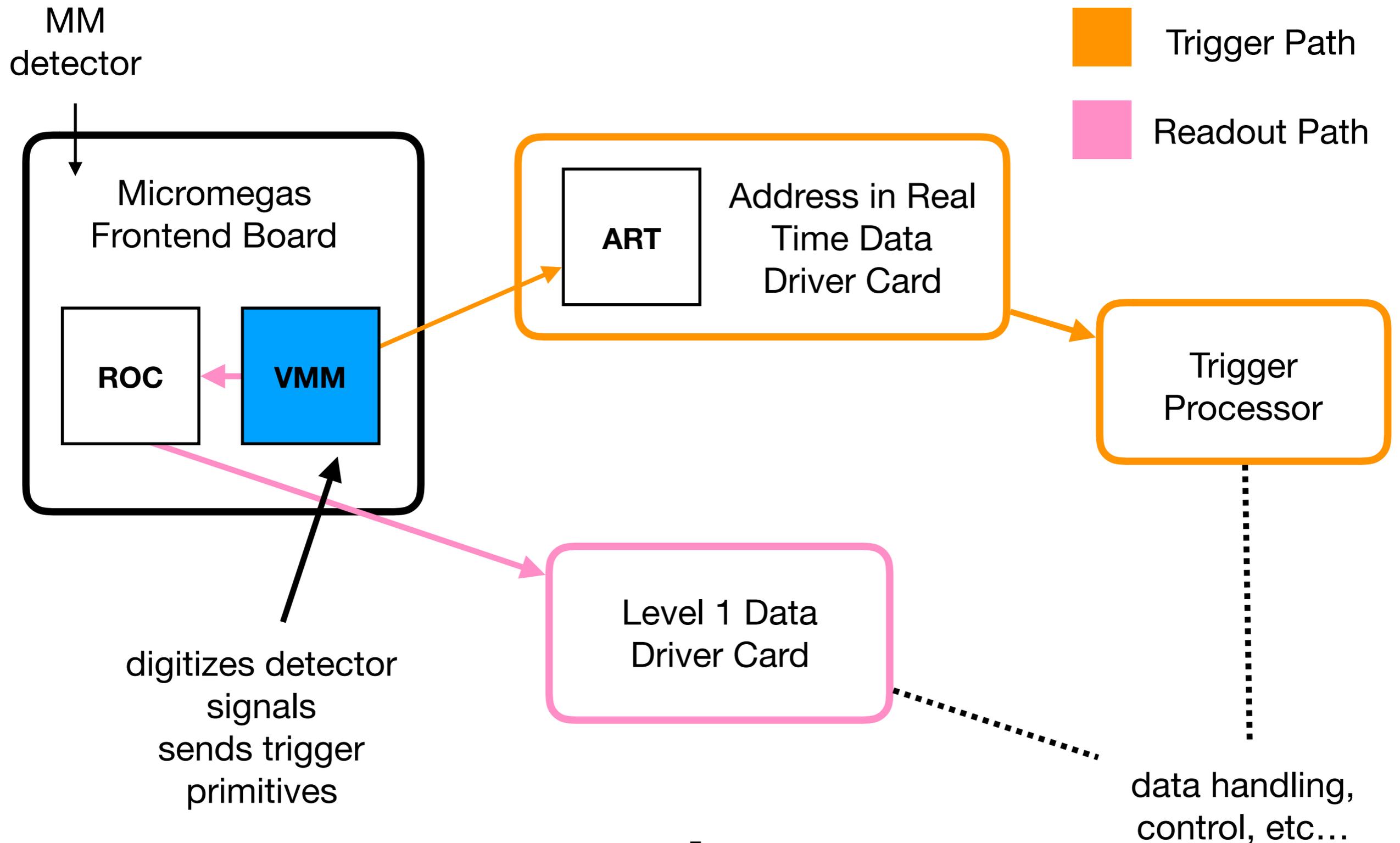


Level 1 Data
Driver Card

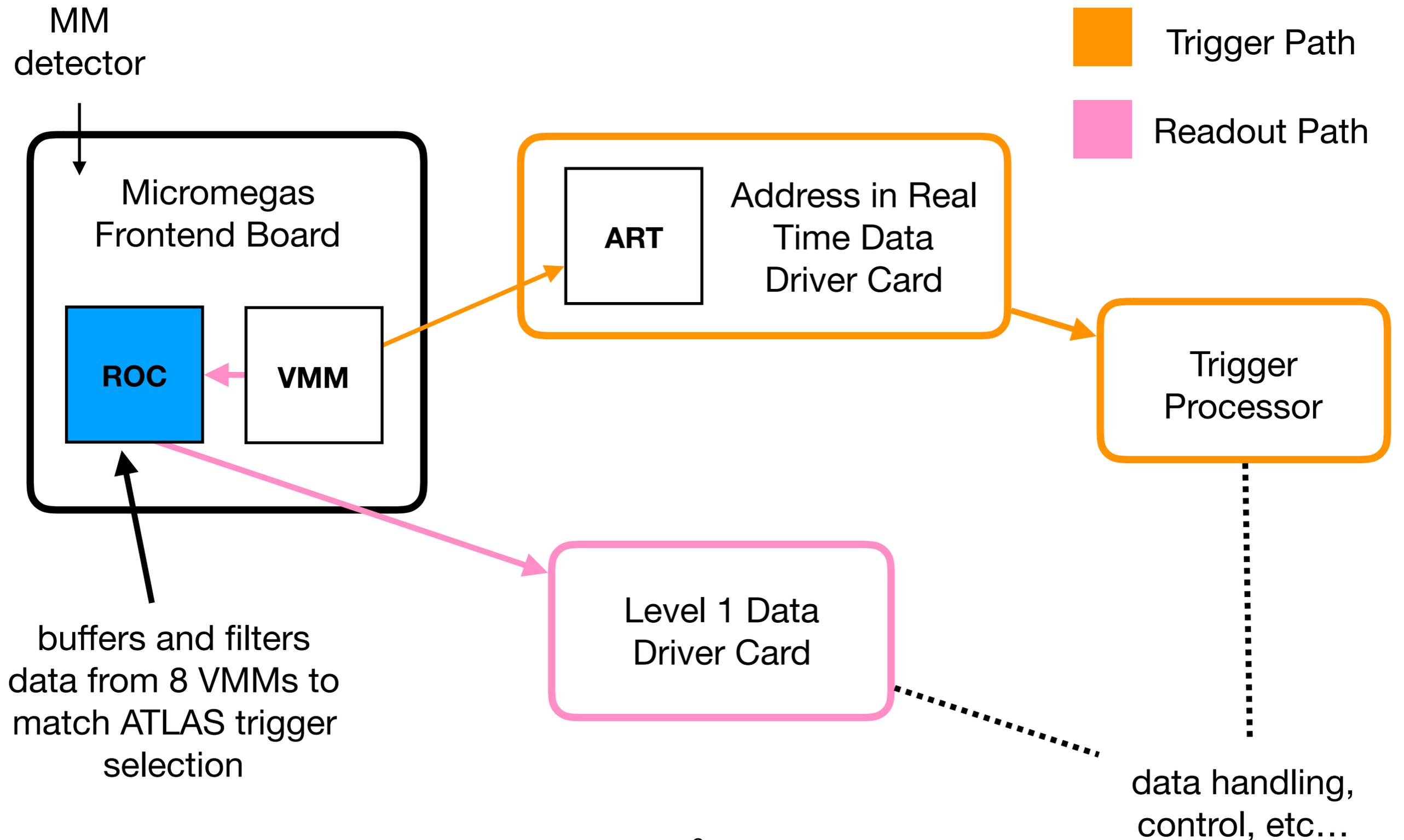


strip Frontend
Board

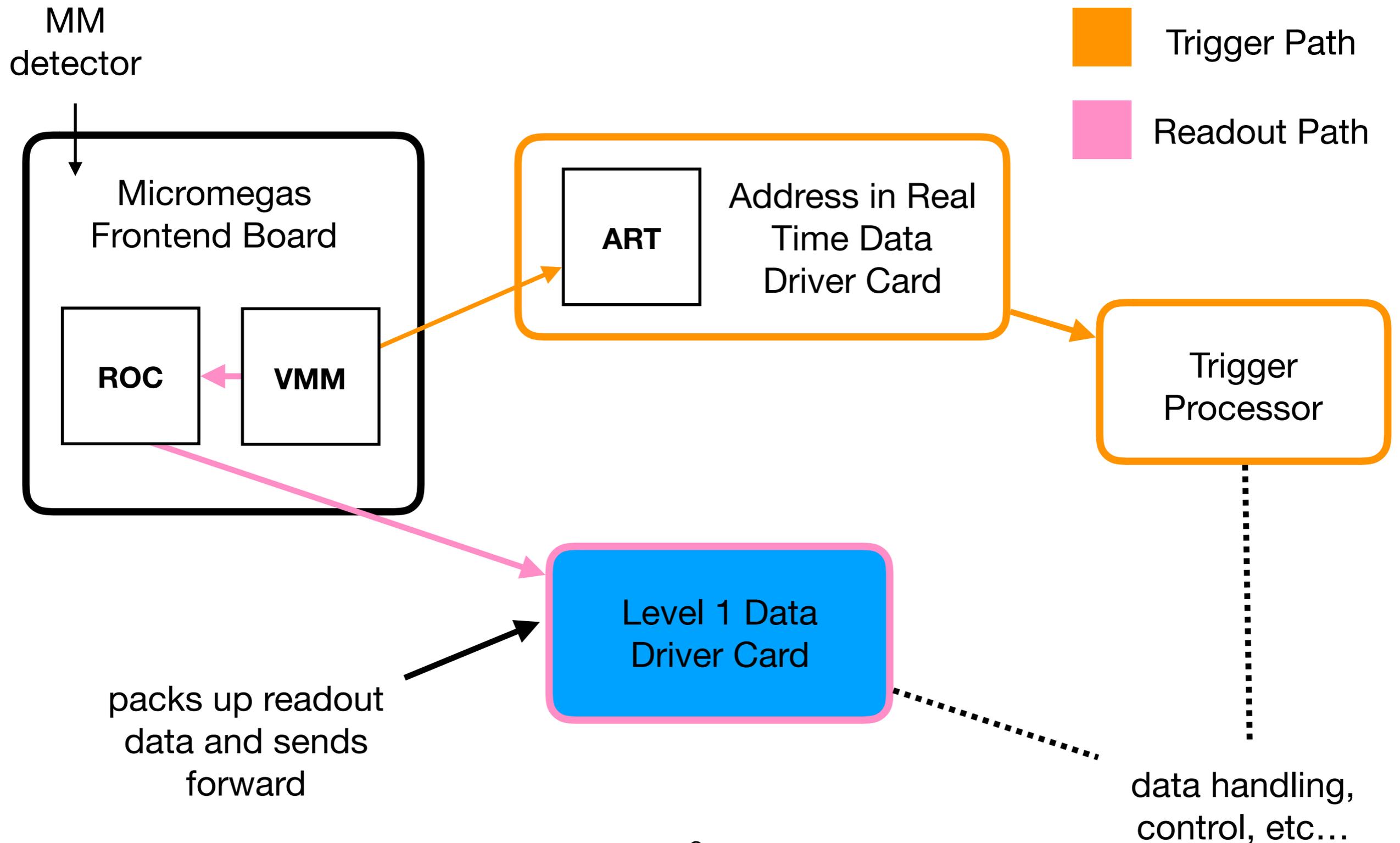
MICROME GAS READOUT PATH



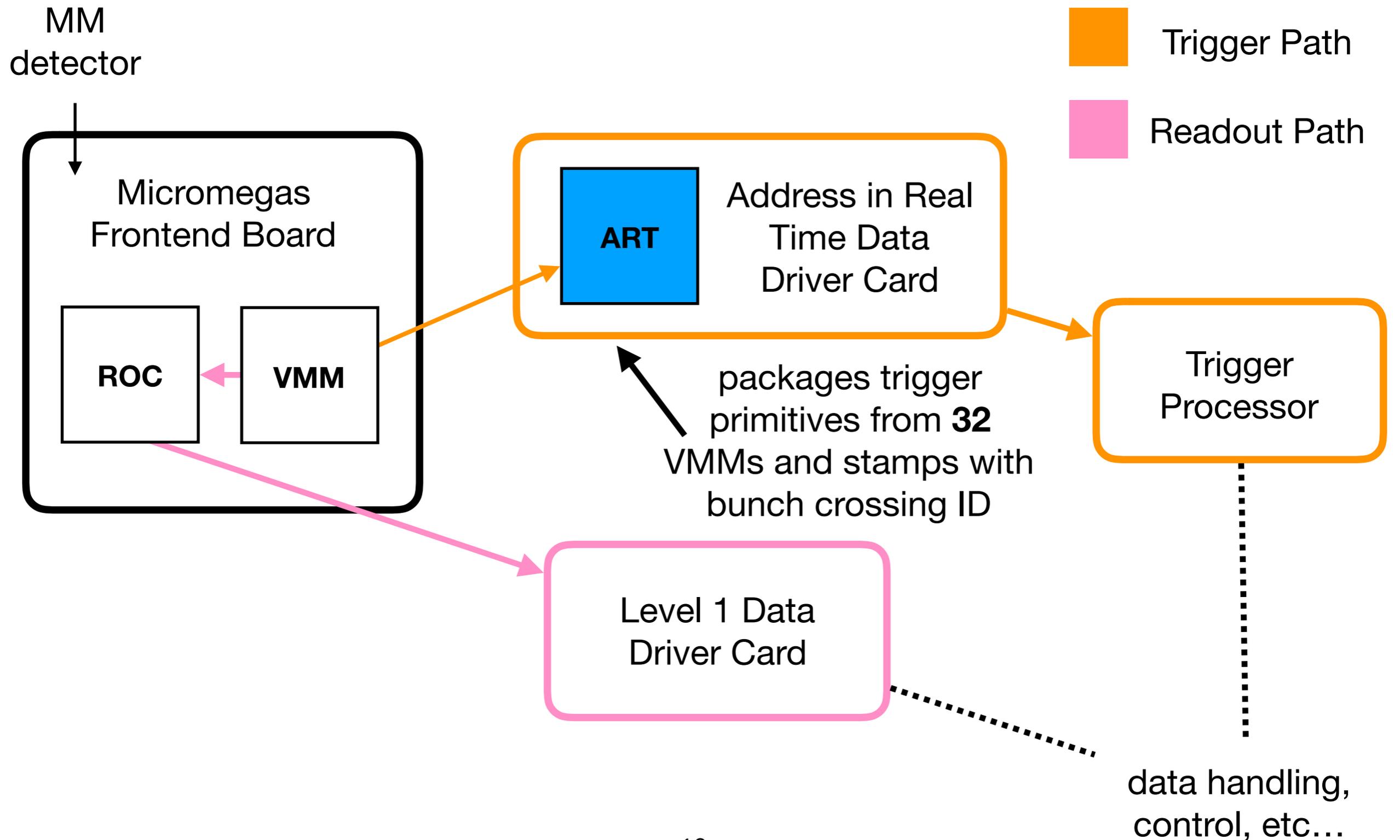
MICROME GAS READOUT PATH



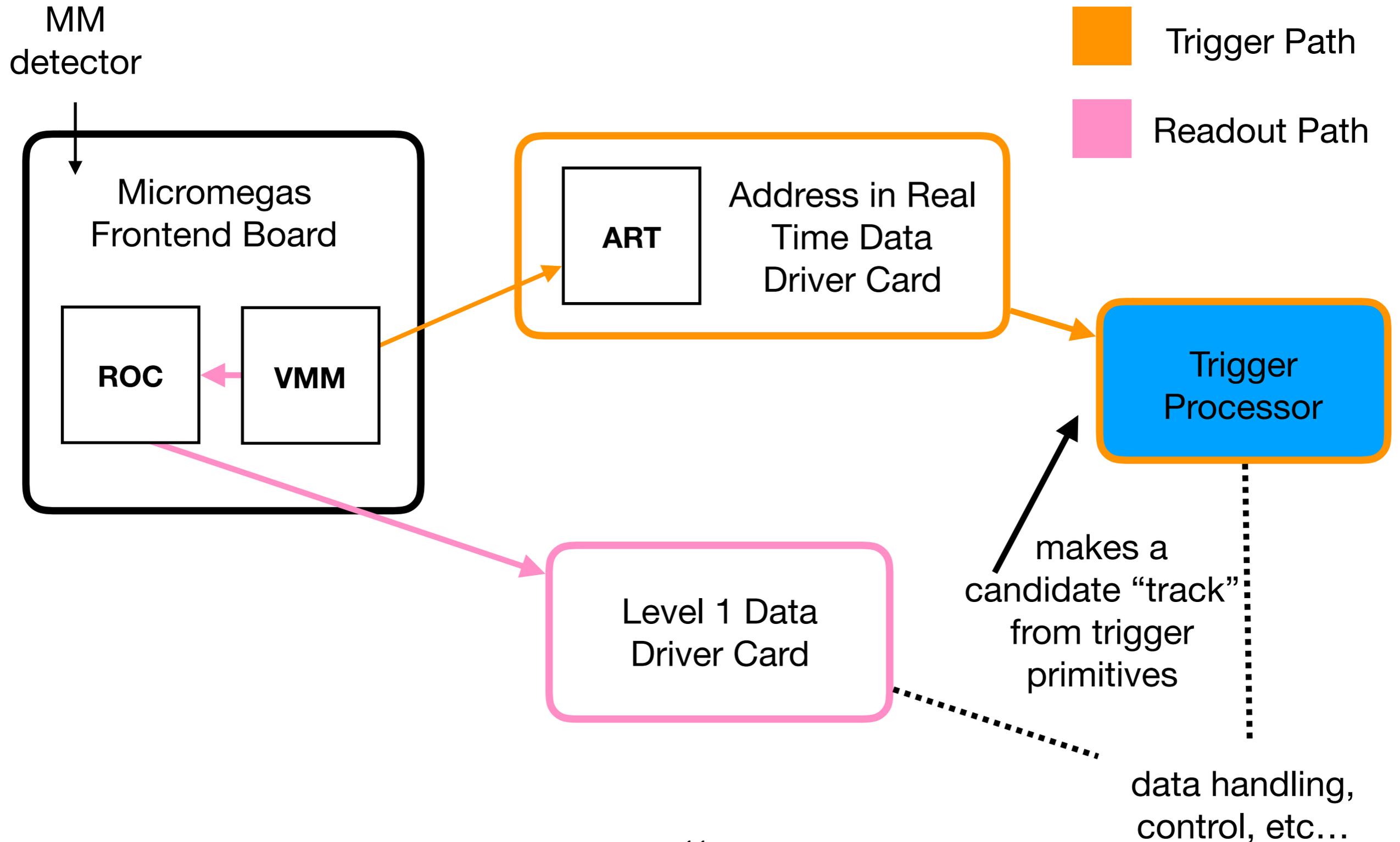
MICROME GAS READOUT PATH



MICROME GAS **TRIGGER** PATH

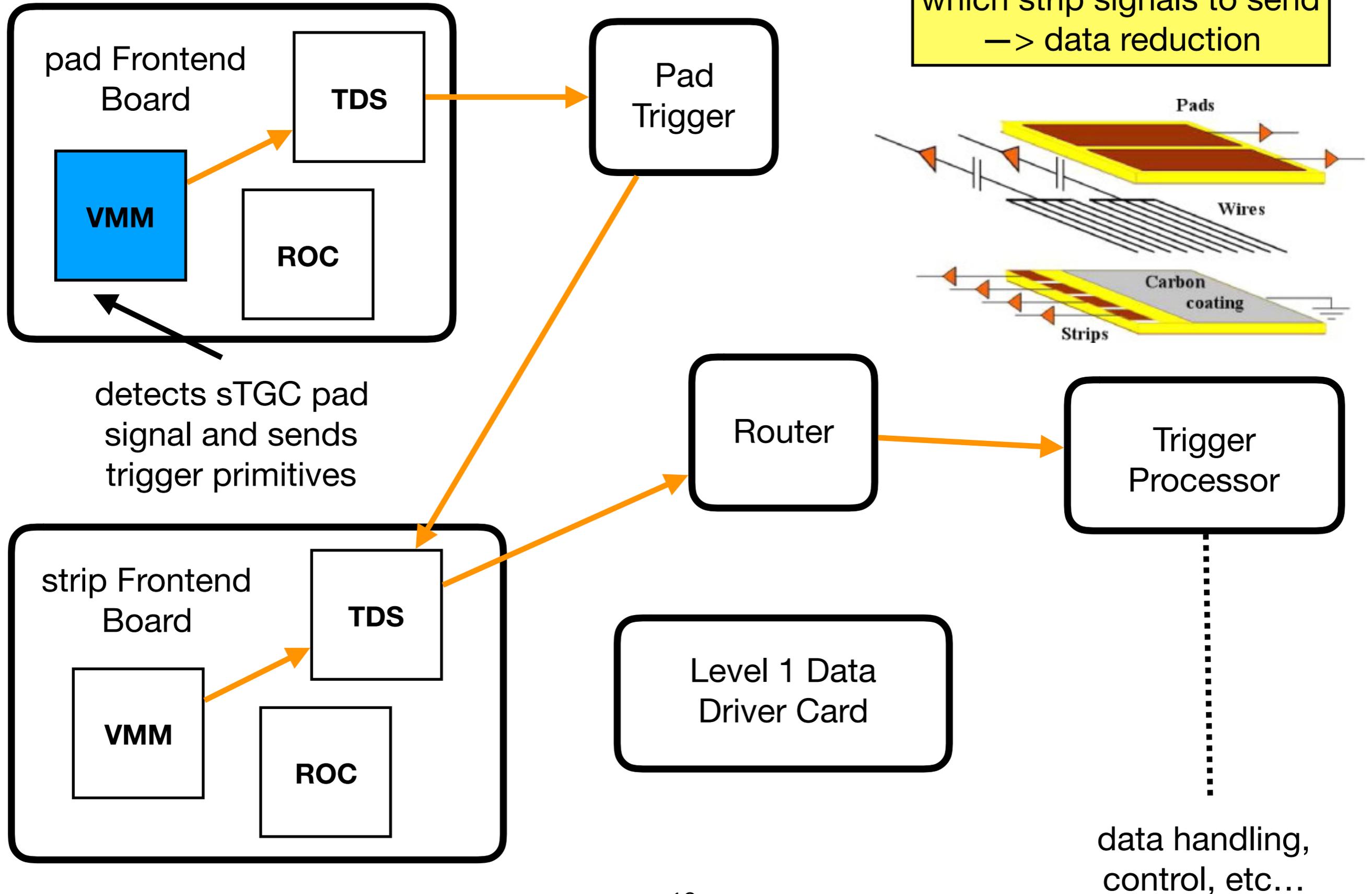


MICROME GAS **TRIGGER** PATH

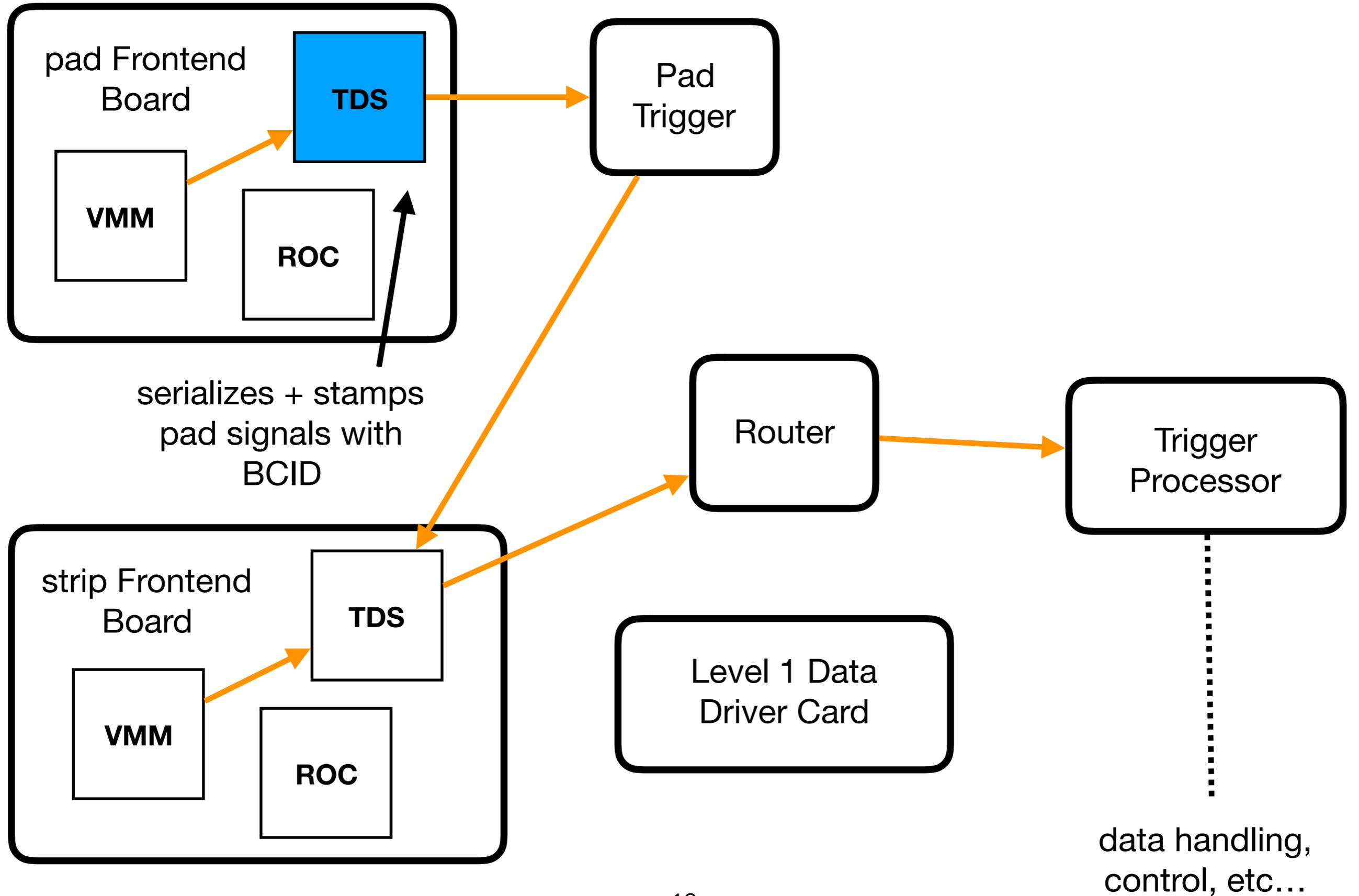


STGC TRIGGER PATH

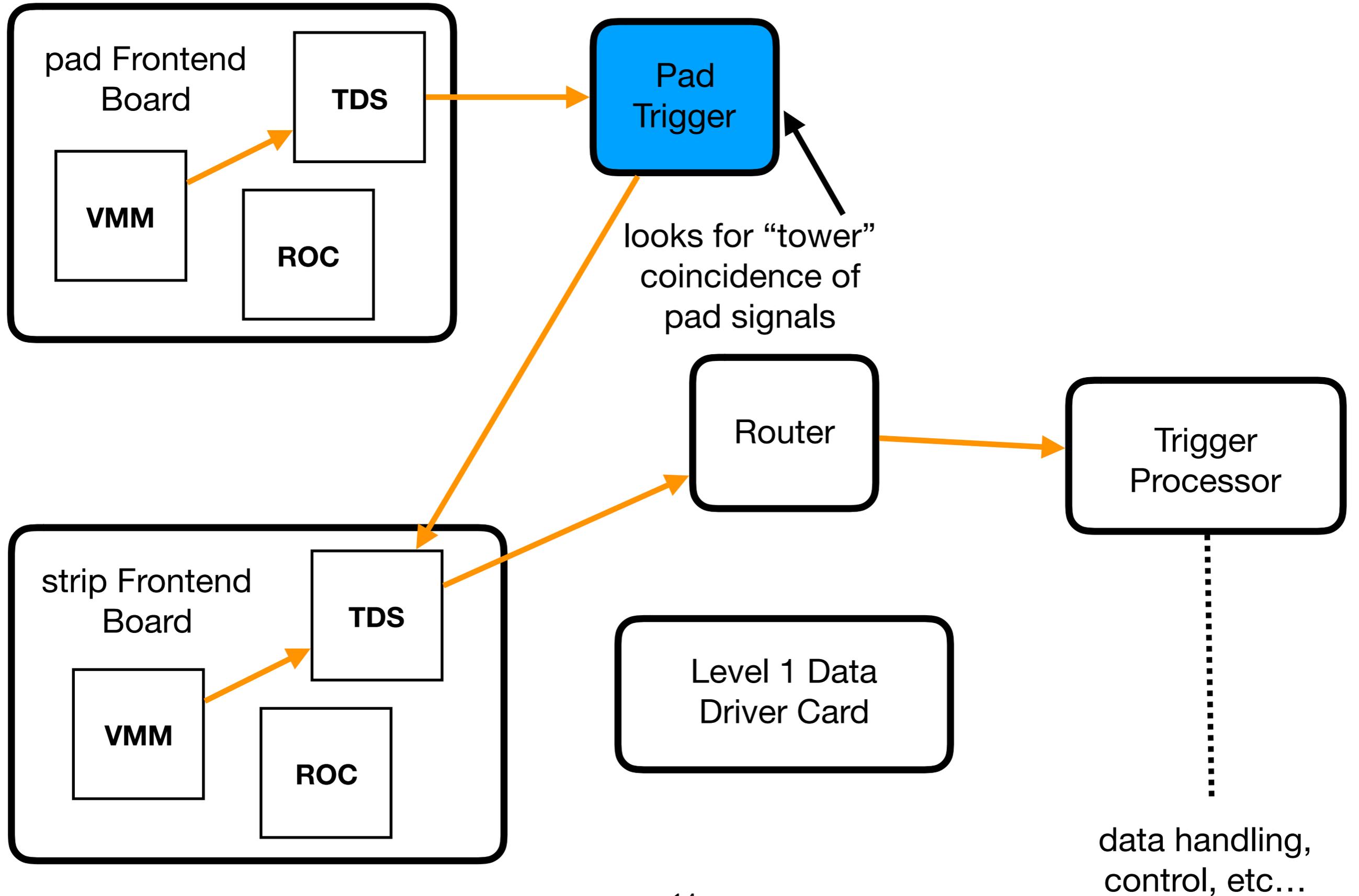
key design principle: use pad signals to filter out which strip signals to send
—> data reduction



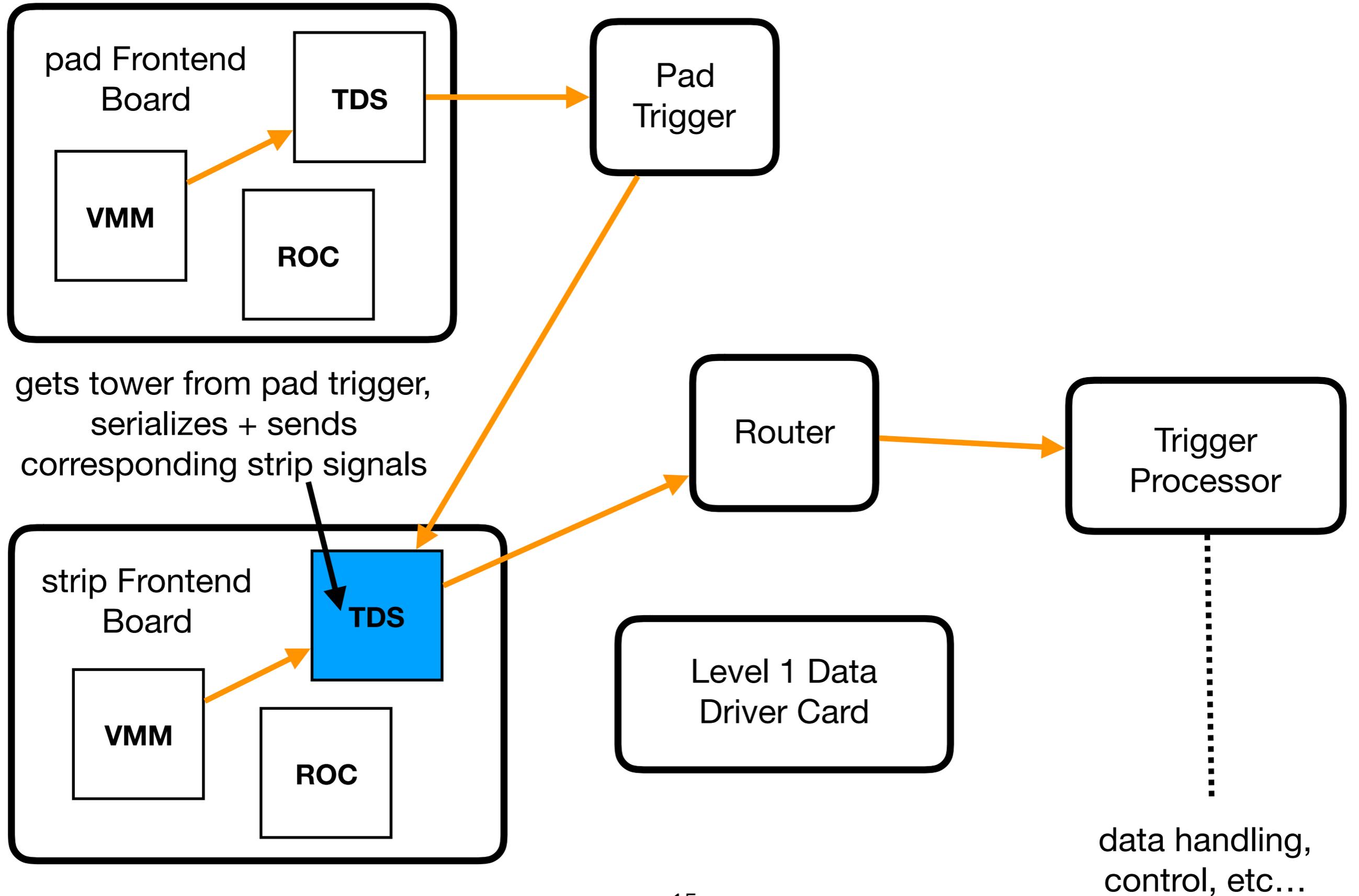
STGC TRIGGER PATH



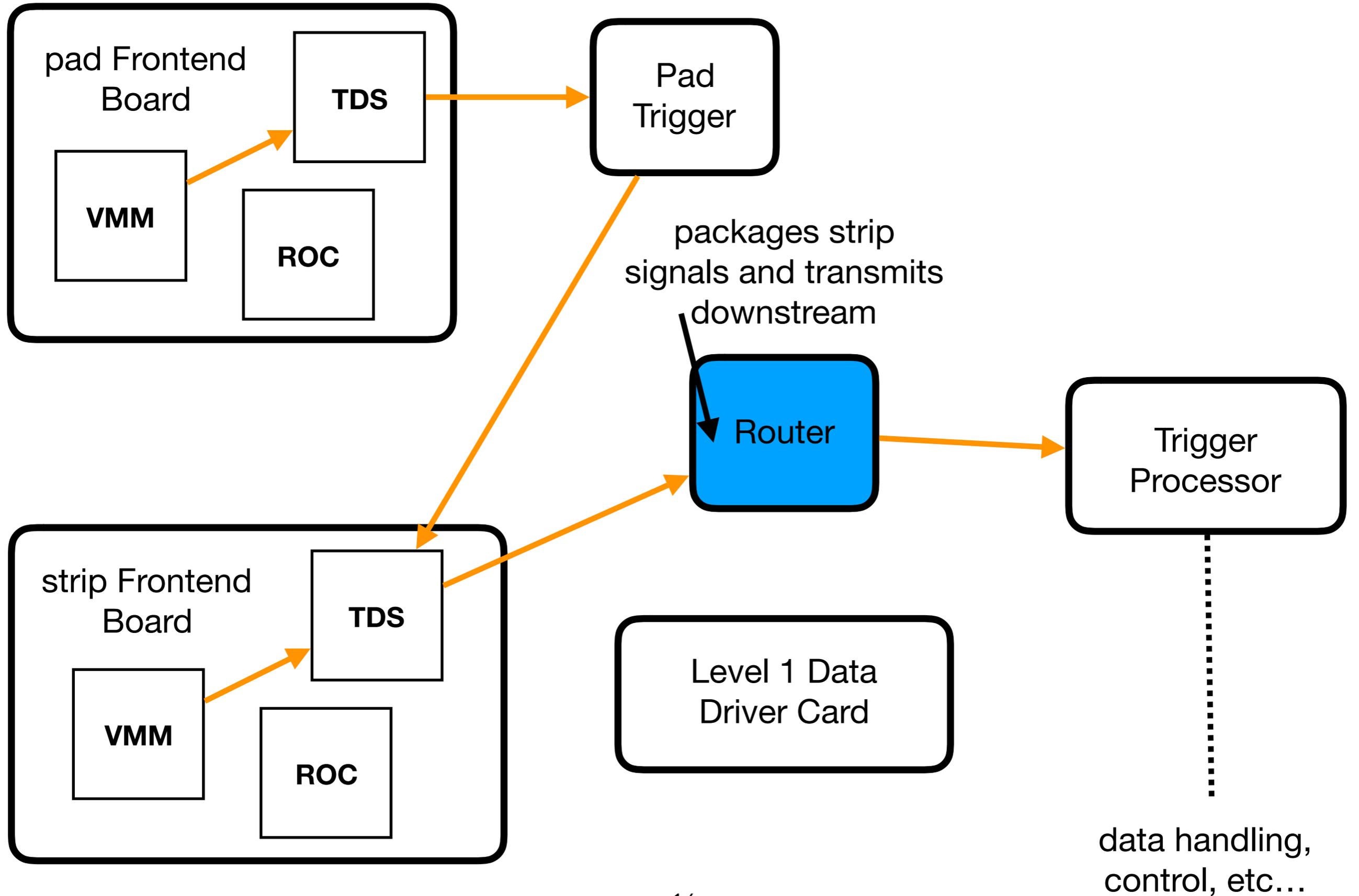
STGC TRIGGER PATH



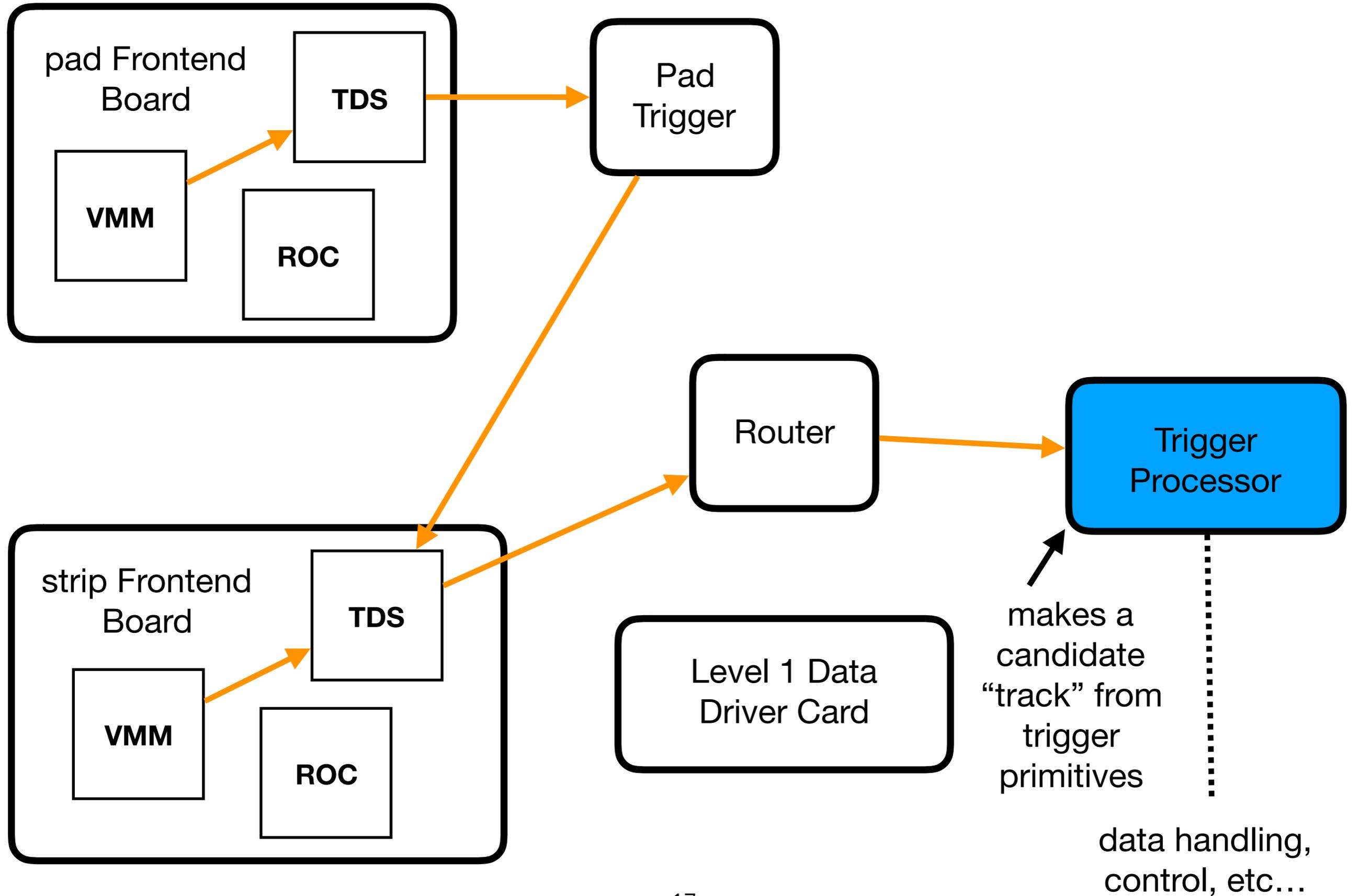
STGC TRIGGER PATH



STGC TRIGGER PATH



STGC TRIGGER PATH



STATUS OF ELECTRONICS (HARDWARE)

deciding on final producer

under review

pre-production

production

done

MM Frontend Board

sTGC Frontend Boards

ART Data Driver Card

Router

Trigger Processor

all ASICs

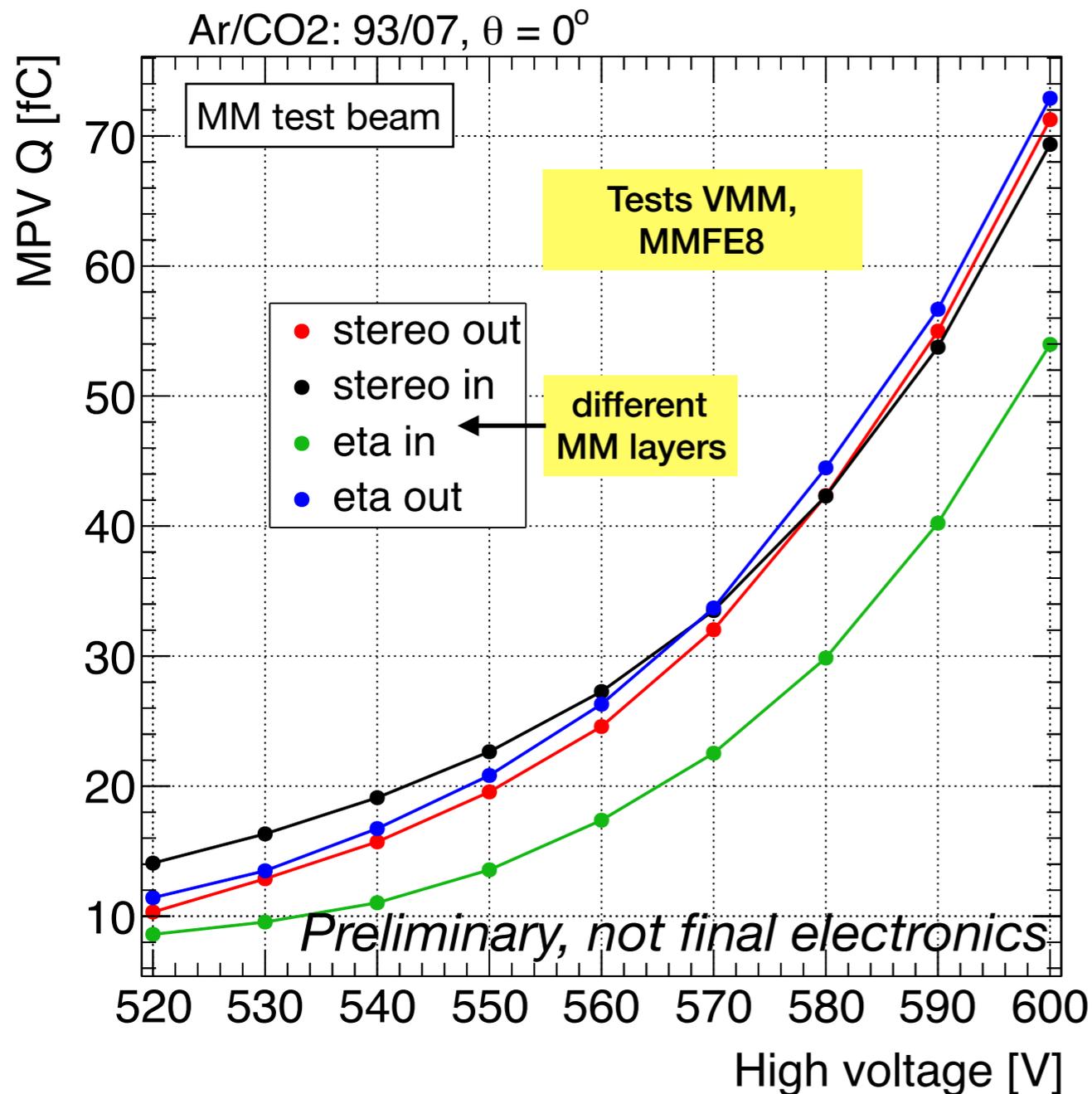
Level-1 Data Driver Card

completely tested and delivered

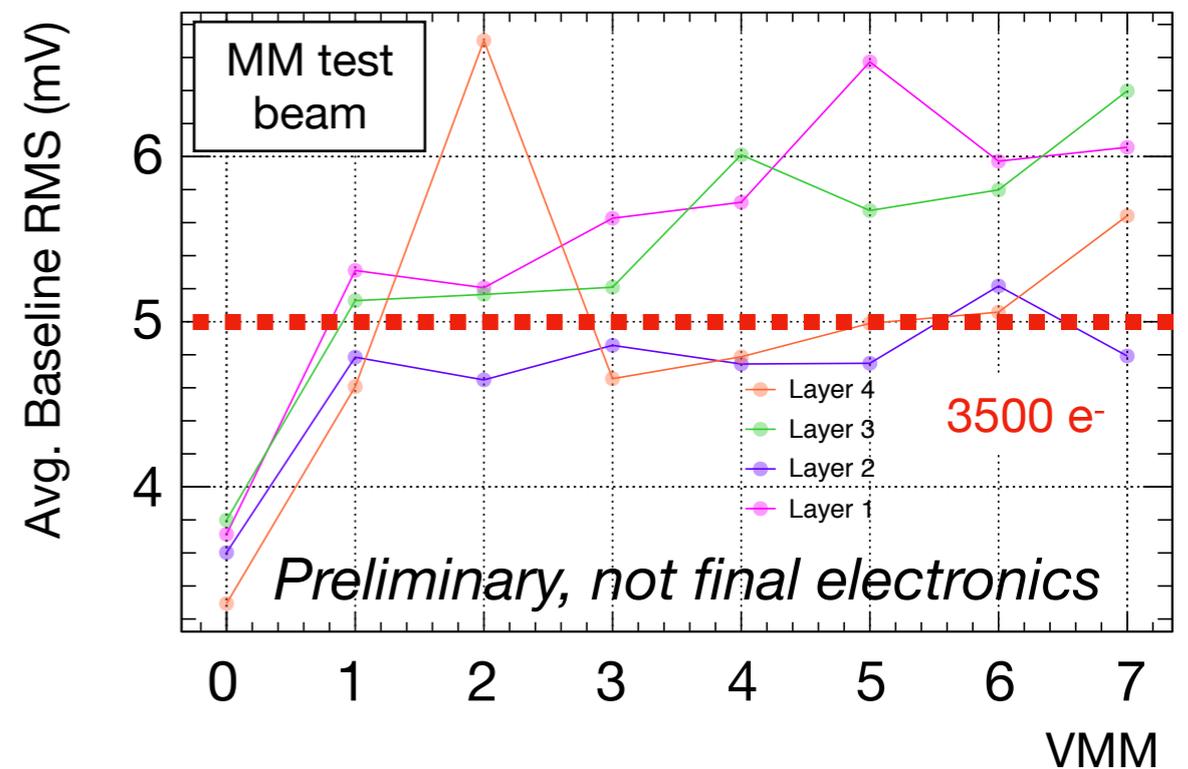
mezzanine card will go into pre-production soon, pre-series carrier cards under test

Pad Trigger

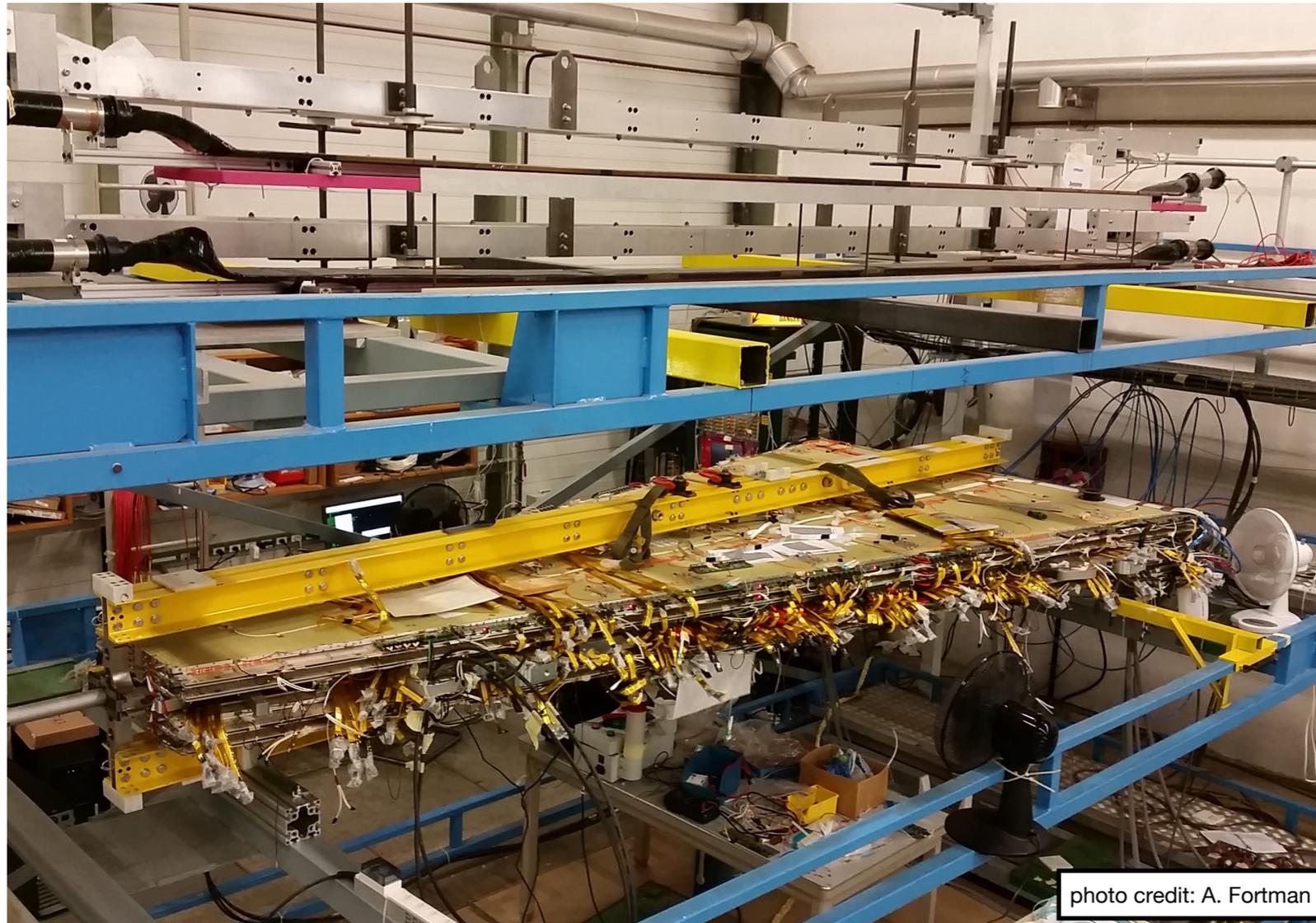
MICROME GAS READOUT CHAIN TESTS



- Electronics have been **continuously** tested during their development and review chain
- For the readout path, we have conducted measurements of efficiency, resolution, noise in a 2018 test beam with pions on a full-size chamber (**VMM, Frontend Board**)



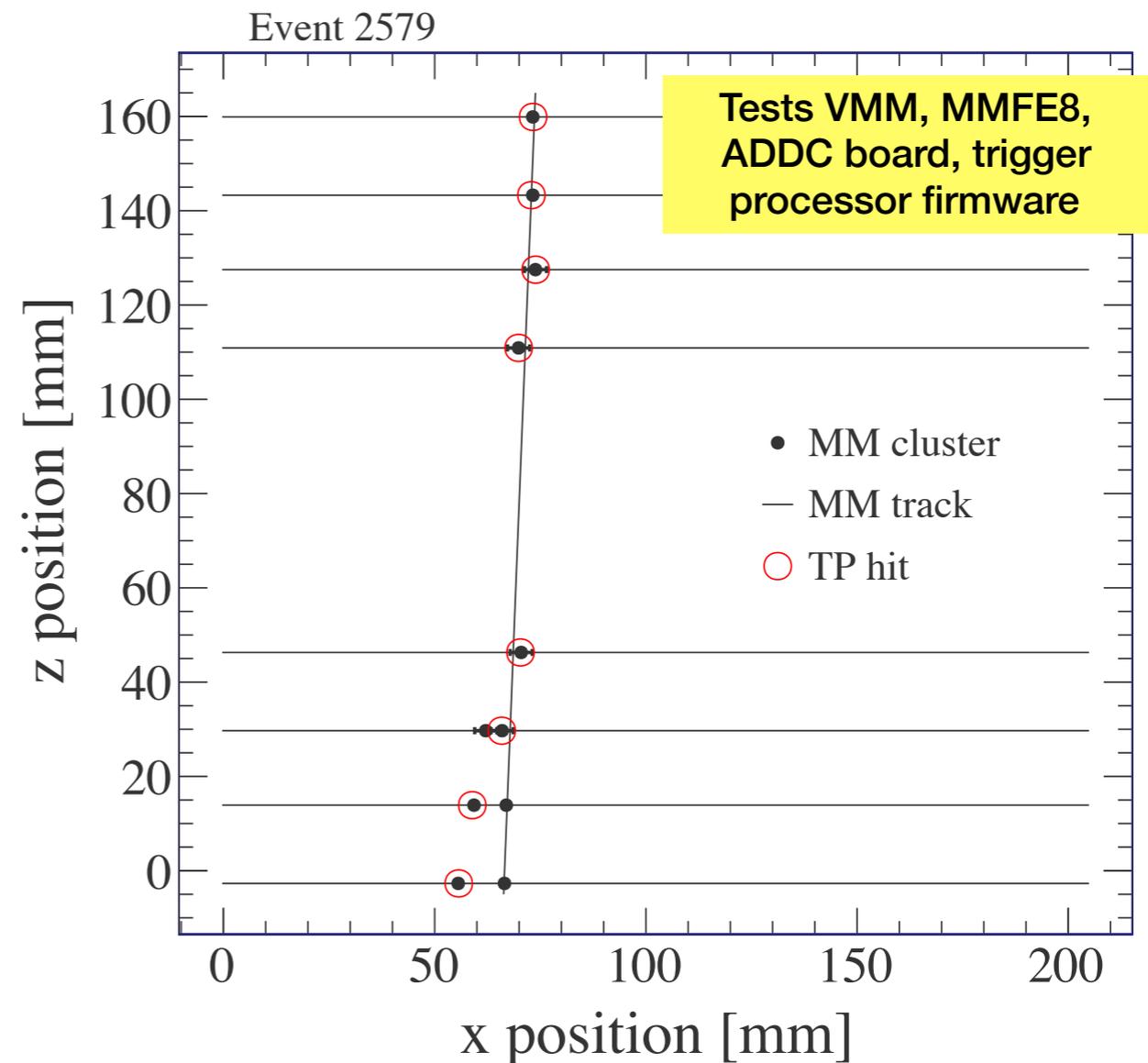
MICROME GAS READOUT CHAIN TESTS



- Now evaluating a double wedge (1/16 of a MM wheel) which is planned for ATLAS installation for HV stability and electronics noise
- Testing the “full system” with 120 Hz of cosmics
- Have successfully collected data with the **VMM** —> **ROC** —> **Level-1 Data Driver Card prototype**

MICROMEGAS TRIGGER CHAIN TESTS

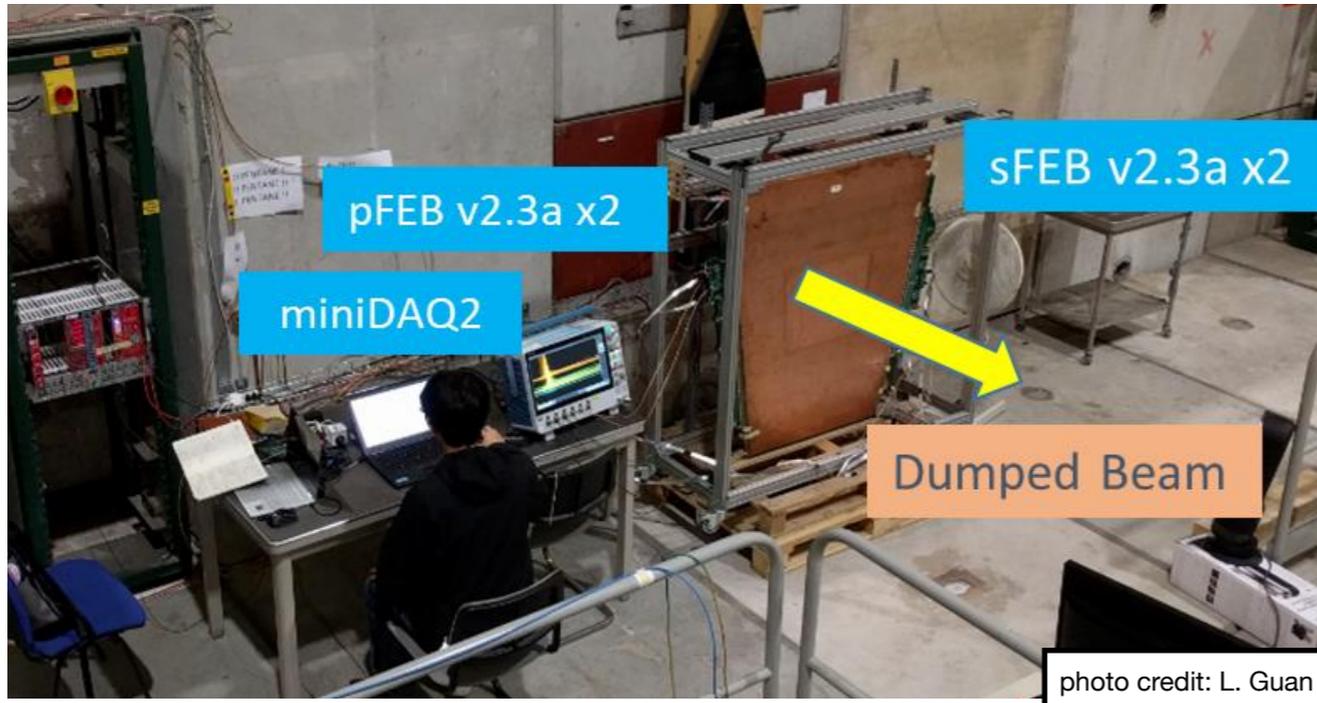
- For the trigger chain, we developed and debugged the trigger processor firmware by taking cosmic muon data with a prototype chamber, **ART Data Driver Card (ADDC) v1** and prototype **MM Frontend Boards**
- In the testbeam, the trigger path from **VMM** to the **ADDC v2** with **ART** was validated
- Currently developing trigger DAQ with the final ATLAS system to test final trigger processor hardware



Sep 2017 cosmic track with full prototype trigger chain

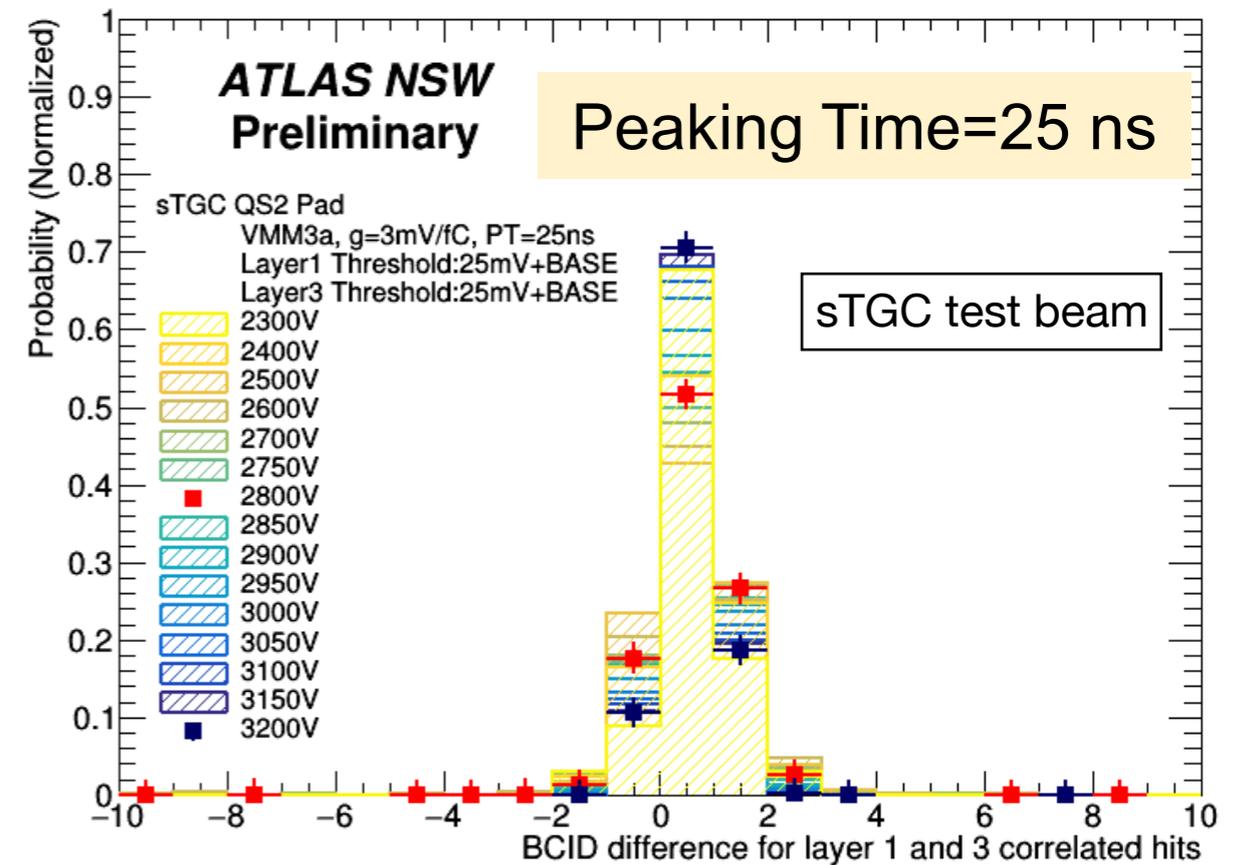
STGC ELECTRONICS TESTS

Test beam - tests of pFEB and sFEB prototypes with VMM, TDS

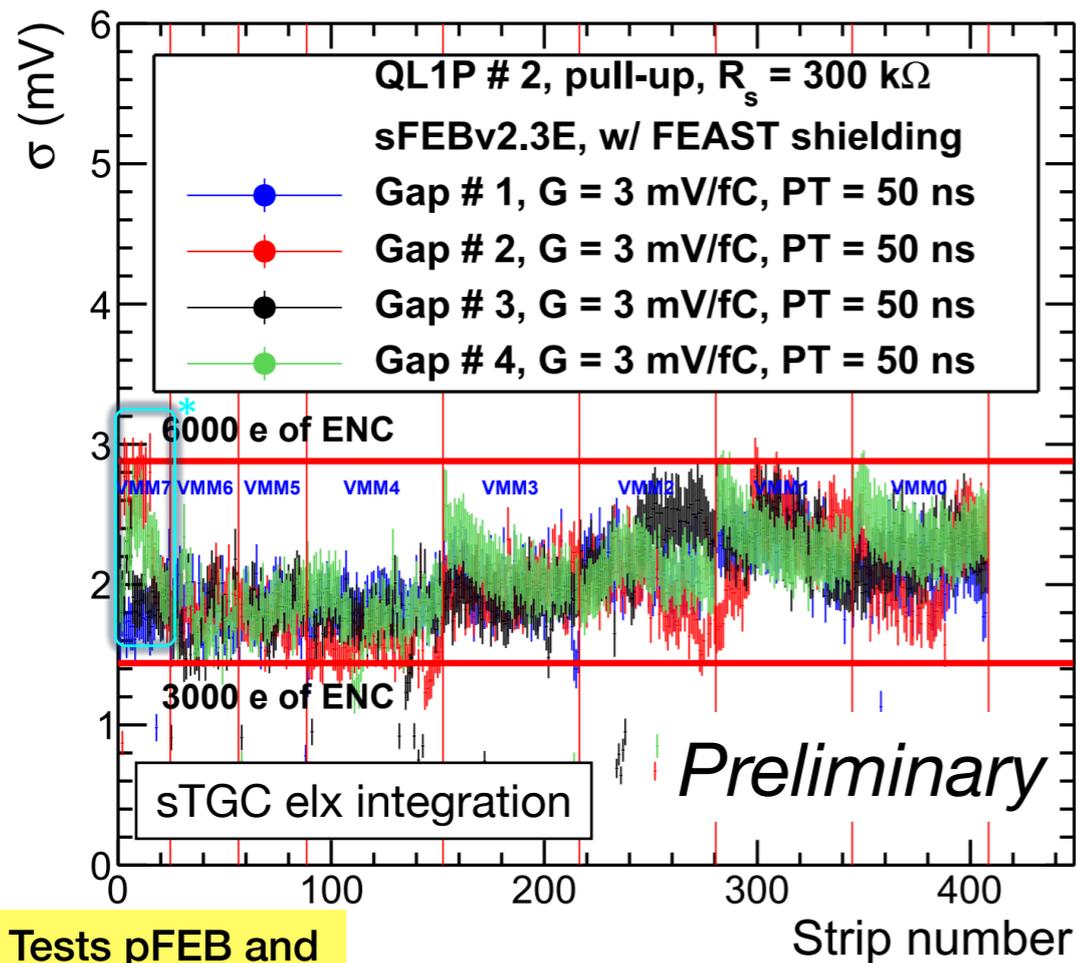


- sTGC detector efficiencies, charge distributions, resolutions, were also measured in a test beam

- Coincidences between two pads was demonstrated using **pad Frontend Board** prototype with VMM, TDS



STGC ELECTRONICS TESTS



Tests pFEB and VMM

- Currently testing a large sTGC quadruplet equipped with latest **strip** and **pad Frontend Board** prototypes
- Extensive noise tests conducted, e.g. recent tests identified and fixed noise from the on-board DC-DC converters
- Digital readout path with **VMM** and **ROC** also being tested
- **Pad trigger** firmware prototype has been completed

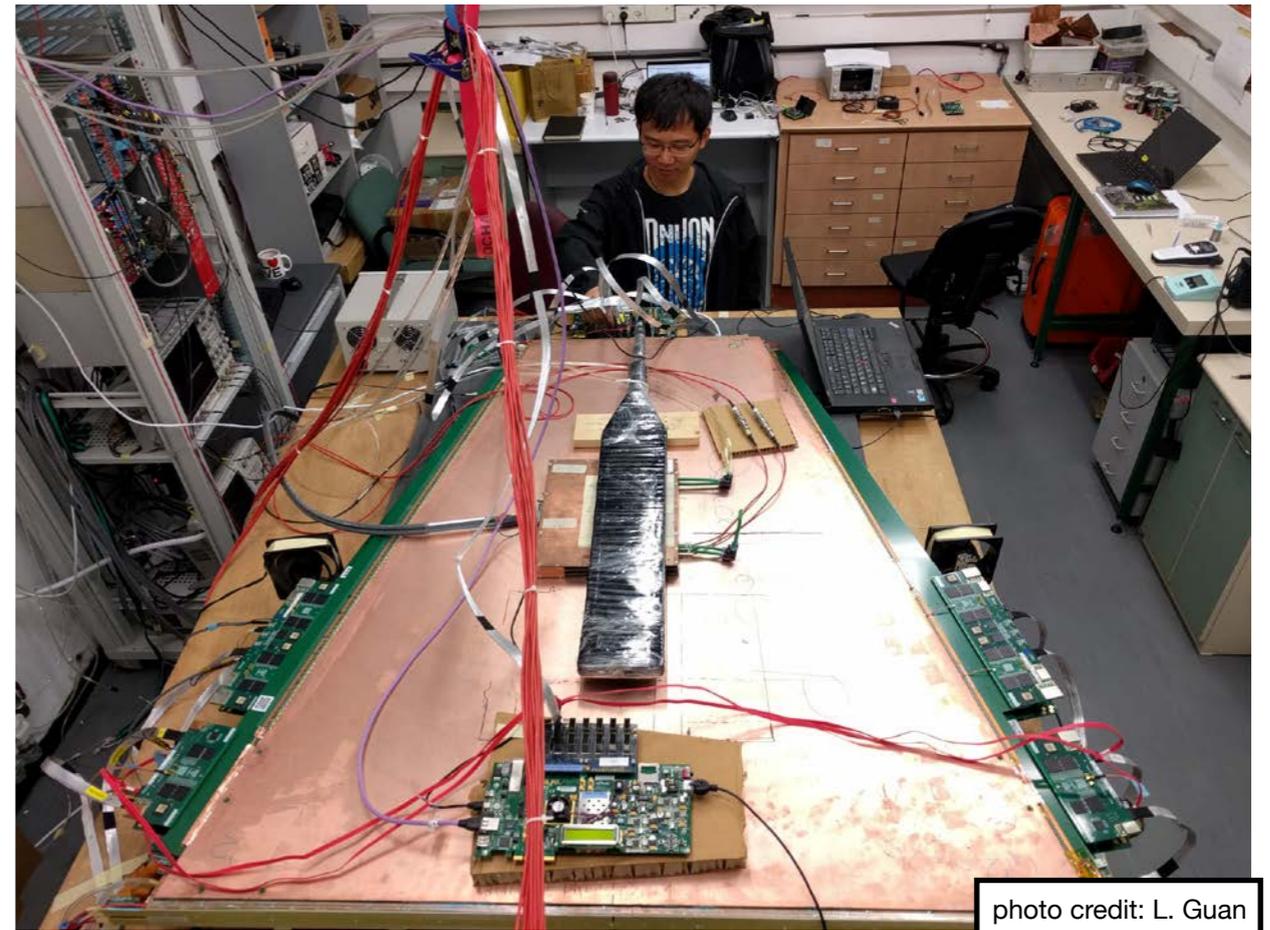


photo credit: L. Guan

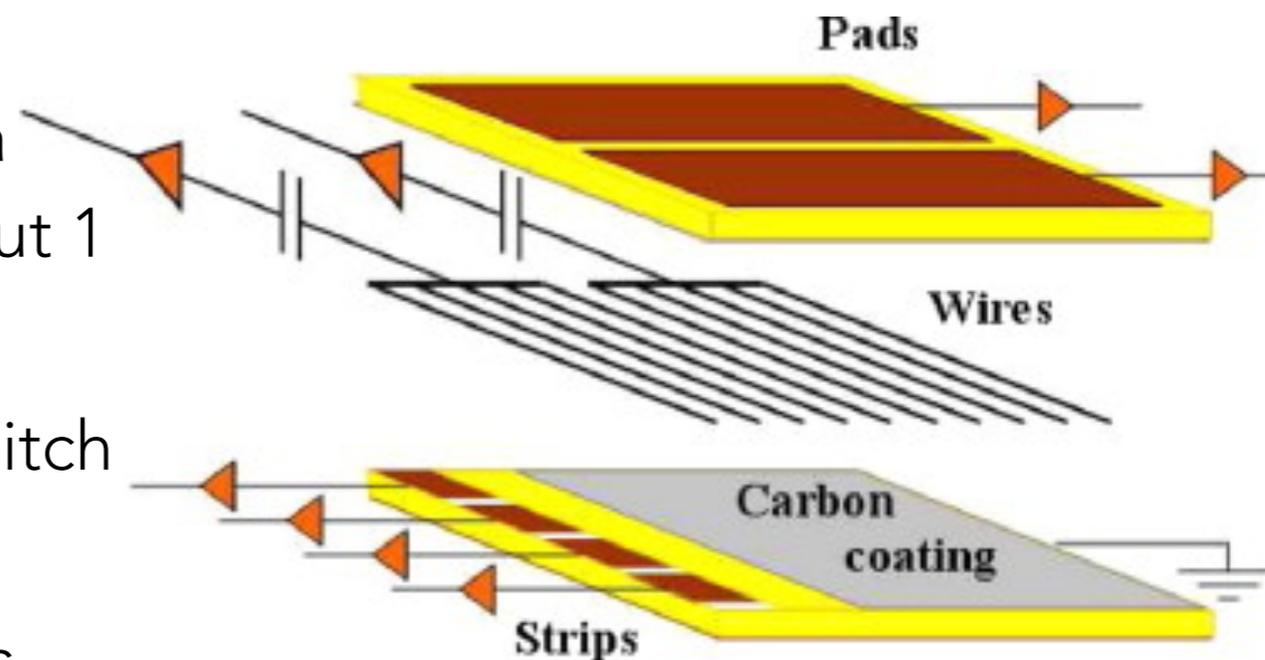
SUMMARY

- NSW + NSW electronics system was designed to handle the challenges of increased instantaneous luminosity at the High Luminosity LHC
 - High radiation environment, high particle rates
- Right now is an exciting time! Integration ongoing with final chambers and electronics to confirm that the system is functional before ATLAS installation of a wheel planned in 2020
- Thank you!

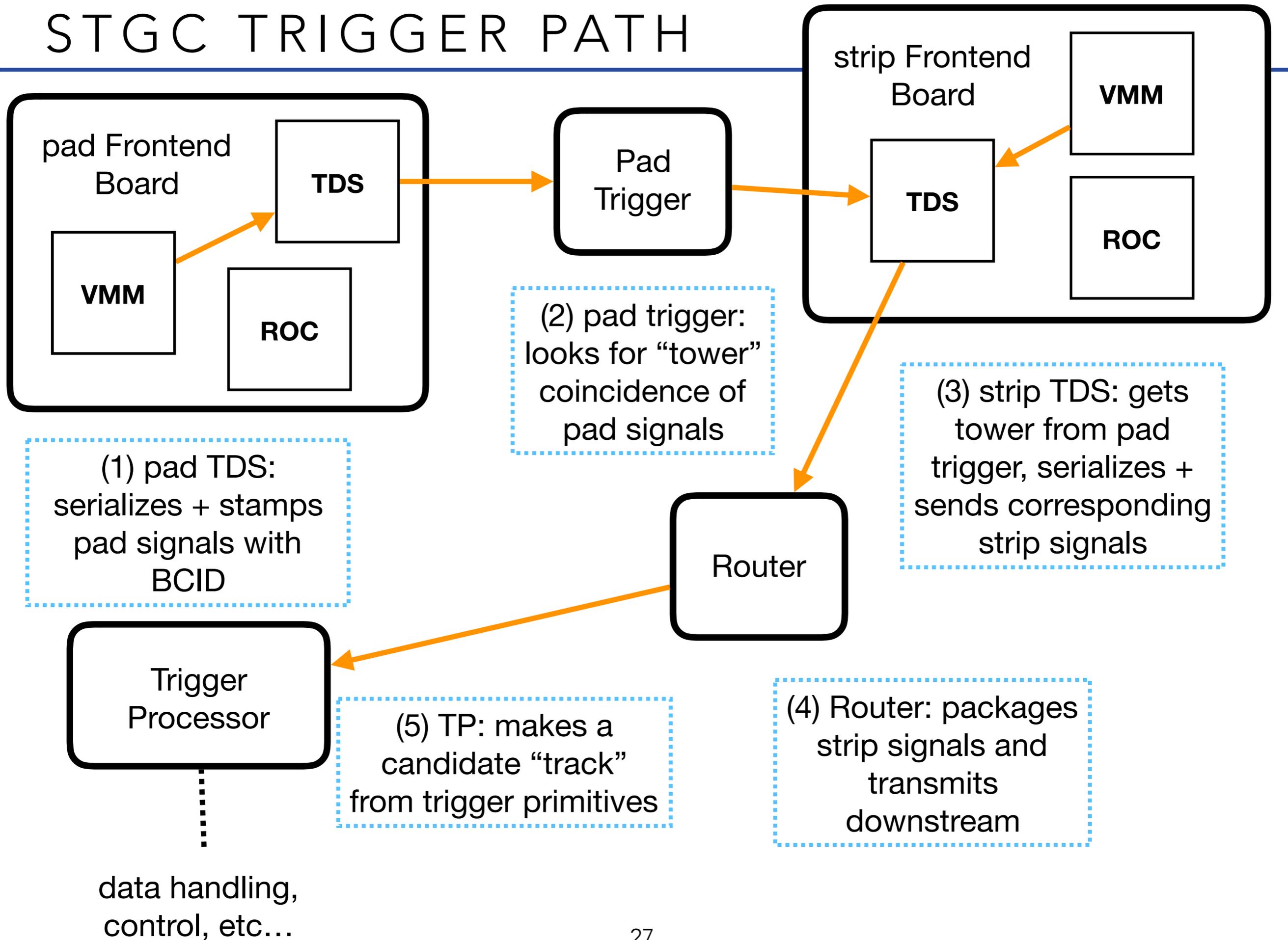
BACKUP

SOME STGC DESIGN CHALLENGES

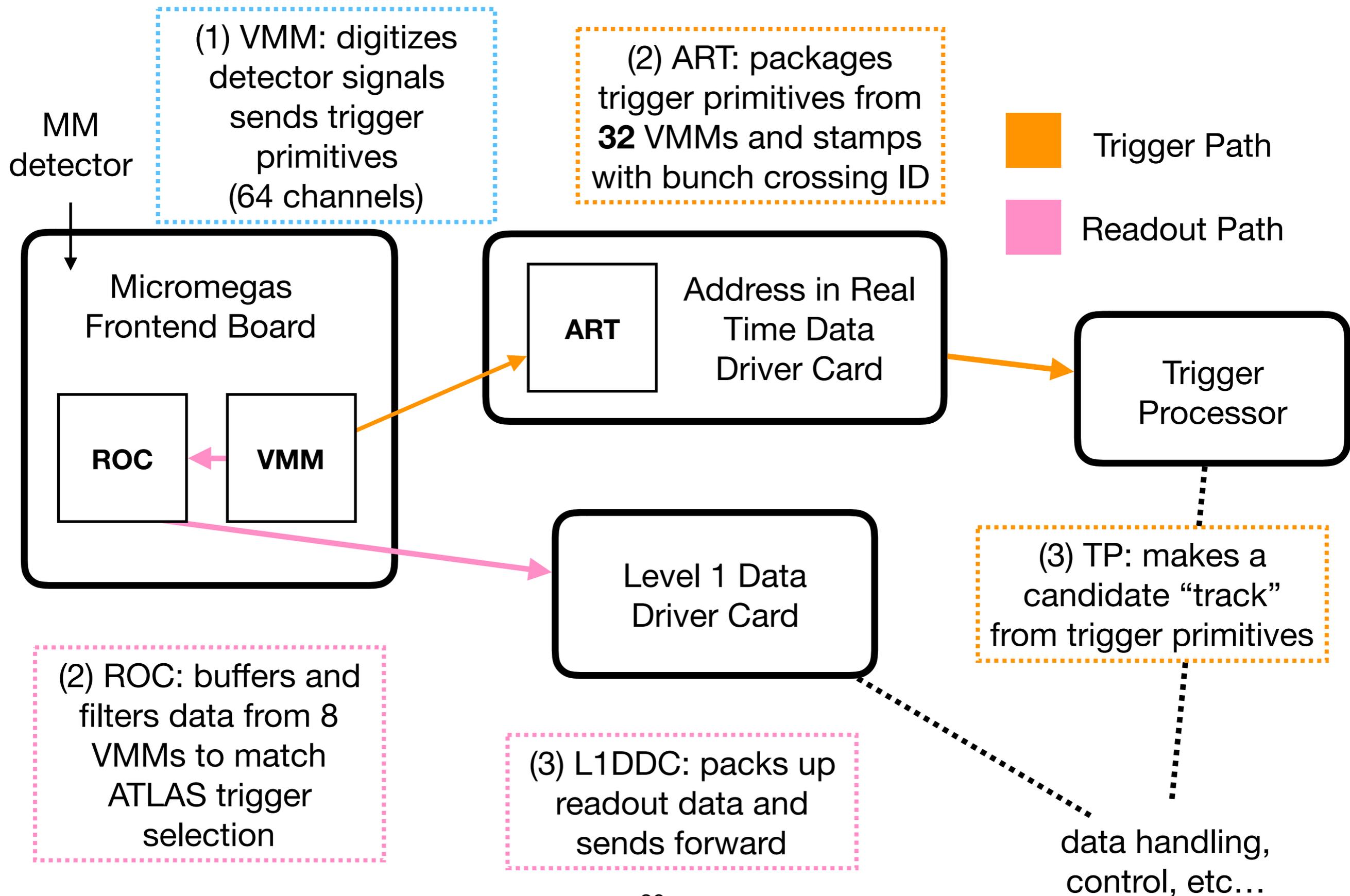
- **Unique sTGC challenge**
- **~45k sTGC pads, ~280k strips in the entire NSW**
- **Need fine strip granularity without huge amounts of trigger data to process**
 - MM sends address of first strip hit in a VMM (strip pitch ~425-450 microns, but 1 VMM covers ~2.7 cm)
 - sTGC pads cover 4+ cm, sTGC strip pitch 3.2 mm
- *Solution:* select which strip trigger signals should be processed using pad signals
- **Basis of electronics design**
- using pads to filter which strips are read out reduces data rate by ~ 60-100x



STGC TRIGGER PATH



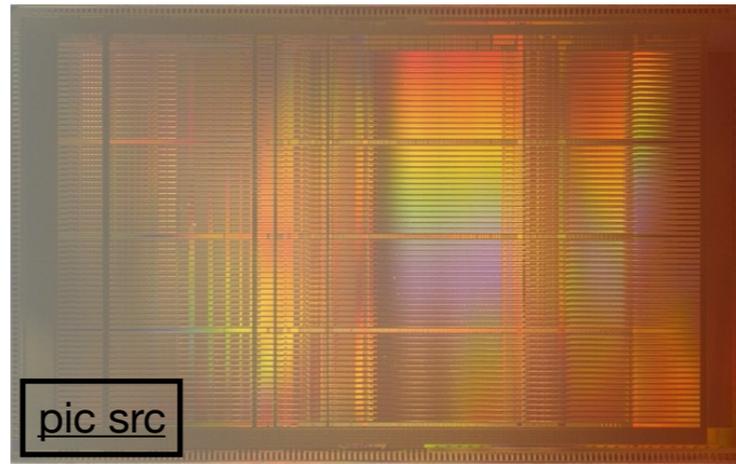
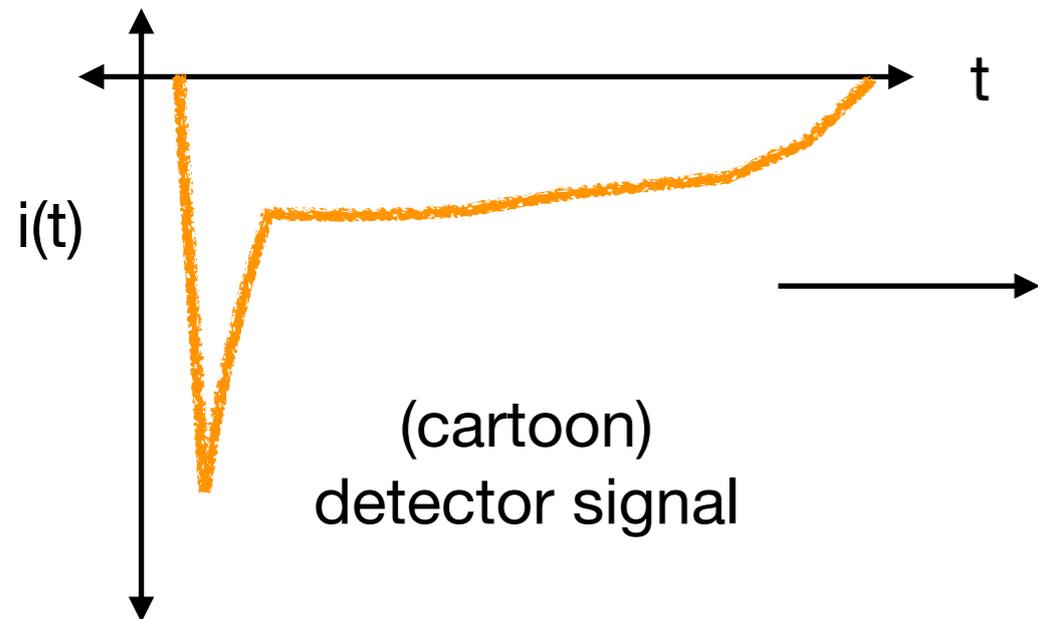
MICROMEAS ELECTRONICS



NSW ELECTRONICS DESIGN

1. **2+ million** MM strips need to be read out, **~45k** sTGC pads, **~280k** strips for the sTGC
2. Radiation intensive environment
 - Total Ionizing Dose ~ 0.5 Mrad
3. Need low power losses, MM requires 34 kW of power, sTGC requires 14.6 kW of power
4. Everything needs to be **fast** - < 1025 ns for trigger signals to go to ATLAS "Sector Logic"
5. Reuse as many electronics as possible between sTGC and MM

SPOTLIGHT: VMM FRONT-END ASIC



- **64** input channels
- measures **time** and **charge** of signal
- provides fast trigger signals
- used for both MM and sTGC
- radiation hard CMOS technology

Readout path

8-bit fine time information

10-bit charge information

BCID

channel

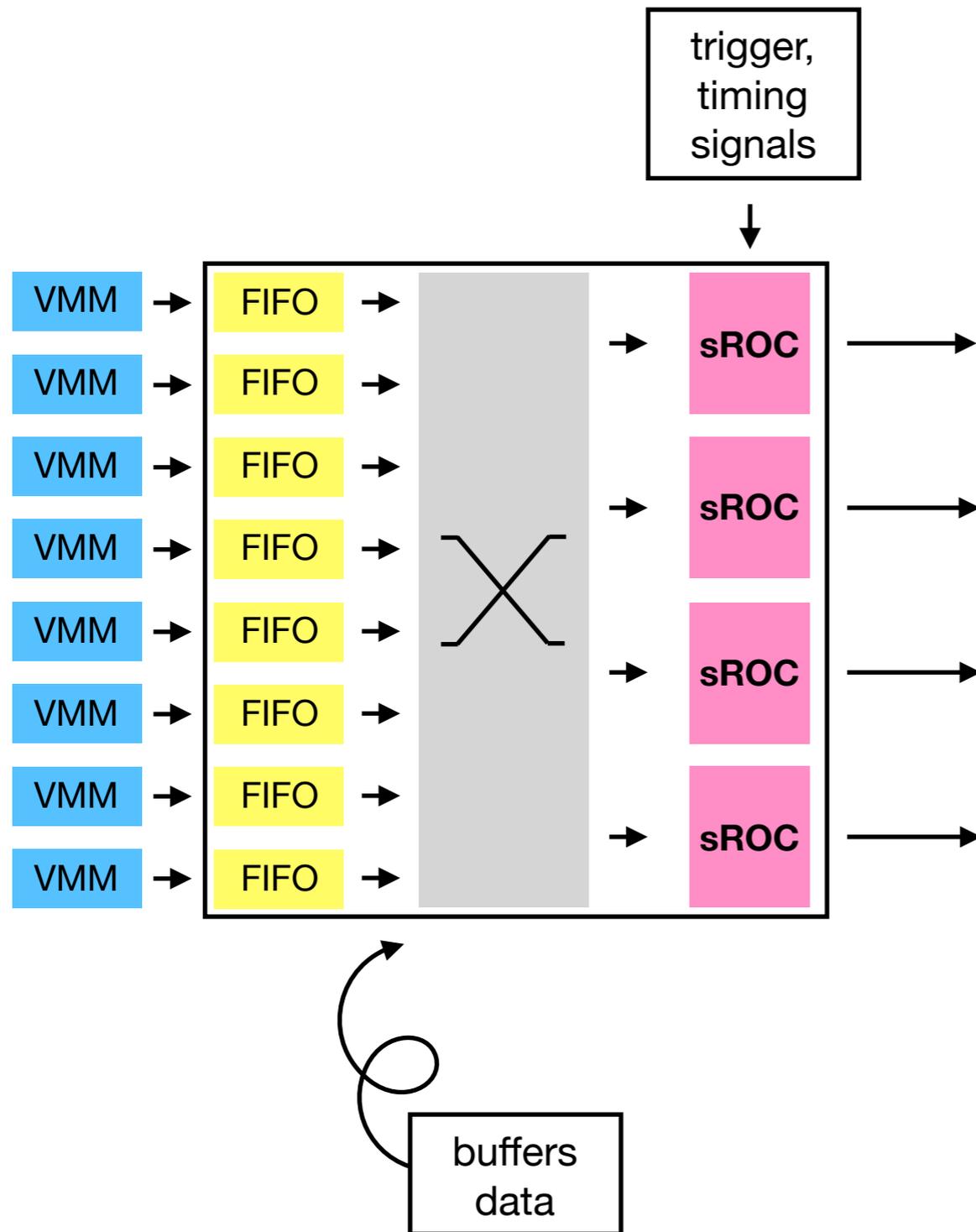
Trigger path

MM trigger hit: channel address of first strip over threshold

Pad trigger signal: pulse for Time over Threshold (ToT)

Strip trigger signal: 6-bit channel peak value

ROC, ART, TDS



Readout Controller (ROC)
looks for hits matching a desired BCID + packages the hits
transmits at ~ 320 Mb/s

Address In Real Time (ART)
deserializes VMM MM trigger hits
stamps them with the BCID

Trigger Data Serializer (TDS)
serializes VMM data and
matches pads and strips