FRONTEND AND BACKEND ELECTRONICS FOR THE ATLAS NEW SMALL WHEEL UPGRADE

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ON BEHALF OF THE ATLAS MUON COLLABORATION
The High Luminosity Large Hadron Collider will have 2-4x larger peak instantaneous luminosity compared to LHC Run 2.

Run 3 will have a factor of ~1.5x increase in instantaneous luminosity.

The New Small Wheel (NSW) upgrade will replace the Small Wheel of the current ATLAS Muon Spectrometer to handle large particle rates.

Important for Run 3, vital for HL-LHC.
WHY DO WE NEED AN UPGRADE?

- **Tracking:** Monitored Drift Tubes will lose efficiency at high hit rates due to higher instantaneous luminosity

- **Triggering:** Lowest unprescaled muon trigger is dominated by fake muons in the endcap region
WHY DO WE NEED AN UPGRADE?

- **Tracking:** Monitored Drift Tubes will lose efficiency at high hit rates due to higher instantaneous luminosity

- **Triggering:** Lowest unprescaled muon trigger is dominated by fake muons in the endcap region
Micromegas (MM) detector

- Precision tracking
  - **small strip pitch** (~425-450 microns compared to current 3 cm drift tube)
  - **short drift time** (~100 ns compared to ~750 ns for drift tubes)
  - fine pitch and fast drift time allow MM to handle high particle rates

also provides a trigger signal!

small strip Thin Gap Chambers (sTGC)

- Fast triggering
  - **small strip pitch** (3.2 mm) compared to TGC wire groups (~10-50 mm) —> ~ 2 mrad trigger track resolution
  - **high efficiency** under tests with γ irradiation of 20 kHz/cm²
  - will **reduce** the Level 1 lowest unprescaled **muon trigger rate** by > ~ 7x

also used in tracking!
NEW SMALL WHEEL ELECTRONICS

- A combination of custom **frontend** and **backend** boards + chips are needed!
- Need to handle the MM and sTGC readout and trigger paths

Micromegas
Frontend Board

Address in Real Time
Data Driver Card

in MM chain

in sTGC + MM chain

Level 1 Data
Driver Card

strip Frontend
Board
Micromegas Readout Path

Micromegas Frontend Board

- ROC
- VMM

VMM digitizes detector signals and sends trigger primitives.

ART

Address in Real Time Data Driver Card

Level 1 Data Driver Card

Trigger Processor

Trigger Path

Readout Path
data handling, control, etc…
Micromegas Readout Path

MM detector

Micromegas Frontend Board

ROC

VMM

buffers and filters data from 8 VMMs to match ATLAS trigger selection

ART

Address in Real Time Data Driver Card

Level 1 Data Driver Card

Trigger Processor

data handling, control, etc…
Micromegas Readout Path

- MM detector
- Micromegas Frontend Board
  - ROC
  - VMM
- ART
- Address in Real Time Data Driver Card
- Trigger Processor
- Level 1 Data Driver Card
- Packs up readout data and sends forward
- Data handling, control, etc…
Micromegas Trigger Path

- Micromegas Frontend Board
  - ROC
  - VMM

- ART
- Address in Real Time Data Driver Card

- Trigger Path
- Readout Path

- Trigger Processor

- Level 1 Data Driver Card

- MM detector

- packages trigger primitives from 32 VMMs and stamps with bunch crossing ID

- data handling, control, etc…
MICROMEGAS TRIGGER PATH

MM detector

Micromegas Frontend Board

ROC  VMM

ART

Address in Real Time Data Driver Card

Trigger Processor

Level 1 Data Driver Card

makes a candidate “track” from trigger primitives

data handling, control, etc…
STGC TRIGGER PATH

Key design principle: use pad signals to filter out which strip signals to send —> data reduction

In Chapter 2 the requirements for the triggering system in the NSW have been defined. The triggering detectors should provide bunch crossing identification, requiring good time resolution, and good angular resolution, better than 1 mrad, for online reconstructed segments, which in turn entails fairly good online spatial resolution. The sTGC detector provides both capabilities as will be demonstrated in this chapter and for this reason is regarded as the main triggering detector in the NSW. It provides also a fair spatial resolution for the off-line tracking that will help the precision tracking, specially during the HL-LHC phase.

4.1 sTGC

The basic Small strip Thin Gap Chamber sTGC structure is shown in Fig. 4.1(a). It consists of a grid of 50 $\mu m$ gold-plated tungsten wires with a 1.8 mm pitch, sandwiched between two cathode planes at a distance of 1.4 mm from the wire plane. The cathode planes are made of a graphite-epoxy mixture with a typical surface resistivity of 100 k$\Omega$/$\square$ sprayed on a 100 $\mu m$ thick G-10 plane, behind which there are on one side strips (that run perpendicular to the wires) and on the other pads (covering large rectangular surfaces), on a 1.6 mm thick PCB with the shielding ground on the opposite side (see Fig. 4.1(b)). The strips have a 3.2 mm pitch, much smaller than the strip pitch of the ATLAS TGC, hence the name ‘Small TGC’ for this technology.

A similar type of structure was used in the past for the OPAL Pole-Tip calorimeter, where 400 detectors were constructed and run for 12 years.

The TGC system, used in the present ATLAS muon end-cap trigger system, has passed a long phase of R&D and testing. The basic detector design for the NSW has two quadruplets 35 cm apart in $z$. Each quadruplet contains four TGC’s, each TGC with pad, wire and strip readout.
STGC TRIGGER PATH

- **pad Frontend Board**
  - VMM
  - ROC
  - TDS
  - Serializes + stamps pad signals with BCID

- **strip Frontend Board**
  - VMM
  - ROC
  - TDS

- **TDS**
- **Pad Trigger**
- **Router**
- **Level 1 Data Driver Card**
- **Trigger Processor**

Data handling, control, etc…
**STGC TRIGGER PATH**

- **Pad Frontend Board**
  - VMM
  - ROC
  - TDS
- **Trigger Processor**
- **Strip Frontend Board**
  - VMM
  - ROC
  - TDS
- **Pad Trigger**
  - Looks for "tower" coincidence of pad signals
- **Router**
- **Level 1 Data Driver Card**

Data handling, control, etc…
STGC TRIGGER PATH

- pad Frontend Board
  - VMM
  - ROC
- TDS
- Pad Trigger
  - Router
  - Level 1 Data Driver Card
  - Trigger Processor

Data handling, control, etc...

gets tower from pad trigger, serializes + sends corresponding strip signals
STGC TRIGGER PATH

pad Frontend Board
  VMM
  ROC
  TDS
Pad Trigger
  packages strip signals and transmits downstream
Router
Level 1 Data Driver Card
Trigger Processor
data handling, control, etc…
STGC TRIGGER PATH

Data flow:
- Pad Frontend Board
  - VMM
  - ROC
- TDS
- Pad Trigger
- Router
- Level 1 Data Driver Card
- Trigger Processor

- Makes a candidate “track” from trigger primitives
- Data handling, control, etc…
STATUS OF ELECTRONICS (HARDWARE)

- **MM Frontend Board**
  - Trigger Processor
  - Mezzanine card will go into pre-production soon, pre-series carrier cards under test,
  - Under review

- **sTGC Frontend Boards**
  - All ASICs
  - Pre-production

- **ART Data Driver Card**
  - Level-1 Data Driver Card
  - Pad Trigger
  - Production

- **Router**
  - Completely tested and delivered
  - Done

Deciding on final producer
MICROMEGAS READOUT CHAIN TESTS

- Electronics have been continuously tested during their development and review chain.
- For the readout path, we have conducted measurements of efficiency, resolution, noise in a 2018 test beam with pions on a full-size chamber (VMM, Frontend Board).

July 2018 Test beam with prototype MMFE8s + VMM3 on a SM2
• Now evaluating a double wedge (1/16 of a MM wheel) which is planned for ATLAS installation for HV stability and electronics noise

• Testing the “full system” with 120 Hz of cosmics

• Have successfully collected data with the VMM —> ROC —> Level-1 Data Driver Card prototype
MICROMEGAS TRIGGER CHAIN TESTS

- For the trigger chain, we developed and debugged the trigger processor firmware by taking cosmic muon data with a prototype chamber, ART Data Driver Card (ADDC) v1 and prototype MM Frontend Boards.
- In the testbeam, the trigger path from VMM to the ADDC v2 with ART was validated.
- Currently developing trigger DAQ with the final ATLAS system to test final trigger processor hardware.
STGC ELECTRONICS TESTS

Test beam - tests of pFEB and sFEB prototypes with VMM, TDS

- sTGC detector efficiencies, charge distributions, resolutions, were also measured in a test beam

- Coincidences between two pads was demonstrated using pad Frontend Board prototype with VMM, TDS

- Efficiency reaches the plateau @ 2.9 kV - slightly higher than desired: non-final (larger) attenuation setting (“pi-network” for VMM high charge operation)

- High (>95%) pad efficiency and a 300V plateau achievable with nominal threshold.

- Timing studies: measured BCID difference for correlated hits between layer 1 & 3 pads.

- 70% correlated pad hits within the same BCID (2/2 coincidence. Where we start!).

- Note earlier offline analysis of readout chain data derived an average of 93% event within 25ns with 3-4 coincidences. Further optimizations needed during commissioning:
  - 3/4 coincidence
  - Bunch clock phase adjustment
  - HV optimization
**STGC ELECTRONICS TESTS**

- Currently testing a large sTGC quadruplet equipped with latest **strip** and **pad** *Frontend Board* prototypes

- Extensive noise tests conducted, e.g. recent tests identified and fixed noise from the on-board DC-DC converters

- Digital readout path with **VMM** and **ROC** also being tested

- **Pad trigger** firmware prototype has been completed
SUMMARY

- NSW + NSW electronics system was designed to handle the challenges of increased instantaneous luminosity at the High Luminosity LHC
  - High radiation environment, high particle rates
  - Right now is an exciting time! Integration ongoing with final chambers and electronics to confirm that the system is functional before ATLAS installation of a wheel planned in 2020
- Thank you!
SOME STGC DESIGN CHALLENGES

- Unique sTGC challenge
- ~45k sTGC pads, ~280k strips in the entire NSW
- Need fine strip granularity without huge amounts of trigger data to process
  - MM sends address of first strip hit in a VMM (strip pitch ~425-450 microns, but 1 VMM covers ~2.7 cm)
  - sTGC pads cover 4+ cm, sTGC strip pitch 3.2 mm
- Solution: select which strip trigger signals should be processed using pad signals
- Basis of electronics design
- using pads to filter which strips are read out reduces data rate by ~ 60-100x
STGC TRIGGER PATH

(1) pad TDS: serializes + stamps pad signals with BCID

(2) pad trigger: looks for “tower” coincidence of pad signals

(3) strip TDS: gets tower from pad trigger, serializes + sends corresponding strip signals

(4) Router: packages strip signals and transmits downstream

(5) TP: makes a candidate “track” from trigger primitives
(1) VMM: digitizes detector signals and sends trigger primitives (64 channels)

(2) ART: packages trigger primitives from 32 VMMs and stamps with bunch crossing ID

(3) ROC: buffers and filters data from 8 VMMs to match ATLAS trigger selection

(3) L1DDC: packs up readout data and sends it forward

(3) TP: makes a candidate “track” from trigger primitives

MM detector

Micromegas Frontend Board

ART

Address in Real Time Data Driver Card

Level 1 Data Driver Card

Trigger Processor

VMM

ROC
1. **2+ million** MM strips need to be read out, ~**45k** sTGC pads, ~**280k** strips for the sTGC
2. Radiation intensive environment
   - Total Ionizing Dose ~ 0.5 Mrad
3. Need low power losses, MM requires 34 kW of power, sTGC requires 14.6 kW of power
4. Everything needs to be **fast** - < 1025 ns for trigger signals to go to ATLAS “Sector Logic”
5. Reuse as many electronics as possible between sTGC and MM
**SPOTLIGHT: VMM FRONT-END ASIC**

- **64 input channels**
- measures **time** and **charge** of signal
- provides fast trigger signals
- used for both MM and sTGC
- radiation hard CMOS technology

### Readout path

- 8-bit fine time information
- 10-bit charge information
- BCID
- channel

### Trigger path

- MM trigger hit: channel address of first strip over threshold
- Pad trigger signal: pulse for Time over Threshold (ToT)
- Strip trigger signal: 6-bit channel peak value

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**VMM - ASIC evolution**

- **VMM1 (2012)**
  - 50 mm²
  - 500k MOSFETs (8k/ch.)
  - mixed-signal
  - 2-phase readout

- **VMM2 (2014)**
  - 115 mm²
  - > 5M MOSFETs (>80k/ch.)
  - planned deep re-design of VMM1
  - higher functionality and complexity
  - continuous fully-digital readout

- **VMM3 (2015-16)**
  - 130 mm²
  - > 6M MOSFETs
  - includes L1 handling and SEU-tolerant logic

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[Link](https://indico.cern.ch/event/299180/session/4/contribution/45)
Readout Controller (ROC) looks for hits matching a desired BCID + packages the hits and transmits at ~ 320 Mb/s.

Address In Real Time (ART) deserializes VMM MM trigger hits, stamps them with the BCID.

Trigger Data Serializer (TDS) serializes VMM data and matches pads and strips.