Development of highly compact digital pixels for the vertex detector of the future e^+e^- collider*

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ABSTRACT

Future electron-positron collider experiments impose stringent requirements on the vertex detectors. It requires to shrink as much as possible the pixel dimensions, while maintaining other key features such as low power consumption and high readout speed. Two in-pixel digitization structures are proposed based on the concept of Depleted Monolithic Active Pixel Sensors (DMAPS).

The two structures with balance between high precision and circuit simplicity guarantee compact pixels, yet with satisfying high signal over noise ratio. Prototype with these two highly compact structures, with a pixel pitch size of 22 μm, has been designed with a 0.18 μm CMOS Image Sensor process. It contains 112×96 pixels, covering an area of 3×3.3 mm^2. The prototype will operate in the rolling-shutter mode, with expected processing speeds of 100ns/row and 80ns/row, respectively, for the two proposed structures.

INTRODUCTION

Precise determination of the charged particle tracks and reconstruction of the primary and displaced decay vertices always drive the need for a high precision vertex detector for future electron-positron collider experiments. Such vertex detector should be constructed with pixel detectors with high spatial resolution and low material budget, and fast readout to keep the detector occupancy low. CMOS pixel sensor (CPS) with pixel level discrimination represents one of the most promising candidates. However, the complexity of in-pixel digital circuit always leads to increased pixel size, which is disfavored to obtain high spatial resolution.

Recent developments have demonstrated that DMAPs could bring in more advantages to charged particle tracking compared to conventional Monolithic Active Pixel Sensors (MAPS), such as lower sensing point equivalent capacitance and higher signal collection efficiency. In this context, we propose two highly compact digital pixel structures, based on the advantageous DMAPs concept, which shall lead to improved spatial resolution.

Selected CMOS technology

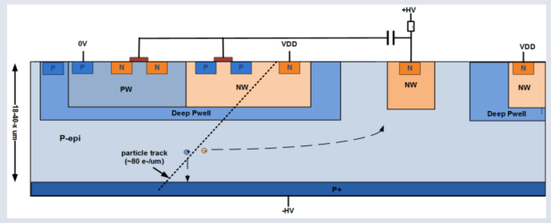


Figure 1: cross-section of the selected quadruple well CMOS process; full CMOS is allowed in-pixel due to the deep Pwell layer.

- Selected 0.18 μm CMOS Imaging Sensor (CIS) technology for R&D, featuring:
  - Quadruple well process, deep PWELL shields NWELL of PMOS: full in-pixel CMOS
  - Thick (18-40 μm) and high resistivity (≥1 kΩ•cm) epitaxial layer: deeper depletion region
  - *Thin gate oxide (<4 nm): robust to total ionizing dose*
  - *6 metal layers: layout benefitted*

In-pixel architecture and signal treatment

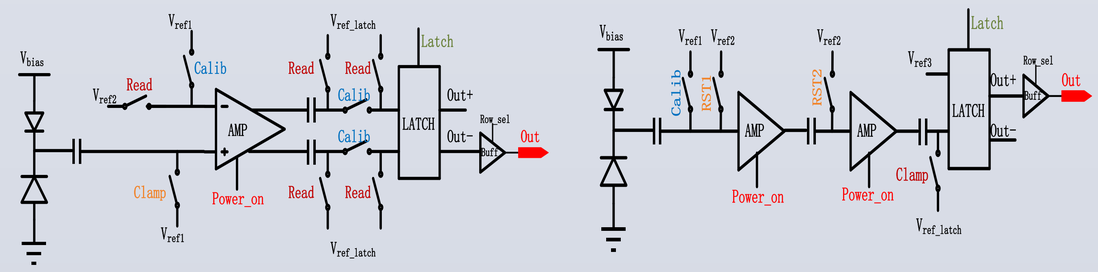


Figure 2: Two pixel structures with differential amplifier + Latch (version 1, left), and two stage Common-Source amplifier +Latch (version 2, right).

- In-pixel Architecture:
  - High-voltage biased N-well/p-epi collection node (V_{bias} up to 10V) AC coupled to the its consecutive electronics.
  - Comparators designed with the Output Offset Storage (OOS) technology;
  - Thresholds adjusted externally for the differential amplifier (Version 1) and the dynamic Latch (Version 2) ;

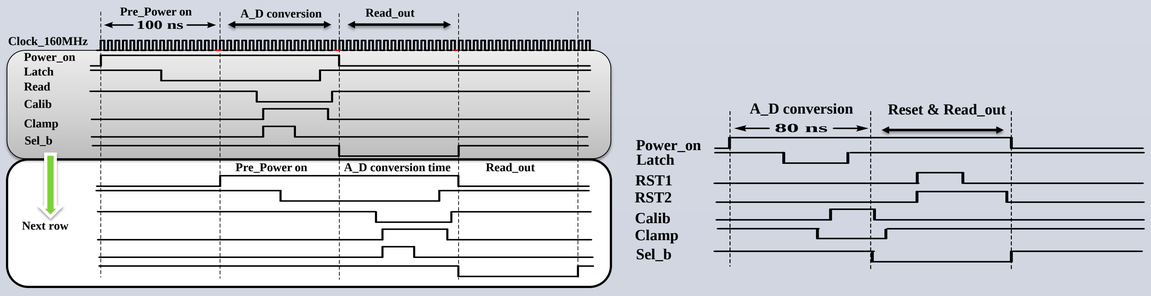


Figure 3: operation timing of the pixel version 1 (left) and version 2 (right).

- Signal and Noise treatment:
  - The useful signal (amount of e^- collected by the diode) is translated into a voltage drop on the diode; AC coupled structure transmit this voltage drop to the following comparators where signal is amplified and digitalized; digital signal is then stored in the Latch and outputted to column through a digital buffer row by row;
  - The offset of the amplifiers are removed by the combined offset cancellation technique;

Collection node

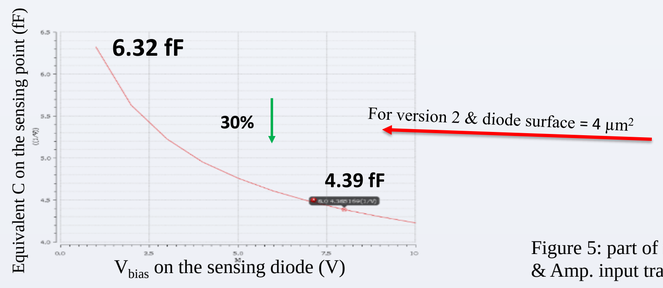


Figure 5: part of the version 2 pixel schematic; a carefully layout & Amp. input transistor size was chosen.

Figure 4: sensing node Equi. C vs V^{bias} (post-layout simulated) for version 2.

Table 1: simulated sensing point Equ. C/Charge to Voltage Factor (CVF) with different diode size/biasing.

	Diode size (μm²)	Diode Bias (V)	Equivalent C, including AMP input transistors (fF)	Parasitic C (fF)	Total sensing point C (fF)	CVF on the sensing diode (μV/e⁻)	CVF after 1st AMP (μV/e⁻)
Version 1	4	8	3.53 fF	0.786 fF	4.316 fF	37	303
Version 2	4	1	6.32 fF	0.670 fF	6.99 fF	22.9	187.3
		8	4.39 fF		5.06	31.7	250
	8	1	8.13 fF		8.80	18.2	143.8
		8	5.37 fF		6.04	26.5	209.4

"Best case"

Noise: transient noise, Amp. offset, latch offset

Differential amplifier in pixel version 1:

- Input DC level: 600 mV
- Biasing current: 3.7 μA
- Gain: 8.3
- RMS noise: 1.962 mV
- Transient noise ENC: ≈ 7 e^- (for best case; highly relaied on the equivalent $C_{sensing\ point}$)

Single-end CS Amplifier in pixel version 2:

- Input DC level: 520 mV
- Gain: 8
- RMS noise: 1.566 mV
- Transient noise ENC: 6.3 e- (for best case)

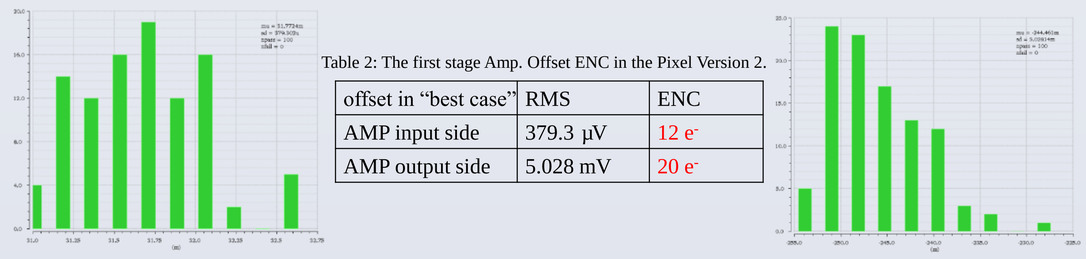


Figure 6: Monte Carlo Simulation of the first stage Amp. Offset (process variation + mismatch) of the pixel version 2: input point (left) and outpoint (right).

Table 2: The first stage Amp. Offset ENC in the Pixel Version 2.

offset in "best case"	RMS	ENC
AMP input side	379.3 μV	12 e^-
AMP output side	5.028 mV	20 e^-

- This offset can be cancelled using the offset cancellation technique.
- The shifted operation DC level of the AMP leads to a gain variation, which contributes to the final Fixed Pattern Noise (FPN).

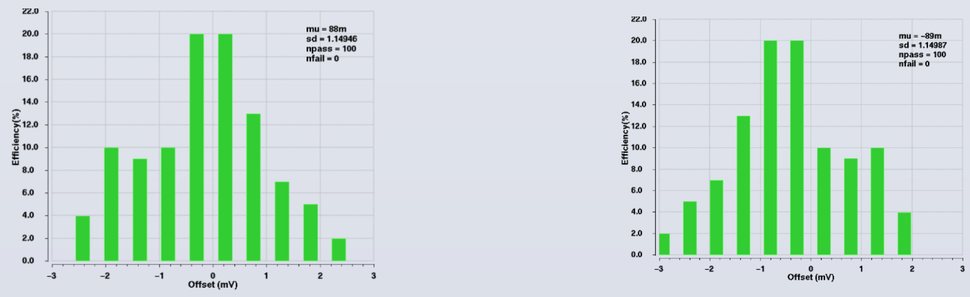
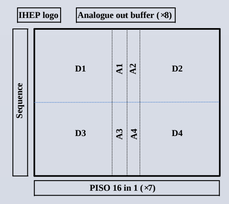


Figure 7: Monte Carlo Simulation of the dynamic Latch offset (process variation + mismatch); raising edge (left) and falling edge (right).

Table 3: latch offset ENC

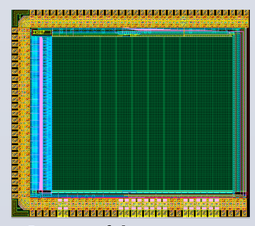
Latch offset in "best case"	RMS	ENC
Version 1	1.15 mV	≈ 4 e^-
Version 2		negligible

Prototype layout and specifications

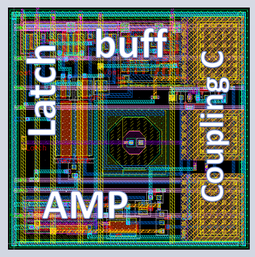


Architecture of the prototype

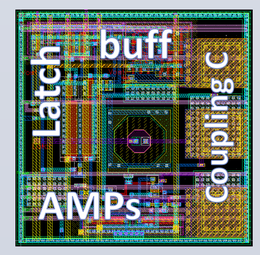
- Some prototype specifications:
  - 0.18 μm CMOS technology;
  - 112×96 square pixels of 22 μm pitch size;
  - 3×3.3 mm^2 layout size;
  - 8 test sub-matrices for two pixel versions, D1-D4 with digital output, A1-A4 with analogue output;
  - 8 Analogue output channels;
  - 16 Column digital data serialized in one LVDS output pair; 7 LVDS pairs in total.
  - Output data speed: 160 MHz
  - 100 ns/80 ns to read one row for the two versions respectively;
  - Noise: 20 – 30 e^- (simulated);
  - Power: ~3.7 μA/pixel



Layout of the prototype: 3×3.3 mm^2



Pixel layout of version1, pitch size = 22μm



Pixel layout of version2, pitch size = 22μm

CONCLUSION AND PERSPECTIVES

With the advantageous concept of depleted CMOS Pixel Sensors, we have proposed two versions of highly compact digital pixels (pitch = 22 μm), which are aimed for the vertex detector of future electron-positron collider experiments. Both versions operate in the rolling-shutter mode and take 100ns and 80ns, respectively, to process one row.

The prototype has been designed with a 0.18 μm CMOS technology and submitted for fabrication in summer 2017. Following-up tests shall deepen our understanding of the performance of the high voltage biased sensing node and in-pixel electronics. Such valuable knowledge shall guide the design of the next generation vertex detector and achieve the desired high spatial resolution.

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