11th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD11) in conjunction with 2nd Workshop on SOI Pixel Detectors (SOIPIX2017) at OIST, Okinawa, Japan

Contribution ID: **60** Type: **POSTER**

Simulation Study of a Pixelated Silicon Sensor on High Resistivity Integrated with Field Effect Transistor

Sunday, 10 December 2017 20:08 (1 minute)

We conceive the position sensitive pixelated silicon detector using the direct illumination of X-ray. Considering the detection efficiency we plan to use the detector for the relatively low energy X-ray. The absorption length of silicon around 10 keV is about 200˜300 um, the active silicon thickness should be twice of the absorption length so that we consider a thickness of 525 μm n-type silicon with high resistivity.
The active volume of the detector is depleted by applying a negative bias voltage to the junction side. The X-ray illumination to the junction side produces electron-hole pairs in the active volume and the produced electrons are wept to the other side of the pixel detector and provides the position information of the conversion point. The cylindrical structure of JFET is employed as the switch to readout the charges accumulated in the pixels. When X-ray is illuminated to the detector, the switches in every pixel are open and the charges are transferred to the drain from the source of the FET. All pixels with one row are read in parallel and the next row is selected by the controlling voltage after finishing the reading one row. For this purpose the double metal structure is needed; the first metal layer for controlling gate voltage and the second metal layer for readout. The polyimide is served as the charge storage capacitor. A thick SiO2 layer between two metal layers separates from each other to insulate the second metal layer.
Figure 1 is a cross-sectional view of the pixelated silicon detector integrated with JFET switch. The deep p-well under the drain is implanted to prevent any signal electrons drifting directly toward the drain. On the other hand the N+ is implanted for the source and drain of the FET. The field shaper is introduced to isolate between pixels. We perform the simulation of the pixelated silicon position detector with JFET switch and present a characteristics of the transistor such as the drain current as a function of the voltage between the source and drain for the gate voltage, as shown in Figs. 2 and 3. We plan to develop the prototype of the detector shown in Fig. 4 on a very high resistivity integrated with an FET switch based on results of the simulations.

Figure 1: https://www.dropbox.com/s/3ocni3slw84o1h4/Figure1.jpg?dl=0
Figure 2: https://www.dropbox.com/s/4zhpc64rzcuqvt7/Figure2.jpg?dl=0
Figure 3: https://www.dropbox.com/s/655cowqne2xix4b/Figure3.jpg?dl=0
Figure 4: https://www.dropbox.com/s/azwjmstnehqrj6l/Figure4.jpg?dl=0

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Session Classification: POSTER

Track Classification: Simulations