Development of a MAPS detector prototype for the BESIII inner tracker upgrade

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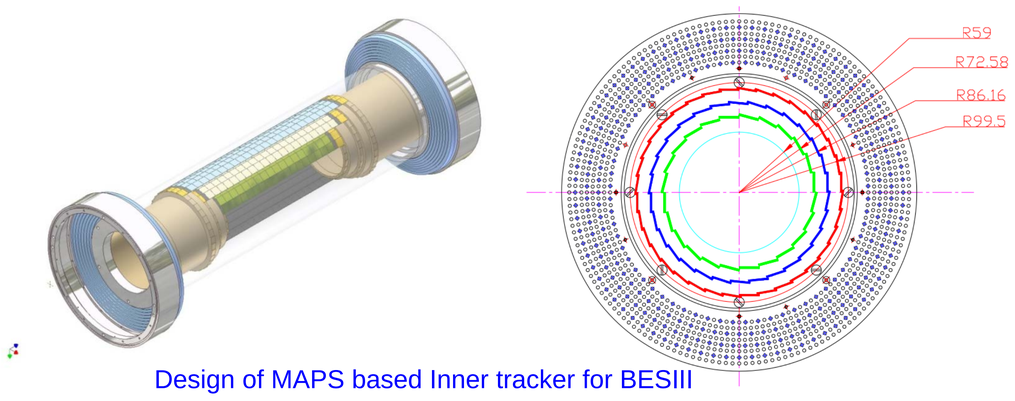
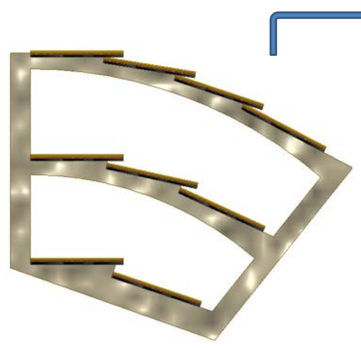
The Beijing Spectrometer III (BESIII) is a high precision detector for the Beijing electron-positron collider II (BEPCII), a high luminosity, multi-bunch e^+ e^- collider running at the tau-charm energy region. The drift chamber (MDC) is the main tracking detector of the BESIII, used for accurate measurements of the position and momentum of charged particles produced in e^+ e^- collisions, and charged particle identification by measuring dE/dx.

After it has been running 8 years, the MDC is suffering from the aging problems due to huge beam induced background, which caused the cell gains dropped dramatically (39% for the first layer cells) , and further more led to decreases of the spatial resolution and the reconstruction efficiency. In order to ensure the inner chamber can be replaced in case of radiation damage, besides building an improved new inner drift chamber, a MAPS (monolithic active pixel sensor) detector prototype, 1/10 coverage of the inner drift chamber, is selected as one of the pre-research schemes, due to its quite attractive features of low material budget, low power consumption and high spatial resolution. The prototype is composed of three layers of MAPS detector modules (ladder), covering 1/10 of the inner chamber in r-φ section, and full length of the inner chamber in z direction. We present the chip test, the design, the assembly and the test of the ladder, as well as the development of the readout electronics.

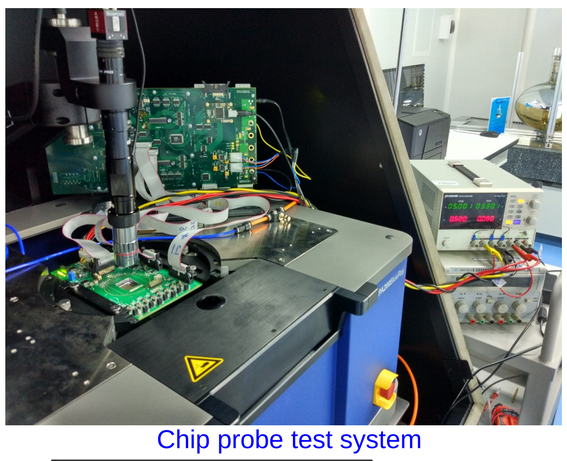


Design of MAPS based Inner tracker for BESIII

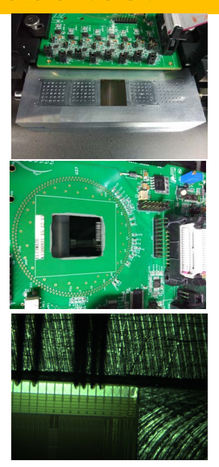


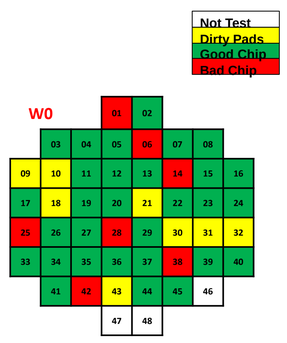
Prototype layout:
- 1/10 Coverage of the inner tracker (~ 720cm^2→180 chips→ about 180M pixels)
- 3 layers of MAPS prototype
- 18 ladders
  r-φ section: 2 , 3 , 4 ladders in each layer
  z direction: 2 sets of ladders in each layer
- 10 Mimosa28 chips / Ladder
  (chips were developed by IPHC, Strasbourg)

Chip probe test

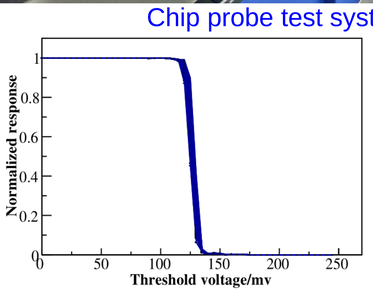


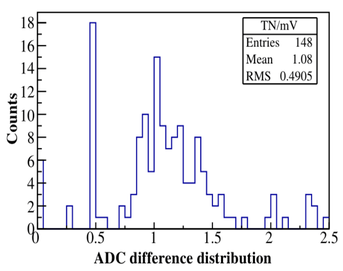
Chip probe test system

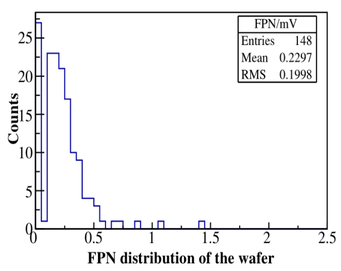




Yield and wafer map



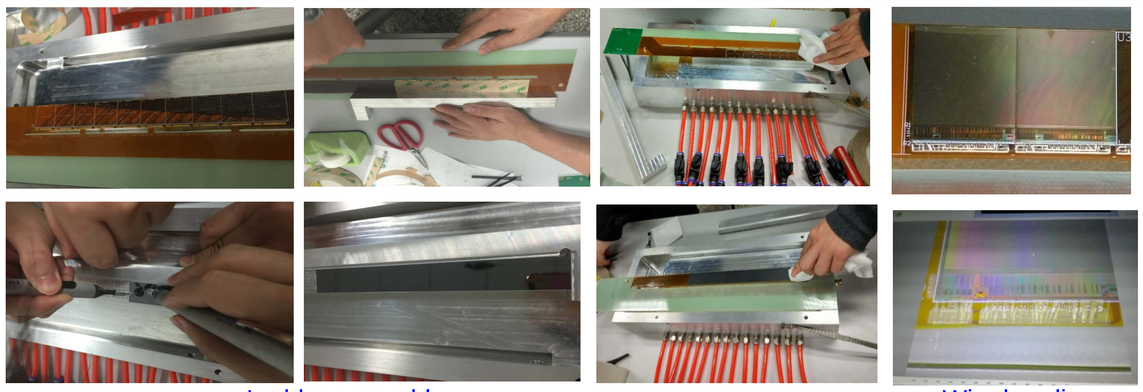




In order to select good chips and provide a reference for the parameter configuration of the chips when they are working in the detector, a MAPS chip probe testing system was set up for the chip functional check and preliminary performance test. With this probe test system, the JTAG communication, the power consumption and the clamping voltage of the chips were test, as well as the data format of the chip output. We also performed the noise level test of the chips and the threshold scan of the discriminators.

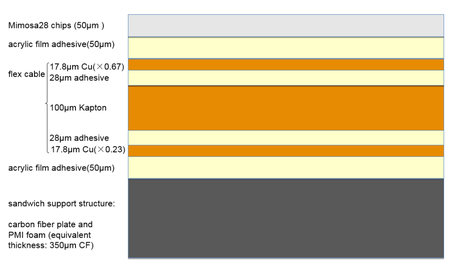
6 wafer chips were tested, and typical chip yield is about 65%.

Ladder assembly



Ladder assembly

Wire bonding



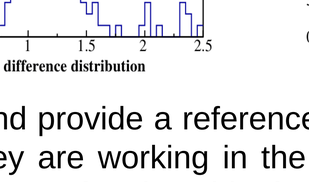
Ladder is the basic structural and functional block of the detector，consisting of 10 Mimosa28 chips thinned to 50μm, a flex cable and a carbon fiber supporter. Pixel chips in a row are connected to the flex cable by wire bonding, and then glued to the carbon fiber support frame, which provides stable mechanical support.

Ladder assembly was operated at a special platform to ensure the location accuracy of the chips, and realize the integration of the chip, the flexible cable and the carbon fiber supporter.

Low material (0.37% X_0 / ladder) , high precision (chip location precision on the ladder: < 10μm) ladders were achieved.

Readout electronics and DAQ

Schematic of readout electronics



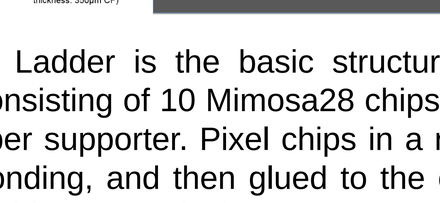
Functional modules of the DAQ

- A distributed electronics readout system has been developed
- Ladder → FCB → Readout Board → Switching → PC
- SiTCP based Gigabit Ethernet (IP core embedded in FPGA) data transmission
- Each electronics module is a network node
- UPD protocol: transfer run control commands and chip/electronics configuration information
- TCP/IP protocol: transfer electronics raw data
- Data readout rate：~700Mb/s

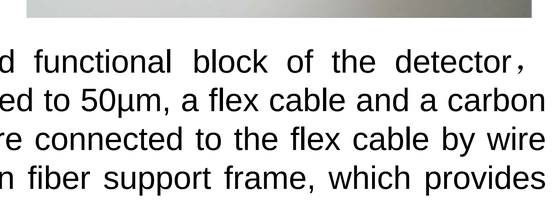
Ladder preliminary test by radiation source

Pixel response test by ^{55}Fe X rays

Cluster size of ^{90}Sr β rays



Crosstalk test between two neighboring chips



Cluster size of ^{55}Fe X rays

The ladders together with the readout electronics were test by ^{55}Fe X rays and ^{90}Sr β rays. The threshold scan, the crosstalk, the imaging performance, temperature effect on the noise level were studied. We also studied the hit reconstruction algorithm.

The test results show that both the ladder and readout electronics work well, and the preliminary results are consistent with the expectation, which meet the requirements of the BESIII inner tracker.

The ladder beam test will be performed next year.