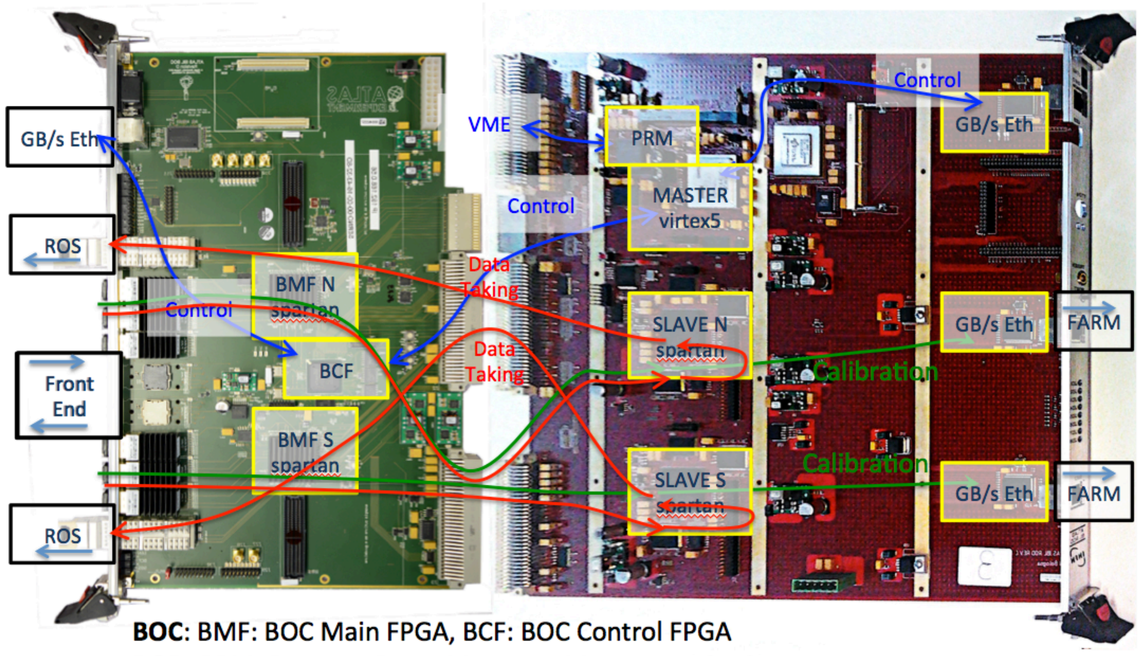
A multi-channel PCI Express readout board for fast readout of large pixel detectors

A. Gabrielli[1,2], F. Alfonsi[1,2], G. Balbi[1], G. D'Amen[1,2]
D. Falchieri[1], N. Giangiacomi[1,2], R. Travaglini[1]
for the ATLAS TDAQ Collaboration
[1]INFN Bologna, [2]Physics and Astronomy Department University of Bologna
alessandro.gabrielli@bo.infn.it

Abstract

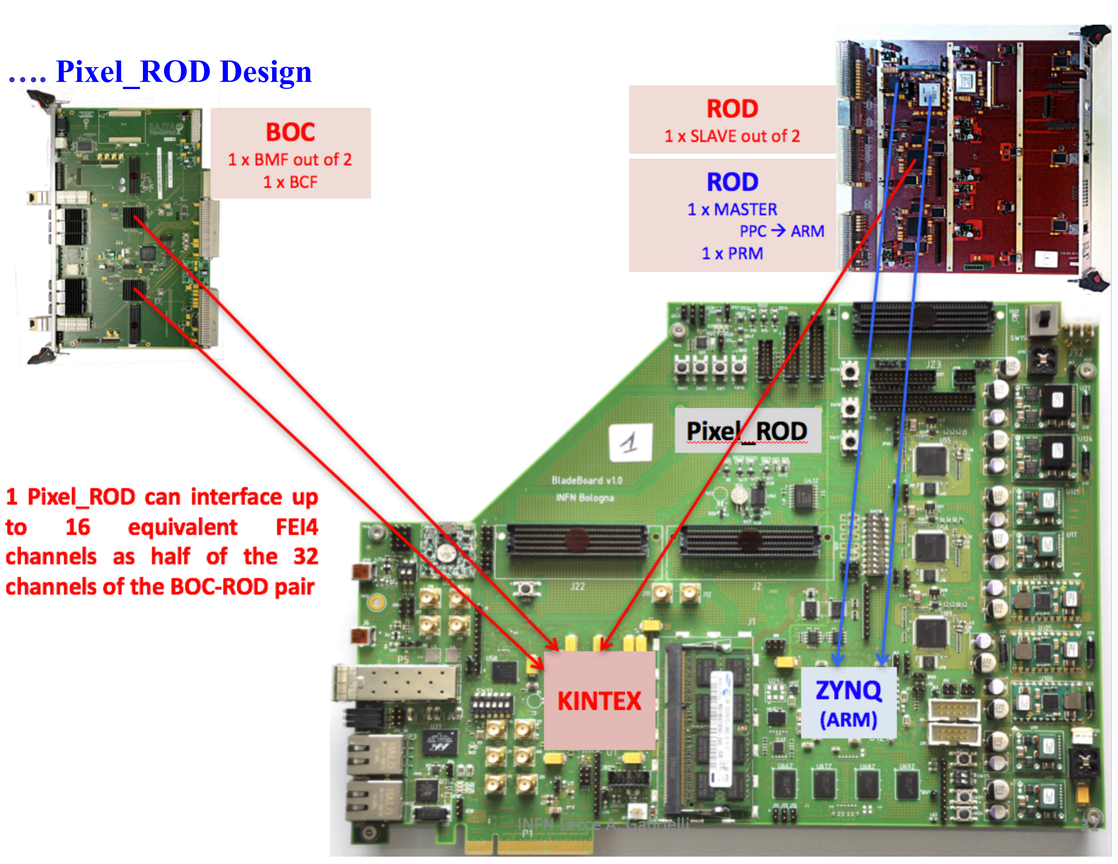
After having commissioned the readout electronics currently implemented in the Insertable B-Layer, Layer 1 and Layer 2 of the ATLAS Pixel Detector (B-Layer and Disk readout electronics in under commissioning), we have designed and fabricated a new readout electronic board looking at the upgrade of the LHC pixel detectors. Two prototypes of a PCI_express Gen 2 board, namely Pixel_ROD featuring all the minimal I/Os and interfaces to address the future front-end electronics, have already been fabricated and tested. The GBTx and RD53A are the first chips that we are going to interface with: preliminary tests are here presented.

From ATLAS IBL, Layer-2, Layer-1, B-Layer, Disks BOC ROD cards to …..



BOC: BMF: BOC Main FPGA, BCF: BOC Control FPGA
ROD: PRM: Program Reset Manager, Master and 2 x Slaves

…. Pixel_ROD Design



1 Pixel_ROD can interface up to 16 equivalent FEI4 channels as half of the 32 channels of the BOC-ROD pair

- 7-series Xilinx® FPGAs
  - ✓Kintex7 XC7K325T-2FFG900C;for trigger and data processing
  - ✓Zynq XC7Z020-1CLG484C with physical dual-core ARM Cortex-A9
- 1 x PCIe Express Gen2 8x-lane (2Gb/s min to the PC memory, up to 10Gb/s)
- 16 x GTX@ 12.5Gb/s on PCIe, SFP, SMA, FMC, Eth
  - ✓1 x SFP 10-Gb/s link (GBTx) tested at 5Gb/s
  - ✓1 x HPC (400-pin) HS diff lines (4 up to 10Gb/s)
  - ✓2 x LPC (160-pin) HS diff lines (1 up to 10Gb/s)
  - ✓DDR3 2GB x 667 MHz (kintex)
  - ✓DDR3 1GB x 667 MHz (Zynq)
  - ✓2 x GB/Eth (1 up to 10Gb/s)
  - ✓2 x USB JTAG
  - ✓2 x SMA (1 up to 10Gb/s)

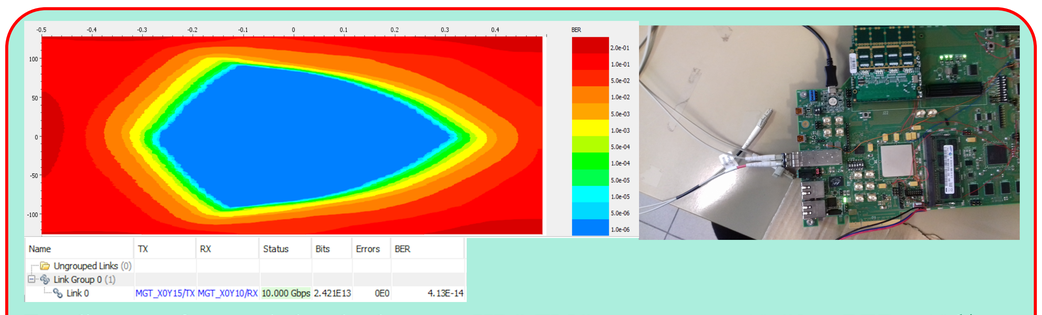
Pixel_ROD IO-Feature

Legenda
Low Pin Count (LPC)
High Pin Count (HPC)
FPGA Mezzanine Card (FMC)
small form-factor pluggable (SFP)
SubMiniature version A (SMA)

Overall Tests

The Figure on the left shows a 21-bit bus, which is used as an inter-FPGA connection to let the Kintex and Zynq communicate, a 64-bit bus to connect the Kintex with an external 2GB DDR3 memory module and four 32-bit buses to connect the Zynq FPGA to 4 external banks of DDR3 memories (1 GB altogether). In particular, the right picture shows a possible data-taking configuration with 5 input optical fibers, 4 via a mezzanine card (FM-S14) connected electrically to a FPGA Mezzanine Card (FMC) connector, and 1 small-form-factor pluggable (SFP) input. All these inputs can read data at a rate up to 12 Gb/s, resulting to a 60Gb/s input bandwidth. The output rate, using an x8 lane PCI Gen2 bus, can run up to 5 GT/s (Giga-Transfer/s that, for 8 lanes and 8b/10b encoding, results to a 4 GB/s output rate). So far, in our laboratory, we have carried out many 2.5 GB/s read-write tests over the PCI Express bus, by connecting the PC motherboard to the Kintex DDR3 memory in Direct Memory Access (DMA) mode, bypassing the Kintex transceivers.

Transceiver and PCI Tests	Elcetrical/Optical (Fibers)	Elcetrical/Optical (Fibers)	Electrical (SMA)	Electrical (Ethernet)	PCI Gen 2
Input Channels	4 x HPC + 1 x SFP	1 x LPC	1	1	8
Output Channels	4 x HPC + 1 x SFP	1 x LPC	1	1	8
Max Bandwidth	12.5 Gb/s	12.5 Gb/s	12.5 Gb/s	12.5 Gb/s	4.0 GB/s
Tested Bandwidth	**12.5 Gb/s**	-	**12.5 Gb/s**	**1 Gb/s**	**2.5 GB/s**
FELIX GBT Mode	**4.8** Gb/s	-	-	-	-
FELIX Full Mode	**9.6** Gb/s	-	-	-	-
Aurora 64b/66b	x1 / x4 @ **10** Gb/s	-	-	-	-



Eye diagram of a generic loopback test on **HPC FMC** connector at: **10 Gb/s, BER ≈ 10^{-14}**

Test in generic loopback on **SFP** connector at 4.8 Gb/s with **BER ≈ 10^{-12}**

AURORA (64b/66b) Protocol Tests

** **Simplex mode: (4 lanes at 1.28 Gb/s)**
-- loopback communication on the **HPC FMC** connector

** **Duplex Mode: (1 lane at 10 Gb/s)**
-- loopback communication on the **HPC FMC** connector

Pixel_ROD to Mini_FELIX tests

** **GBT mode: (4.8 Gb/s)**
-- communication From Pixel_ROD to FELIX
-- communication From FELIX to Pixel_ROD

** **FELIX Full Mode : (9.6 Gb/s): 100 GByte data transmitted in 100 s**
-- ***reliable*** communication From Pixel_ROD to FELIX

PCI_express (8x Gen. 2) Tests

Tests performed at 2.5 GB/s with 8b/10b encoding (8 hours), final BER ≤ 10^{-14}

Summary

Over the last years the ATLAS Pixel Detector has been upgraded in terms of sensors and readout electronics. The challenge of upgrading the readout electronics for the huge matrices of pixel detectors has led us to design and fabricate a PCI_express board (Pixel-ROD) with all the necessary I/Os looking at the performance to interface with the current and future front end electronic chains. For example, the intention is to interface with the GBT and RD53A chips that will be used for the LHC upgrade. In particular the GBTx communication has recently been optically interfaced at a rate of 10 Gb/s with a mini-FELIX card. Other tests have been physically carried out at a rate of 4.8 GB/s using the 64b/66b Aurora protocol. We are building a demonstrator tool able to emulate a data-taking of physical streams, by connecting together many Pixel-ROD boards. Also, an 8-hour PCI-express DMA readout has been proved towards a PC mother board, with an overall bit-error-rate less than 10^{-15}. The Pixel-ROD board features a 8x PCI express Gen 2 bus and two Xilinx FPGAs: the Kintex7 XC7K325T-2FFG900C and the Zynq XC7Z020-1CLG484C with an embedded physical dual-core ARM Cortex-A9 processor. The Kintex device features16 transceivers nominally running at up to 12 Gb/s. These 16 GTx are connected to different types of physical ports: 8 PCI_express, 4 HPC FMC, 1 LPC FMC, 1 SMA, 1 SFP and 1 Gb-Ethernet port. In addition the two Xilinx devices feature DDR3 external memories tested with read-write cycles at 667 MHz. We are proposing the board as a tool to test, qualify and read out the recent chips and/or channels under development to interface new generation of pixel detectors, besides those for the LHC upgrade. We are planning to extend the use of the board within other CERN-based collaborations.
Eventually the Pixel_ROD has interfaced with a mini-FELIX card (Xilinx VC709) by establishing a communication via either GBT (4.8 Gb/s) or Full_Mode (9.6 Gb/s) protocol. For both configurations, the clock (TTC clock) was recovered from the data stream (using the CPLL and QPLL of the GTx transceiver) and was propagated to all the synchronous components of the Pixel_ROD, primarily to the Zynq as master and to the Kintex as slave component, creating a synchronous data acquisition system.