A Monolithic Active Pixel Sensor prototype for the CEPC vertex detector

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ABSTRACT

With the R&D activities for the CEPC vertex detector, we have developed a CMOS pixel sensor prototype in the TowerJazz 180 nm CMOS Image Sensor (CIS) process. The design goals include a high spatial resolution, a fast readout and a low power consumption. To achieve a highly compact pixel, two different binary front-end circuits with low power consumption have been implemented. A new architecture of asynchronous zero-suppression data-driven readout inside the matrix has been designed. The prototype contains 128 rows and 64 columns with each pixel of 25 μm. The readout speed is 40MHz and the readout time is estimated to be a few microsecond. The data is encoded and read out at 1:2 Gbps using a SPI interface.

A brief introduction on the project

The Circular Electron Positron Collider (CEPC) is proposed by the Chinese high energy physics community in 2012. The CEPC machine will be constructed in a tunnel with a circumference of ~100 km. The machine is expected to operate at the center-of-mass energy of ~240 GeV, with an instantaneous luminosity of 2 × 10³⁴ cm⁻²·s⁻¹. CEPC will serve as a Higgs factory to measure the Higgs properties precisely. This machine could be later upgraded to a proton-proton collider with an unprecedented center-of-mass energy of ~100 TeV. The machine will offer a unique opportunity for direct searches for New Physics in the high-energy range far beyond LHC reach.

CEPC Vertex detector requirements

- Spatial resolution near the IP better than 3 μm → high granularity
- Material budget below 0.15% X₀-layer → Low power dissipation, thinned sensor
- Pixel occupancy not exceeding 1% → High granularity and/or short readout time
- Estimated radiation tolerance: ~2.5 MRad/week (TID) and ~10¹³ 1MeV nₑ/ cm²/year (NIEL)

Digital pixel design

- Small pixel size of 25 μm × 25 μm
- Analog front-end and discriminator continuously active
- Digital pixel circuitry with one hit storage registers
- Two versions of front-end implemented to achieve small area and low power

- Front-end version-I:
  - Same structure as ALPDE chip (for ALICE ITS upgrade), with different parameters
  - Peaking time < 1 μs, pulse duration < 3 μs,
    - with power cons. of 110 nW/pixel
  - ENC: ~8 e⁻
  - Area: ~25 × 9.3 μm²

- Front-end version-II:
  - CSA based front-end, with a very low feedback capacitance
  - Peaking time < 1 μs, with power cons. of 50 nW/pixel
  - ENC: ~24 e⁻
  - Area: ~25 × 9.3 μm²

Pixel array readout

- Data driven → very low power consumption
- Zero-suppression readout architecture: OR-gate chain & Address Encoder and Reset Decoder (AERD) combination → for highly compact pixel & fast readout & low power
  - OR-gate chain inside a super pixel (8×8 pixels) to do the zero-suppression, two dimension projection (ADDRX & ADDR Y) to identify the hit pixel → save in-pixel logic and address lines area
  - AERD between one column of the super pixels → save power and readout time

Digital pixel design

- Die size: 3.2 × 3.7 mm²
- 128 × 64 pixels with size of 25 μm × 25 μm, with two different versions of front-end
- Readout speed: 40 MHz/pixel → readout time less than a few μs
- Matrix power: < 20 mW/cm²
- No Memory in the periphery, data reads out through a 1.2 Gbps serial output port with differential signaling
- All PADS custom designed, to allow applying a reverse bias voltage on the substrate

CONCLUSION AND PERSPECTIVES

We have designed a CMOS pixel sensor prototype in a 180 nm process for the R&D of the CEPC vertex detector. To achieve a very small pixel size together with a low integration time and a low power consumption, we have proposed and implemented a new data-driven readout architecture. The matrix readout combines the traditional OR-gate chain inside a super pixel with a priority tree between the super pixel. Two different front-end structures have been designed targeting an ultra-low power and a highly compact layout. The on-chip DACs and LVDS transceivers are also implemented.

The prototype has been fabricated and returned from the foundry recently. The test system is being developed and the prototype is expected to be characterized in the early 2018.