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## A Monolithic Active Pixel Sensor prototype for the CEPC vertex detector

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The Circular Electron Positron Collider (CEPC) is proposed as a Higgs factory to measure the Higgs boson precisely. The CEPC vertex detector requires a low material budget, a high spatial resolution, a fast readout and a low power consumption. Monolithic Active Pixel Sensor (MAPS) will be the most promising candidate which can most likely satisfy the requirements simultaneously. For the R&D of the CEPC vertex detector, we have developed a prototype MIC4 in the Towerjazz 180 nm CMOS Image Sensor (CIS) process. Two different binary front-end circuits have been implemented inside MIC4 to study their different performances. The power consumption of the front-end is about 35nW/pixel. A new architecture of asynchronous zero-suppression data-driven readout inside the matrix has been implemented. The matrix contains 128 rows and 64 columns with a small pixel pitch of 25  $\mu\text{m}$ . The readout speed is 40MHz/hit and the readout time depends on the hit occupancy. The data is encoded and read out at 1.2Gbps using a SPI interface. The on chip DACs and LVDS transceivers are also implemented. This work presents the design of the prototype, which is in the progress of fabrication and expected to be characterized in the early 2018.

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