A 3.2 Gbps Serial Link Transmitter in 0.18 μm CMOS Technology for CMOS Monolithic Active Pixel Sensors Application

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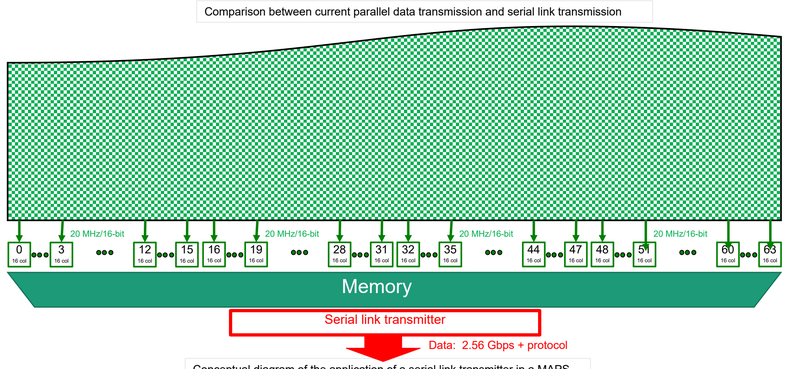
1. Motivation

- CMOS monolithic active pixel sensors(MAPS) for future subatomic physics experiments require integration of high-speed serial data link due to
  - Increasing hit-density
  - Low material budget
- We developed a 3.2 Gbps serial link transmitter for MAPS application

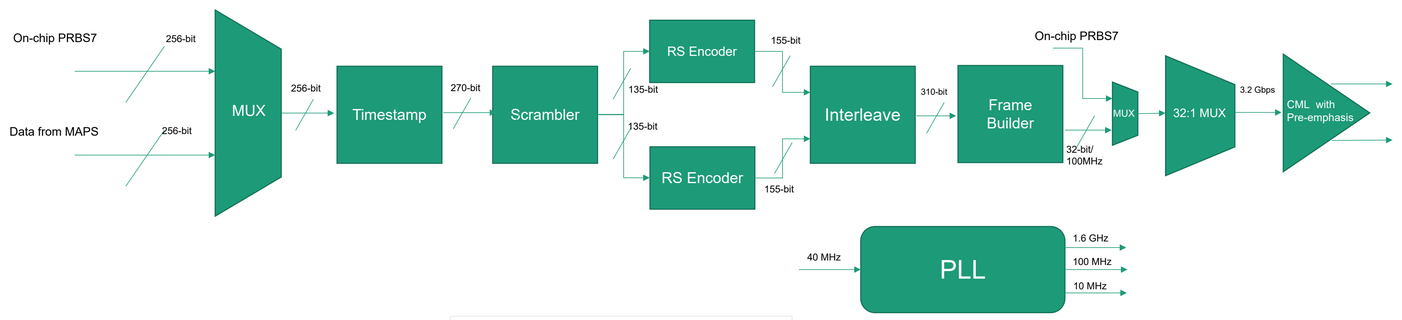
	Current Parallel Data Transmission(8 X 320 MBps, LVDS)	Serial Data Transmission
Cables	18 (16 of them for data and other 2 for clock)	2
Clock Skew	Yes	No
Error Correction	No error correction	Up to 20 bits in a frame

Comparison between current parallel data transmission and serial link transmission



Conceptual diagram of the application of a serial link transmitter in a MAPS

2.Architecture

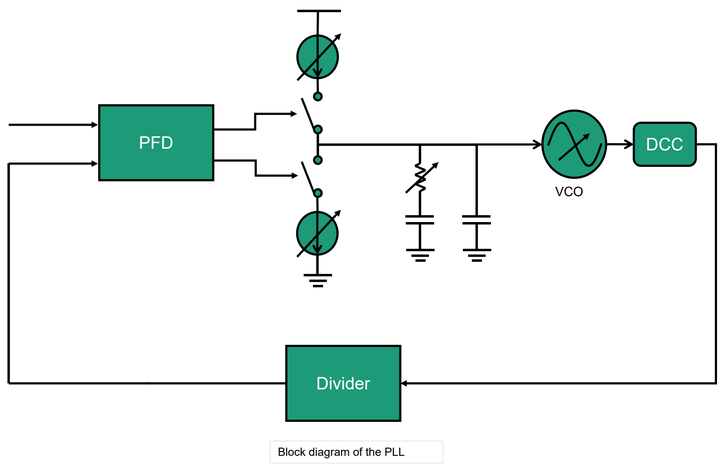


Block diagram of the proposed serial link transmitter

- 256-bit raw data at 10 MHz
- 14-bit timestamp
- Scrambler defined by polynomial $x^{58}+x^{39}+1$
- Interleaved Reed-Solomon (31,27) FEC encoder, correct burst bits up to 20 bits
- Digital circuits are fully triplicated to tolerate SEU
- Half-rate serialization scheme
- 1.6 GHz clock generated with duty-cycle correction
- 32:1 multiplexer with 5-stage binary-tree structure
- CML driver with 3-tap pre-emphasis
- On-chip PRBS-7 for testability

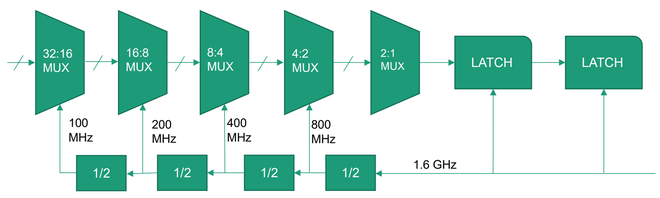
Frame definition

3. The PLL and the serializer

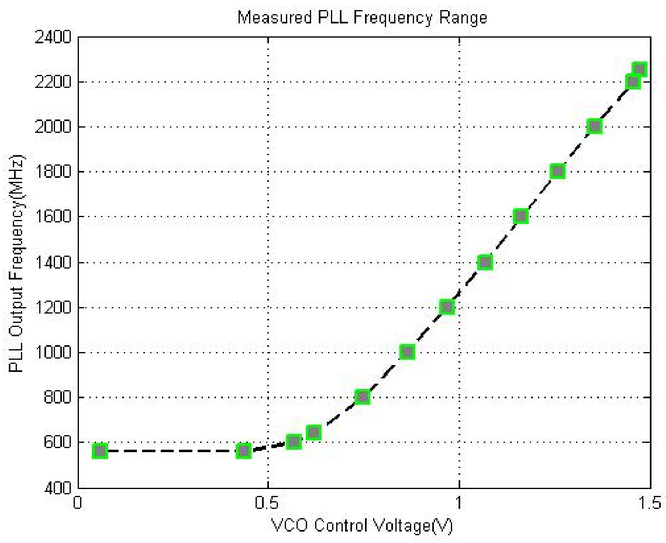


Block diagram of the PLL

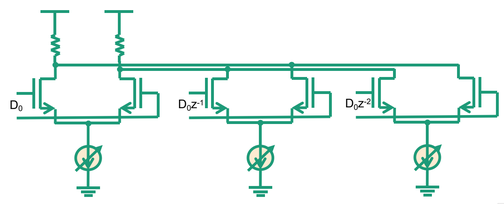
- Charge-pump PLL for clock multiplying by a factor of 40
- Loop bandwidth is programmable to ease in-band noise and out-band noise trade-off
- 4-stage ring voltage-controlled oscillator covers frequency ranging from 0.6 GHz to 2.2 GHz
- Duty-cycle correction circuit minimizes duty-cycle distortion(DCD)
- The divider is fully triplicated to tolerate SEU
- 5-stage binary-tree structure based serializer



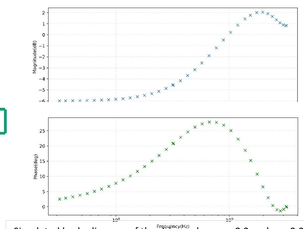
5-stage binary tree serializer



4. The Driver with Pre-emphasis

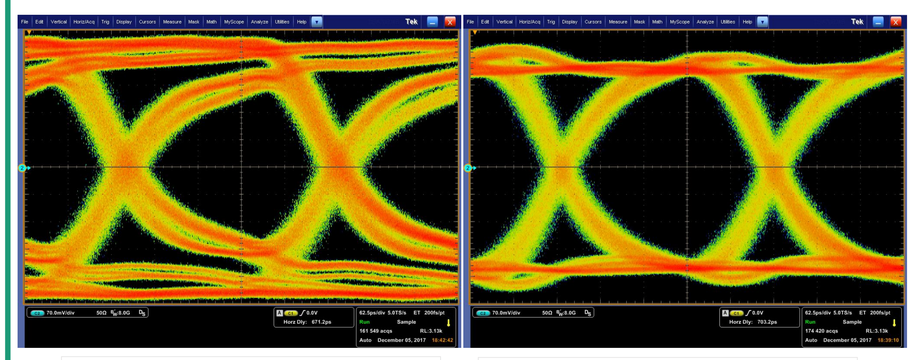


Simplified schematic of the CML driver with pre-emphasis



Simulated bode diagram of the driver when a_0=-0.3 and a_1=-0.2. A 10 dB peaking could be obtained

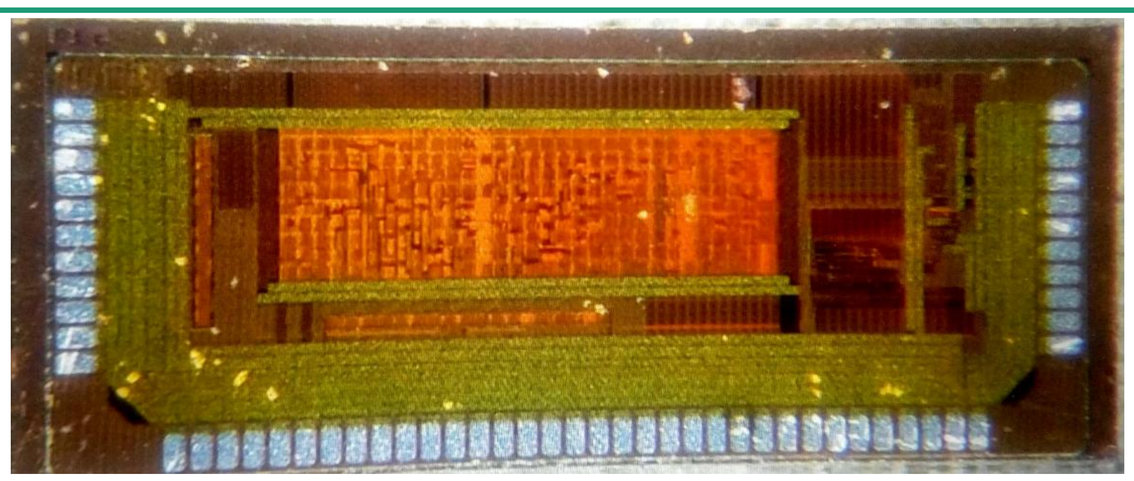
- Pre-emphasis was implemented in the driver because low mass cables are preferred in the system
- Output CML driver realizes programmable 3-tap pre-emphasis
  - Z-domain transfer function: $Y(z^{-1}) = I_o(1 + a_0 z^{-1} + a_1 z^{-2})$
- 2 delayed copies of data are generated by the serializer



Measured eye diagram including the on-chip PRBS 7 generator, the serializer, and the driver with a 1.5 meter cable, pre-emphasis off

Measured eye diagram including the on-chip PRBS 7 generator, the serializer, and the driver with a 1.5 meter cable, a_0=-0.2

4. Preliminary Results Summary



Micrograph of the transmitter prototype chip

- The transmitter was fabricated in TowerJazz 0.18 um CMOS CIS process.
- Core area is 2360 um X 760 um.
- The transmitter was directly wire-bonded to a printed circuits board for testing.
- Measurement shows the PLL works at 1.6 GHz with enough margin.
- The serializer and the CML driver with pre-emphasis function as expected.
- Total jitter is about 57 ps.
- A total power consumption of around 132 mW under a 1.8 V supply was observed.

5. Conclusion and outlook

We developed a serial link transmitter for CMOS pixel sensors application in towerJazz 0.18 μm CMOS CIS Technology. The transmitter includes a Reed-Solomon encoder, a PLL, a serializer and a Current Mode Logic (CML) driver with pre-emphasis. Functionalities of analog circuits is preliminarily verified by measurement.
This is the first time that a multi-Gbps serial link transmitter is developed as a high-reliability, low-mass, low-power consumption data transmission solution for MAPS. Comprehensive measurement will be carried out and the results will be reported in the final paper. We aim to integrate it into a CMOS sensor chip later.

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