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A 3.2 Gbps Serial Link Transmitter in 0.18 µm CMOS Technology for CMOS Monolithic Active Pixel Sensors Application

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CMOS monolithic active pixel sensors (MAPS) with high-speed serial data links are demanded by numerous future subatomic physics experiments due to the increasing hit density, low material budget requirements. A MAPS integrated a serial link transmitter meets requirement of this application due to its saving cables/connectors and high reliability in contrast to with a parallel data link. We present a 3.2 Gbps serial link transmitter designed for CMOS MAPS application in 0.18 µm CMOS Technology. The transmitter includes a PLL for clock generation, a digital interface block with Reed-Solomon encoder, and a CML driver with pre-emphasis. We also considered radiation tolerance in the design.

The PLL generates a 1.6 GHz clock from a 40 MHz reference clock. A ring Voltage-Controlled Oscillator (VCO) is employed due to its area efficiency. The charge pump current and the loop filter resistor are programmable to minimize the jitter. Since the half-rate serializer structure we used is sensitive to the duty cycle of clock signal, a duty-cycle correction circuit is adopted to alleviate Duty-Cycle Distortion (DCD). The clock divider in the PLL loop is triplicated to resist SEU.

The digital interface block combines the user data into 320-bit data frame in which there are a 10-bit frame head, 256-bit pixel data, a 14-bit timestamp and 40-bit overhead. The 256-bit raw data is received at 10 MHz from MAPS. The data with timestamp is scrambled and then encoded with Reed-Solomon algorithm. One can recover SEU up to 20 consecutive bit in a frame, benefiting from this RS(31,27) encoding in our scheme, which is suitable for burst errors in subatomic experiments. The digital interface block delivers data with 32-bit width at frequency of 100 MHz to the serializer. The digital interface block is fully triplicated because that the feedbacks in the scrambler and the encoder are sensitive to errors induced by SEU.

The serializer is a 32:1 multiplexer with 5-stage binary-tree structure. The serializer provides a complementary signal and its two copies of one and two clock period delay to the CML driver.

The CML driver realizes pre-emphasis with one main driver and two post-taps. The output swing and the tap coefficient is programmable. The maximum swing when all the pre-emphasis are off is 800 mV across two 50 Ω internal termination resistors.

The 3.2 Gbps serial link transmitter is designed in a 0.18 µm CMOS technology. The functionalities are verified by simulation. The transmitter consumes 174 mW from a 1.8 V power supply. The prototype have been submitted in May. We expect to report the measurement results on the conference.

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