Two low-power optical data transmission ASICs for the ATLAS liquid argon calorimeter readout upgrade

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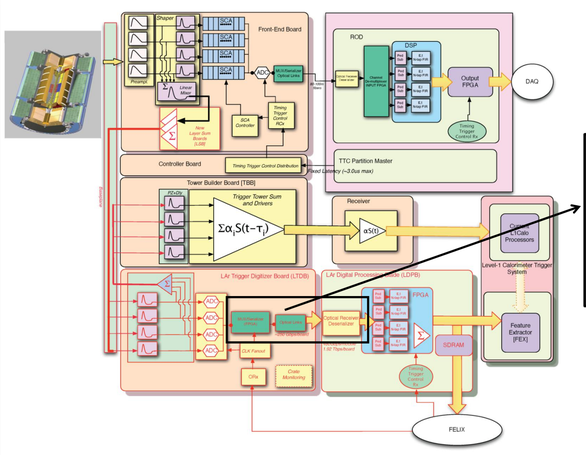
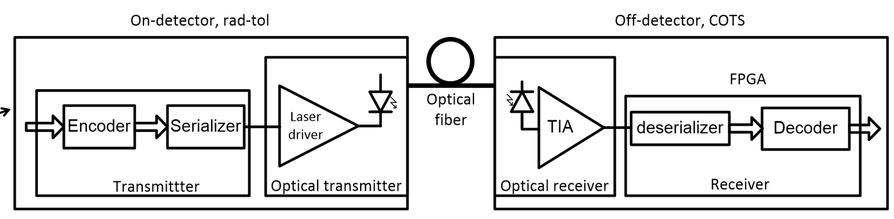
Introduction

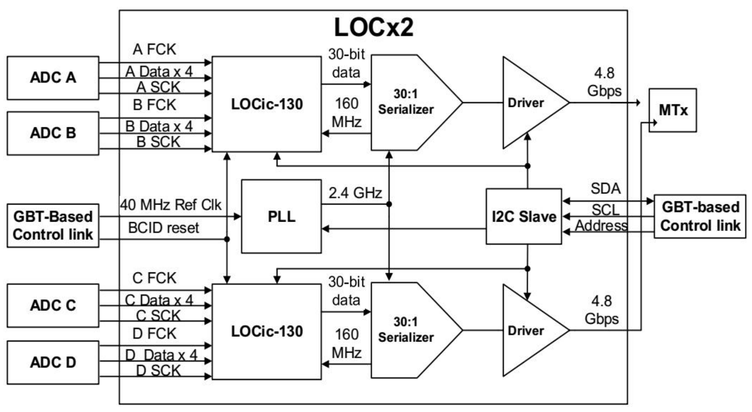




The block diagram of the optical link in ATLAS LAr trigger phase-I update

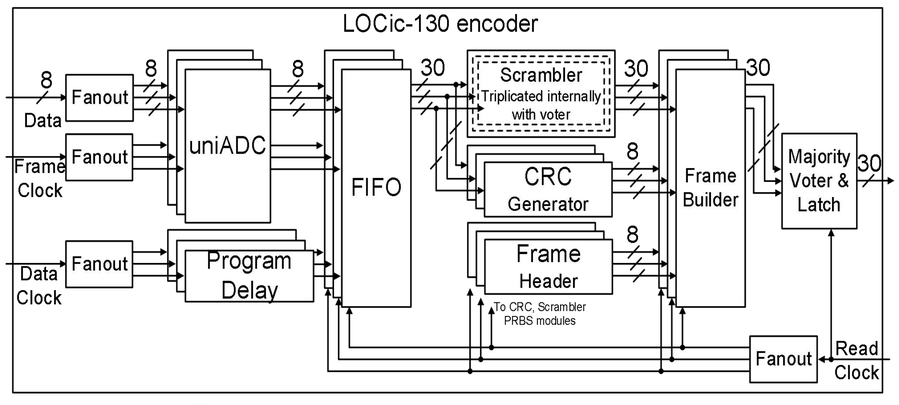
- The ATLAS Liquid Argon calorimeter (LAr) Phase-I trigger upgrade calls for a data transmission rate of 204.8 Gbps for each front-end board (LTDB) [1].
- Serializer and VCSEL driver ASICs are needed for the front-end optical readout due to the demand on data bandwidth, high channel density, low power consumption, low transmission latency and radiation tolerance.
- The baseline ASICs are the serializer LOCx2 and the VCSEL driver LOCId. They are designed in a 0.25-um Silicon-on-Sapphire (SoS) CMOS technology and consume 950 mW and 217 mW, respectively.
- Based on a 130-nm CMOS technology, we decide to exercise our expertise to design two pin-to-pin backup ASICs, LOCx2-130 and LOCId-130.
- LOCx2-130 is a two-channal transmitter ASIC. Each channel receives data from the upstream ADCs [2], encodes the data, and outputs them in serial at a speed of 4.8 Gbps.
- LOCId-130 is a dual-channel VCSEL driver ASIC and each channel operates at 5 Gbps.
- The power consumption of LOCx2-130 and LOCId-130 are 440 mW and 112 mW, respectively.

The design of LOCx2-130 and LOCId-130



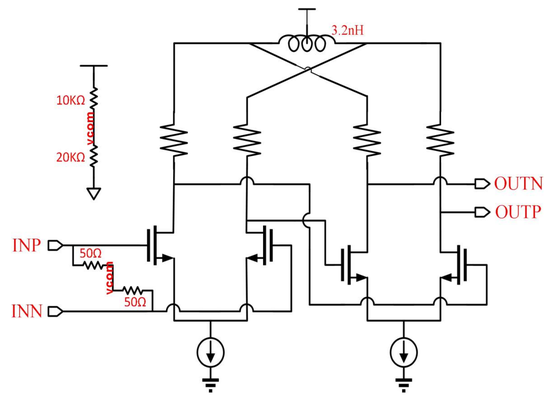
The block diagram of LOCx2-130 ASIC

- The ASIC uses a custom line code called LOCic.
- Each LOCx2-130 data frame has 120 bits, including 8-bit frame header, 96-bit payload and 16-bit frame trailer in data mode or 112-bit payload in calibration mode.
- 12-bit BCID information is embedded in the frame header.
- Each serializer channel of LOCx2-130 takes the digitized data of eight analog signals from two ASIC ADCs or one ADS5272 or one ADS5294.
- LOCx2-130 is composed of two encoders, two 30:1 serializers, two drivers, a shared PLL, and an I2C slave.



The block diagram of LOCic-130 encoder

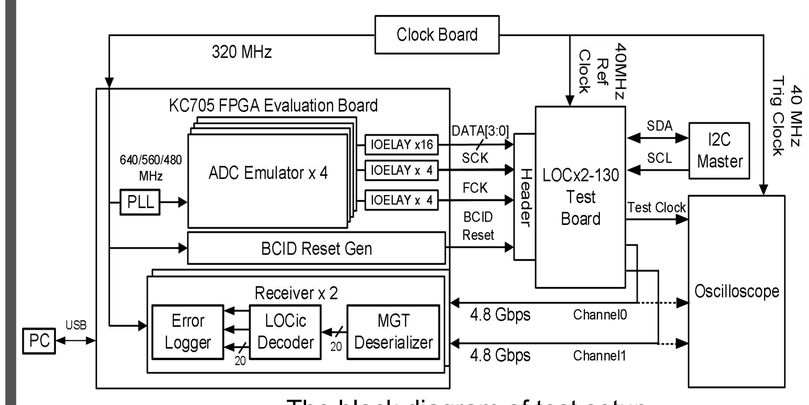
- The encoder is composed of an ADC interface, a synchronous FIFO, a PRBS generator, a CRC generator, a scrambler, and a frame builder.
- The Verilog code of LOCic-130 is triplicated. Modules that have pipeline structure without internal feedback like FIFO and Frame Builder or modules that do have the internal feedback but are reset periodically like the CRC and the Frame Header are simply instantiated by three times as triple redundancy.
- The Scrambler however, has feedback and no reset mechanism, is triplicated internally with the voter added at the input of every D flip-flop to eliminate errors, therefore, the error will not be latched in the D flip-flop and cause permanent malfunction.



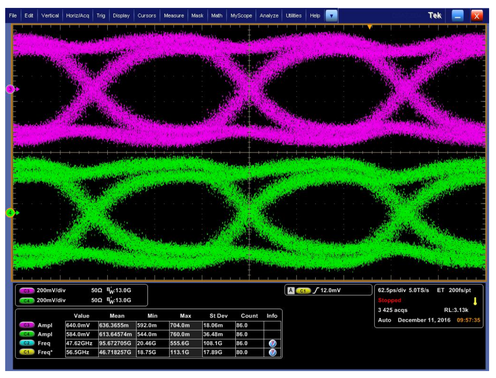
The structure of the limiting amplifier in LOCId-130

- The LOCId-130 is composed of an analog core and an I2C slave module. The analog core of LOCId-130 has two parts: a limiting amplifier (LA) and a high-current differential driver.
- The minimum input signal is assumed to be 200 mVpp. The output is 8-mA modulation current CML. At the output both modulation and bias currents are programmable via I2C.
- The LA adopts a two-stage differential amplifier with a 3.2-nH peaking inductor shared between these two stages, boosting the bandwidth to 3.5 GHz. The LA gain is 14 dB, amplifying input signal from 200 mVpp to 1 Vpp.

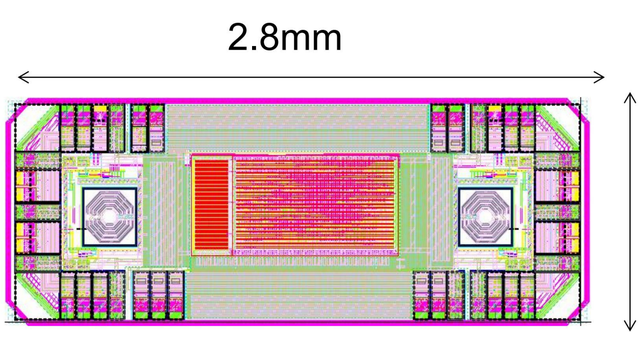
The test and simulation results



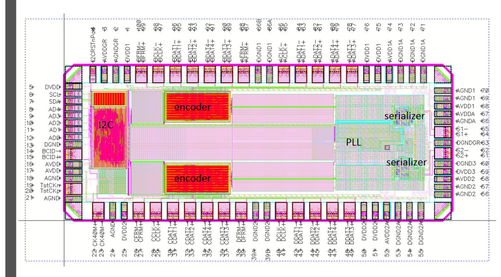
The block diagram of test setup



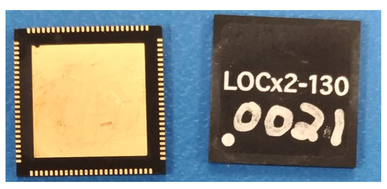
The eye diagram of LOCx2-130 output at 4.8 Gbps



Layout of the LOCId-130 ASIC



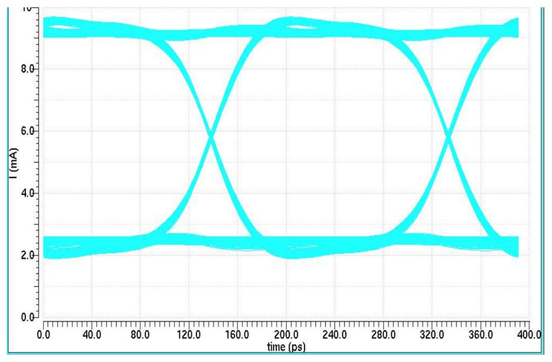
Layout of the LOCx2-130 ASIC



QFN packaged LOCx2-130 ASIC

Serial data output rise time	78.4 ps
Serial data output fall time	78.4 ps
Serial data output deterministic jitter	28.1 ps
Serial data output random jitter	2.3 ps (RMS)
Serial data output total jitter	52.1 ps (peak-peak)
Serial data output amplitude	300 mV (peak-peak)
Serial data output BER	< 10^{-12}
Total power consumption of LOCx2-130	440mW
Total LOCx2-130 latency	34.4~40.7ns

LOCx2-130 measurment



Simulation eye diagrams of LOCId-130 laser current at 5 Gpbs

Conclusion and outlook

- An serializer LOCx2-130 and an VCSEL driver LOCId-130 ASICs are designed for the ATLAS LAr Calorimeter trigger upgrade.
- LOCx2-130 consists of two channels, each channel transmits serial data at 4.8 Gbps with a latency of less than 40.7 ns. The power consumption is 440 mW.
- LOCId-130 has two channels and each channel operates at 5 Gbps. The power consumption is 112 mW.

Acknowledgments

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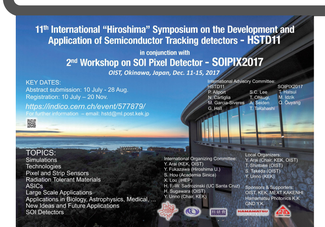
References

[1] ATLAS Collaboration, *ATLAS liquid argon calorimeter Phase-I upgrade technical design report*, CERN-LHCC-2013-017 and ATLAS-TDR-022, September 20, 2013.
[2] J. Kuppambatti, et al, A radiation-hard dual channel 4-bit pipeline for a 12-bit 40 MS/s ADC prototype with extended dynamic range for the ATLAS Liquid Argon Calorimeter readout electronics upgrade at the CERN LHC, 2013 JINST 8 P09008



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