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Two low-power optical data transmission ASICs for the ATLAS liquid argon calorimeter readout upgrade

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A serializer ASIC and a VCSEL driver ASIC are needed for the front-end optical data transmission in the ATLAS liquid argon calorimeter readout phase-I upgrade. The baseline ASICs are the serializer LOCx2 and the VCSEL driver LOCld. They are designed in a 0.25-um Silicon-on-Sapphire (SoS) CMOS technology and consume 950 mW and 217 mW, respectively. Based on a 130-nm CMOS technology, we decide to exercise our expertise to design two pin-to-pin backup ASICs, LOCx2-130 and LOCld-130. Their power consumptions are about half of those of their counterparts. We present the design and test result of LOCx2-130 and the design of LOCld-130.

LOCx2-130 is a low-power, low-latency, dual-channel serializer ASIC and each channel operates at 4.8 Gbps. The two data channels share a PLL. Each channel has a custom data encoder and a serializer. The encoder is digitally synthesized with the transmission latency optimization and protected with triple modular redundancy technique. The PLL and the serializer are adapted from a design that originates from the CERN's GBTX ASIC. The LOCx2-130 prototype has been fabricated, packaged, and evaluated. The power consumption of LOCx2-130 is 440 mW at the design speed of 4.8 Gbps. The output of the serializer passes the eye mask test with a bit error rate of below 10^{-12}. The latency of the chip is less than 34 ns. LOCx2-130 will be fabricated in an engineering run this fall.
LOCld-130 is a dual-channel VCSEL driver ASIC and each channel operates at 5 Gbps. Each channel in the ASIC is individually powered, making the ASIC suitable for applications in dual-channel transmitters or in transceivers. The analog core of LOCld-130 has two parts: a limiting amplifier (LA) and a high-current differential driver. The gain of the LA is 14 dB. A shared inductive peaking is used in the 2-stage amplifier to boost the bandwidth to 3.5 GHz. The power consumption of LOCld-130 is 112 mW when the modulation current is 6 mA and the bias current is 2 mA. The design has been verified in simulation and is ready for submission.

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