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Development of a cryogenic readout circuit based on FD-SOI CMOS for a far-infrared astronomical image sensor

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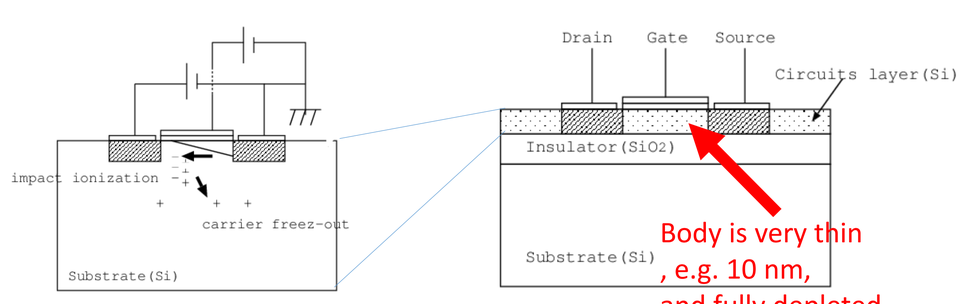
Abstract

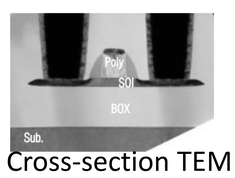
We are developing an image sensor with sensitivity in far-infrared wave lengths (FIR: 30 - 200 μm) for astronomical observations. The readout integrated circuit (ROIC) for the FIR image sensor must be cooled down to cryogenic temperature below 2 K to reduce thermal dark current of the detector.
Conventional bulk-MOSFETs show degradation in I-V characteristics such as kink and hysteresis at cryogenic temperatures. In contrast, fully-depleted silicon on insulator (FD-SOI) MOSFETs show stable characteristics below 4 K. We designed a capacitive trans-impedance amplifier (CTIA) based on FD-SOI CMOS and evaluated its performance at 4.2 K.

I-V characteristics MOSFETs at 4.2 K

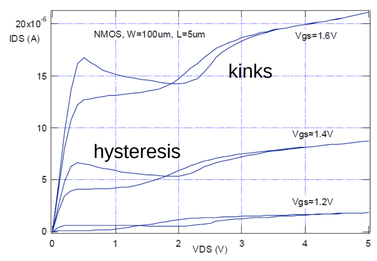


Structure of bulk MOSFET

Structure of FD-SOI MOSFET

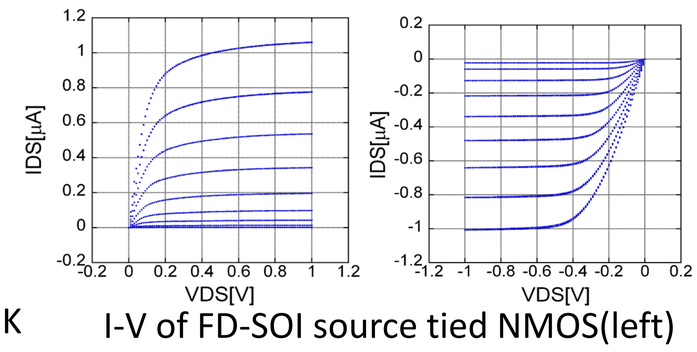


Cross-section TEM photograph of FD-SOI MOSFET
Morikawa et al. 2003



Merken et al. 2004, SPIE 5498, 622

I-V of bulk NMOS at 4.2 K



I-V of FD-SOI source tied NMOS(left) and PMOS(right) at 4.2 K

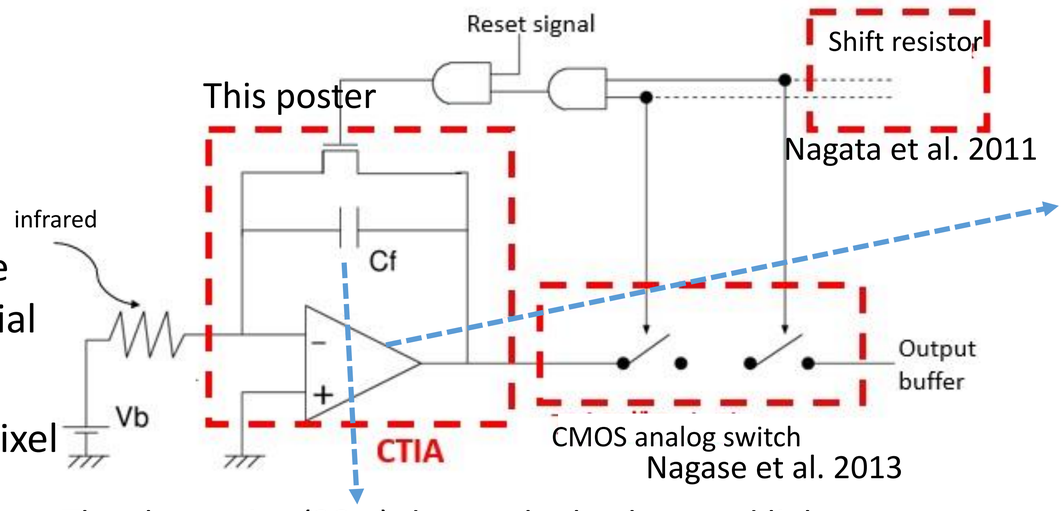
Circuit design

The capacitive trans-impedance amplifier (CTIA) consists of an OPAMP, a feedback capacitor and a reset switch.

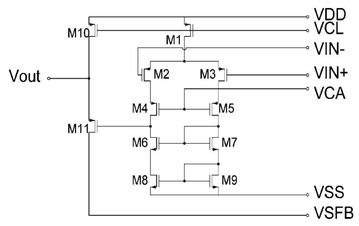
The feedback capacitance C_f was designed so that noise performance reached the natural background limit for a cooled space infrared telescope with diffraction limited spatial resolution with Nyquist sampling pixel size.

The number of electrons to be integrated in a pixel is N_e = 812 e and its shot noise is $(N_e)^{0.5}$ = 28 e. in the integration time (1 s). (Wada et al. 2012)
N_e was derived by using following conditions.

- Detection efficiency η = 0.15
- Spectral resolution R = λ/dλ = 10
- Background intensity I= 4.31 MJy/str at λ=65 μm (Matsuura et al. 2011)



The schematic diagram and performances of the OPAMP

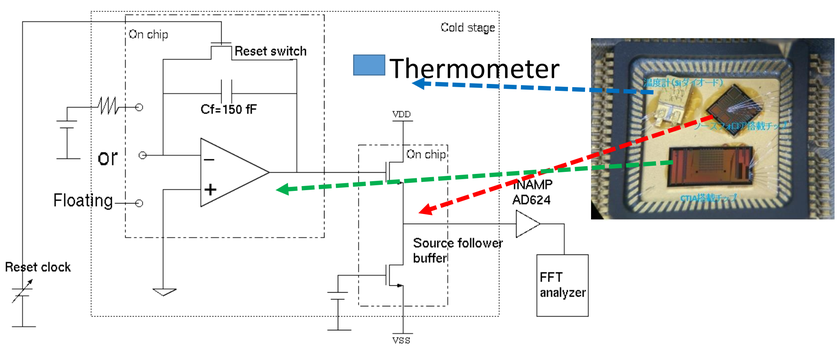


At 4.2 K	Measured performances
Open loop gain	> 7000
Power dissipation	1.3 μW
Output Voltage swing	1.3 V
Input offset voltage	2mV
Variation of input offset voltage	4.2 mV
Input referred noise	19uV/Hz$^{0.5}$

Nagata et al. 2011

The shot noise (28 e) due to the background light is less than electrons (18 e) integrated in the feedback capacitor (C_f =150 fF) by the input referred noise (19 uV) of the OPAMP.
Therefore, the design of the CTIA is matched to the natural background limited performance.

Performance of the CTIA at 4.2 K



Experiment setup of the measurements

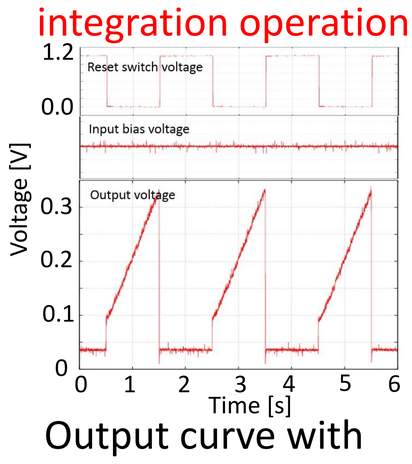
Summary of these measurements

	Design	Measurement
Output swing	2.9 V	1.18 V (Full well=1 × 10^6 e)
Noise(CDS)	18 e	89 e
Power dissipation	1 μW	1.47 μW
Leak current	< 5.0 × 10^{-15} A	1.4 × 10^{-17} A

Reasons of the discrepancy between the design and the measurement values is under investigation :

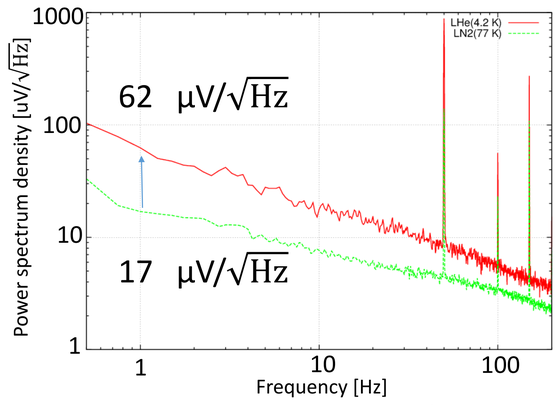
- the decrease of the output swing may be due to kink of MOSFET used for the reset switch.
- The increase of the noise may be due to too large V_{ds} of M10 and M11 in the OPAMP.

Successful reset and integration operation



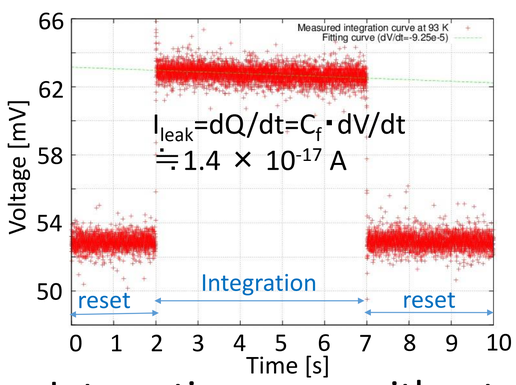
Output curve with a constant input current

Noise performance of the CTIA



Power spectrum density

Leak current



Integration curve without input current

Calculation of readout noise (CDS)

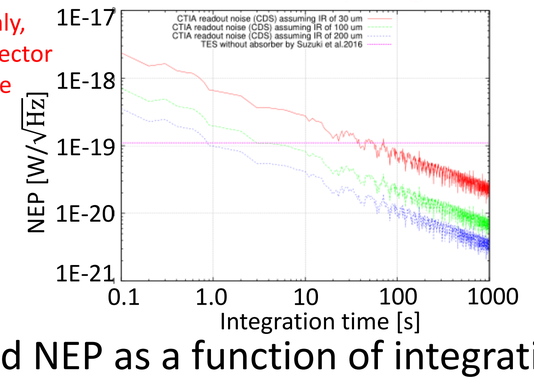
$Q_n = C_f \cdot V_n$, $V_n^2 = \int_{f1}^{f2} V_{PSD}^2 \times |G(f)|^2 df$

The transfer function of correlated double sampling (CDS)

$$G(f) = \int_{-\infty}^{\infty} (\delta(t+T) - \delta(t)) exp[2\pi i f t] dt = 1 - exp(-2\pi i f T)$$

Expected NEP in a CDS sampling

Readout noise only, not including detector dark current noise



Expected NEP as a function of integration time assuming a detector Q.E. of 0.1

Conclusion

We designed a cryogenic CTIA and obtained its excellent performance at 4.2 K.
The CTIA will be combined with 1000 pixels array of the Ge-BIB detector in future works.

Acknowledgments

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