Performance of CMOS pixel sensor prototypes in AMS H35 and aH18 technology for the ATLAS ITk upgrade

Francesco Armando Di Bello[1], Mathieu Benoit[1], D M S Sultan[1], Didier Ferrere[1], Sergio Gonzalez Sevilla[1], Giuseppe Iacobucci[1], *Moritz Kiehn*[1], Mateus Vicente Barreto Pinto[1], Winnie Wong[1], Ettore Zaffaroni[1], Claudia Merlassino[2], Antonio Miucci[2], Thomas Weston[2], Dylan Frizzell[3], Hucheng Chen[4], Kai Chen[4], Francesco Lanni[4], Hongbin Liu[4], Weihao Wu[4], Jessica Metcalfe[5], Matt Zhang[6], Ivan Peric[7], Raimon Casanova Mohr[8], Eva Vilella Figueras[9]

[1] Université de Genève, [2] Universität Bern, [3] University of Oklahoma, [4] Brookhaven National Laboratory, [5] Argonne National Laboratory, [6] University of Illinois at Urbana-Champaign, [7] Karlsruhe Institute of Technology, [8] Universitat Autonoma de Barcelona, [9] University of Liverpool

Abstract

Pixel sensors based on commercial high-voltage CMOS processes are an exciting technology that is considered as an option for the ATLAS inner tracker upgrade. Here, particles are detected using deep n-wells as sensor diodes with the depleted region extending into the silicon bulk. Both analog and digital readout electronics can be added to achieve different levels of integration up to a fully monolithic sensor. Small scale prototypes using the AMS technology have previously demonstrated that it can in-principle achieve the required radiation tolerance above 10^{15} neq/cm^2 and detection efficiencies above 99%. Recently, large area prototypes, comparable in size to a full sensor, have been produced that include most features required towards a final design: the H35demo prototype produced in AMS H35 technology that supports both external and integrated readout and the monolithic ATLASPix1 pre-production design produced in AMS aH18 technology. Both chips are based on large fill-factor pixel designs, but differ in readout structure.

H35demo prototype

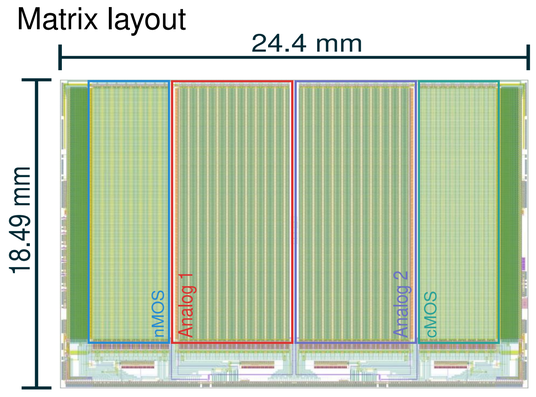
H35demo is large-scale CMOS prototype produced in H35 350 nm ams technology. It contains four independent matrices: two matrices with integrated monolithic readout (nMOS, cMOS) and two matrices that contain only the analog circuitry (Analog1, Analog2) and must be readout with a separate readout chip.

nMOS and cMOS standalone matrices
- 16 × 300 pixels
- 250 µm x 50 µm pitch

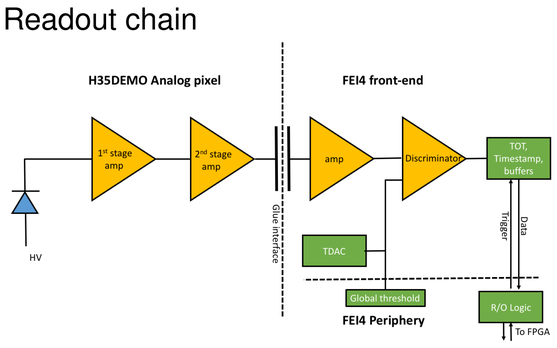
Analog1 and Analog2 matrices
- 23 x 300 pixels
- 250 µm x 50 µm pitch
- Column-drain architecture

In the studies presented here the ATLAS FE-I4B is glued onto the H35demo to form a capacitely-coupled hybrid pixel detector (CCPD).

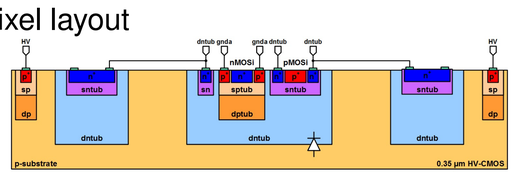
Matrix layout



Readout chain



Pixel layout



ATLASPix1 prototype

ATLASPix1 is a monolithic large-scale prototype produced in aH18 180 nm ams technology. It contains three independent matrices that differ in their pixel geometry and readout architecture.

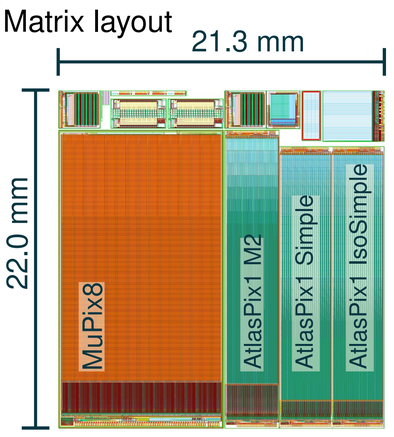
Matrix M2
- 56 × 320 pixels
- 60µm × 50µm pitch
- Parallel-pixel-to-buffer architecture with triggered readout

Matrix Simple
- 25 × 400 pixels
- 130 µm × 40 µm pitch
- Column-drain architecture

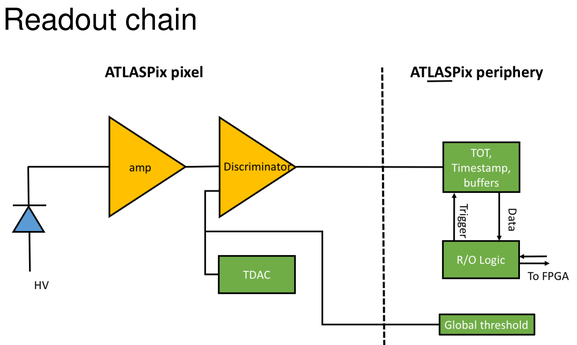
Matrix IsoSimple
- 25 × 400 pixels
- 130 µm × 40 µm pitch
- Column-drain architecture

* Additional fourth well to isolate PMOS transistors

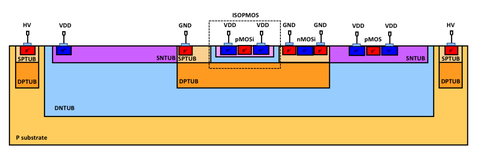
Matrix layout



Readout chain



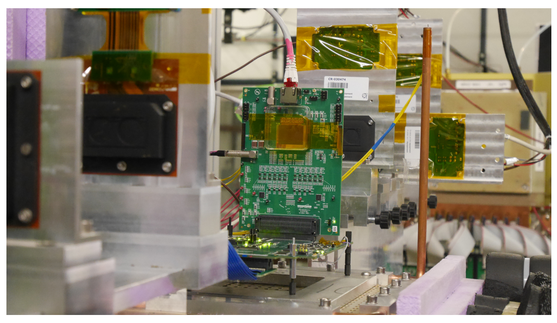
Pixel layout



Telescope setup at CERN SPS and Fermilab

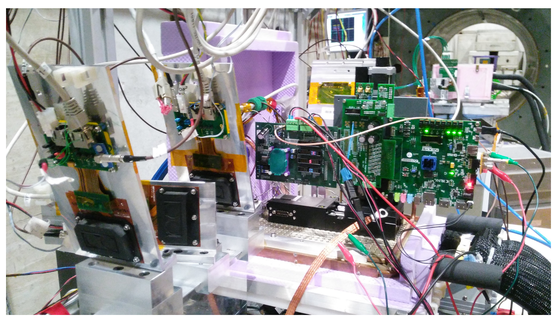
- 6 ATLAS IBL planar modules with FE-I4 readout chip as reference planes
- HSIO2-based data aquisition system with full integration of FE-I4-based devices
- Trigger-busy scheme for standalone devices-under-test

Geneva telescope and H35demo at Fermilab



- 120 GeV/c hadron beam
- Point resolution on the device-under-test ~10-15 µm

Geneva telescope and ATLASPix1 at CERN SPS

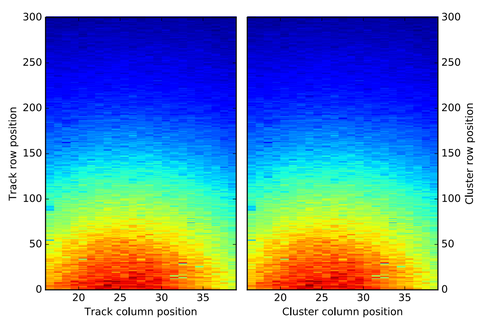


- 180 GeV/c hadron beam
- Point resolution on the device-under-test ~10-12 µm

Testbeam results H35demo

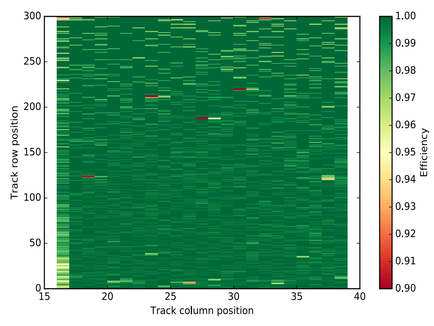
Example track/cluster distributions

Analog1 matrix, 1 kΩcm resistivity



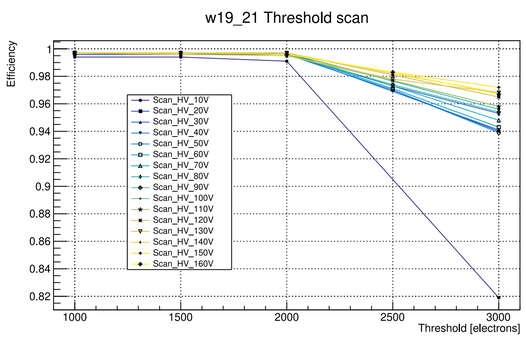
Efficiency

Analog1 matrix, 1 kΩcm resistivity



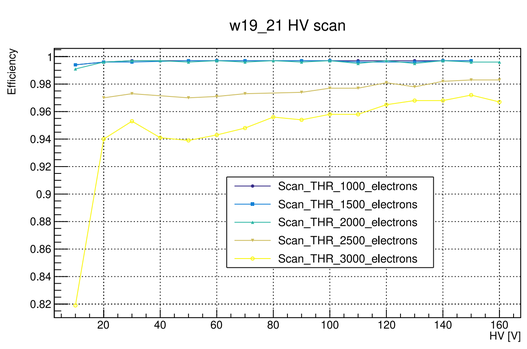
Threshold scan

Analog1 matrix, 1 kΩcm resistivity



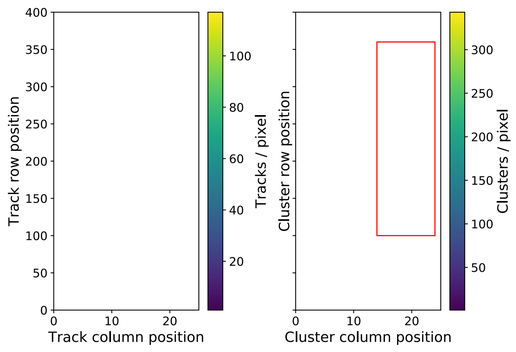
High-voltage scan

Analog1 matrix, 1 kΩcm resistivity

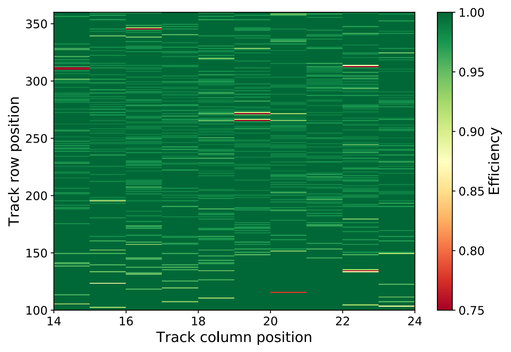


Testbeam results ATLASPix1 Simple matrix

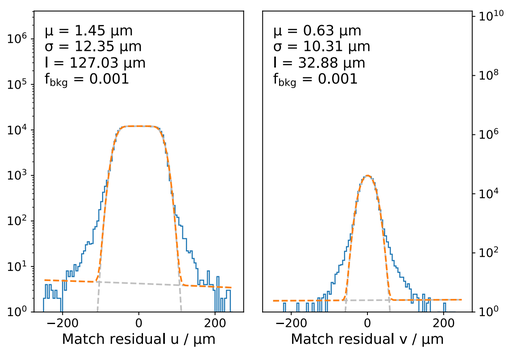
Example track/cluster distributions



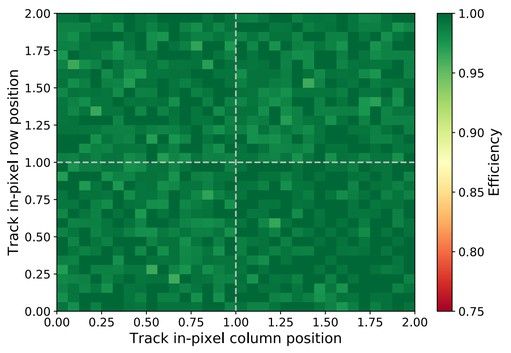
Efficiency in region-of-interest



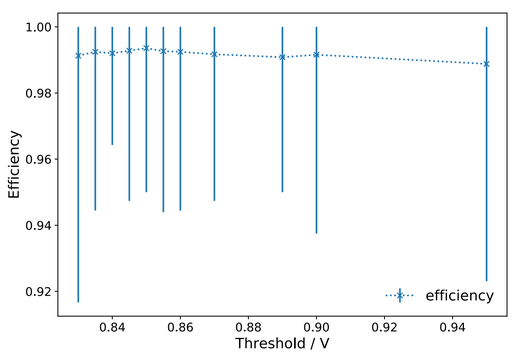
Hit residuals



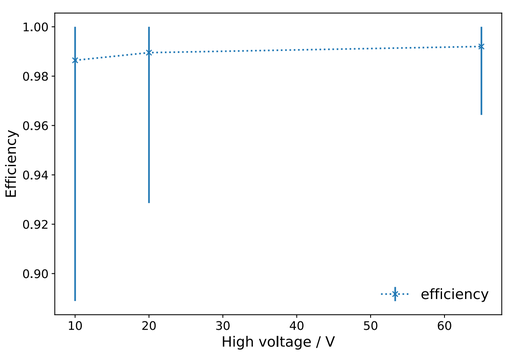
In-pixel efficiency in region-of-interest



Threshold scan



High-voltage scan



All measurements were performed using one of the first available prototypes using the following setup:
- 80 Ωcm substrate resistivity
- Simple matrix
- KIT data aquisition system

The efficiencies shown are the global efficiencies in the region-of-interest. The uncertainties represent the inter-pixel variations and are calculated as the central 90 % interval of the per-pixel efficiency distribution. The mean and the lower limit are dominated by the few low efficiency outlier pixels that can be seen in the efficiency map. They are most likely the result of the preliminary tuning procedure and are expected to improve in the future.

Moritz Kiehn
Département de Physique Nucléaire et Corpusculaire

UNIVERSITÉ DE GENÈVE