Layout Overview and Developments for the upgrade of the Inner Tracker of the ATLAS experiment for the High-Luminosity LHC

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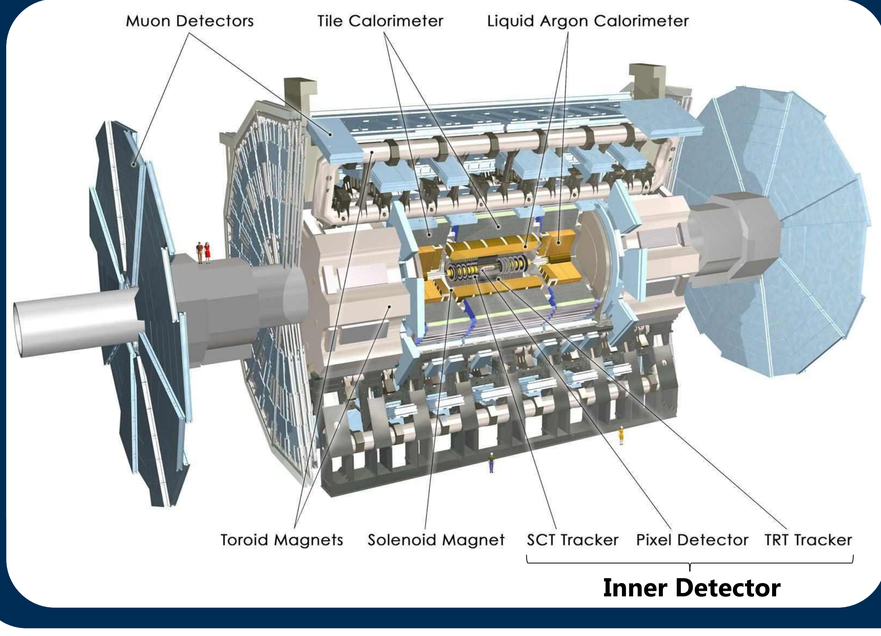
on behalf of the ATLAS ITk Collaboration

The ATLAS Inner Detector (ID)

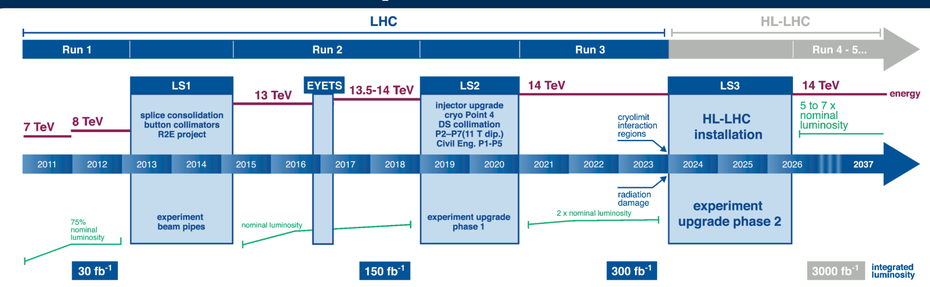


ATLAS is a general purpose experiment at CERN's Large Hadron Collider (LHC).

The Inner Detector (ID), designed for tracking and vertexing with high precision, comprises:

- The Pixel Detector
- The SemiConductor (strip) Tracker (SCT) and
- The Transition Radiation Tracker (TRT).

The LHC Roadmap

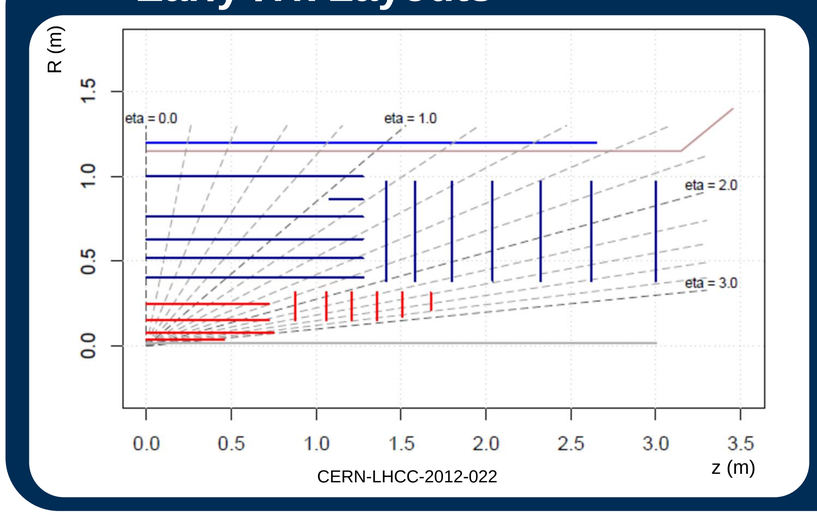


The long term target is to reach integrated luminosity of 4000 fb^{-1}. Two further machine upgrades will be required to achieve this:

- LS2 for instantaneous luminosity 2-3 x 10^{34} $cm^{-2}s^{-1}$
- LS3 for instantaneous luminosity 5-7.5 x 10^{34} $cm^{-2}s^{-1}$

For phase 2, ATLAS needs a new Inner Tracking detector (ITk) because the present pixel and strip detectors cannot survive 4000 fb^{-1} due to radiation damage and the TRT will saturate at HL-LHC multiplicity (200), so cannot be used.

Early ITk Layouts

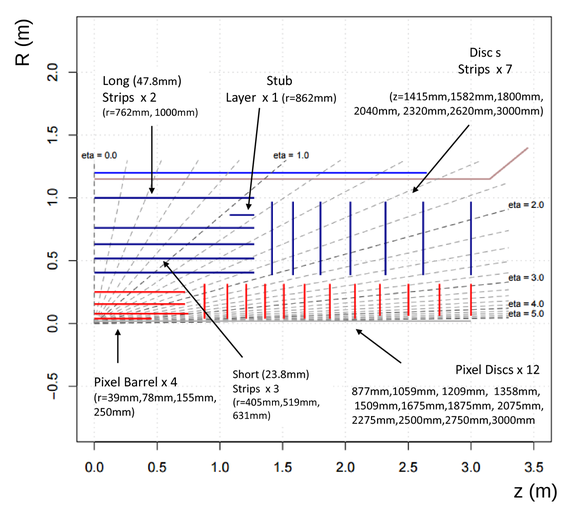


Objective: the ITk must perform at least as well as the present ID but in the harsher environment of the HL-LHC.

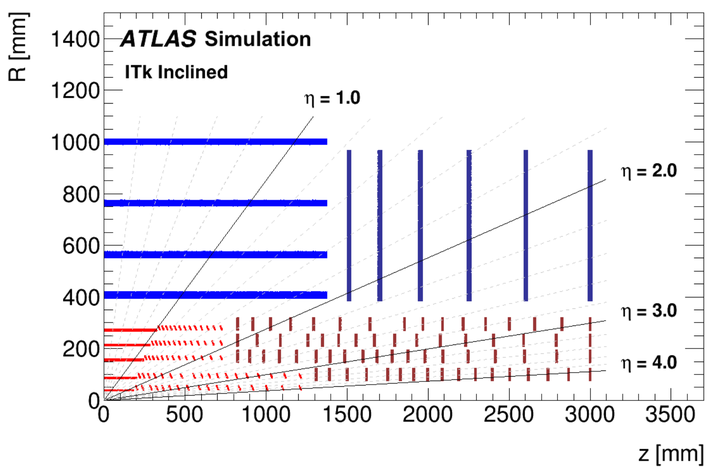
[L] Letter of Intent (LoI) layout (CERN-LHCC-2012-022)
- Coverage of up to |η| ~2.7 with 14 hits per track.
- Pixels: 4 barrels and 6 disks
- Strips: 5 barrels + "stub" layer, 7 disks

[R] Letter of Intent – Very Forward (LoI-VF) layout (2015)
- **Extended tracking acceptance up to |η| ~4.0**
- Pixels: 4 barrels and 12 disks
- Strips: 5 barrels + "stub" layer, 7 disks

Whilst not yet fully optimised, the LoI-VF layout became the baseline from which more realistic layouts could be designed.



Strip Technical Design Report (TDR), January 2017

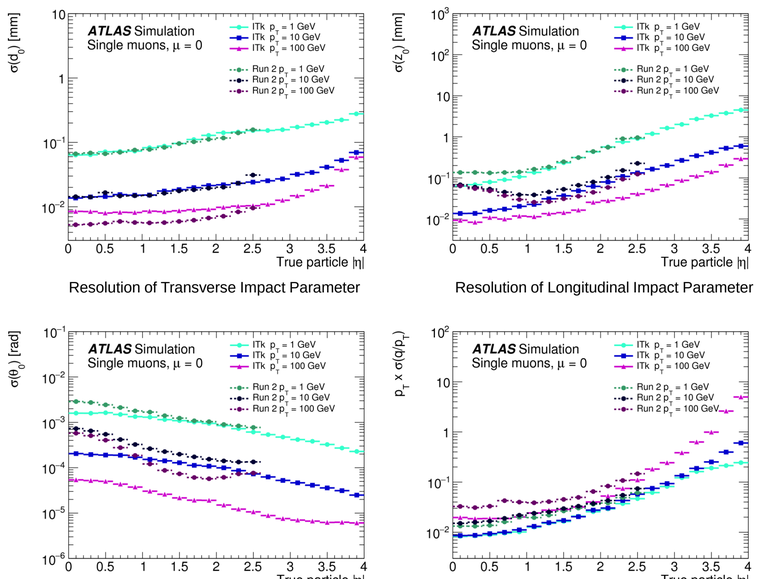


ITk Inclined layout from the Strip TDR (01/2017)

ATLAS-TDR-025

[L] ITk Inclined layout from the Strip TDR (ATLAS-TDR-025)
- Optimised for tracking performance, cost effectiveness, ease of construction and installation.
- Pixels: 5 barrels with "rings" replacing disks
  - inclined modules between barrels and rings
    - less silicon / mass
  - alternate "extended" barrel layout also considered (not shown)
    - easier to build, but more silicon / mass
- Strips: 4 barrels and 6 disks
  - Impractical "stub" layer gone
  - Barrels extended by 0.1 m (from 13 to 14 modules)

[R] Track Parameter Resolutions *compared to Run 2 ID Performance*
- d_0 resolution for p_T =100 GeV tracks worse (but still <10 μm)
  - due to the larger radius of first layer and digital clustering
- z_0 and θ_0 resolution better for all p_T values
  - due to the decreased pixel pitch
- Momentum resolution improved by 50%
  - ITk strip tracker has better precision than TRT

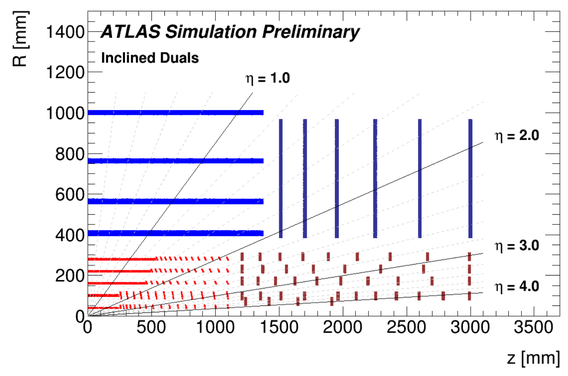


Resolution of Transverse Impact Parameter | Resolution of Longitudinal Impact Parameter

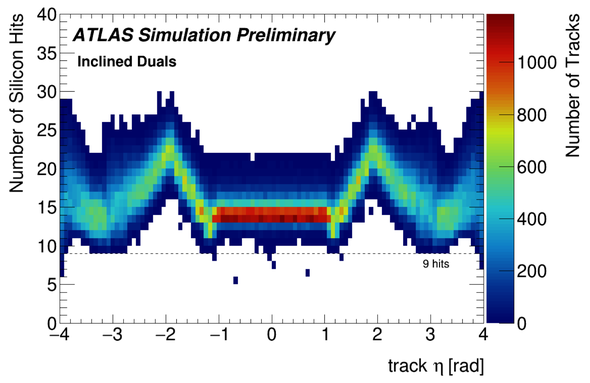
Resolution of Polar Angle | Momentum Resolution

ATLAS-TDR-025

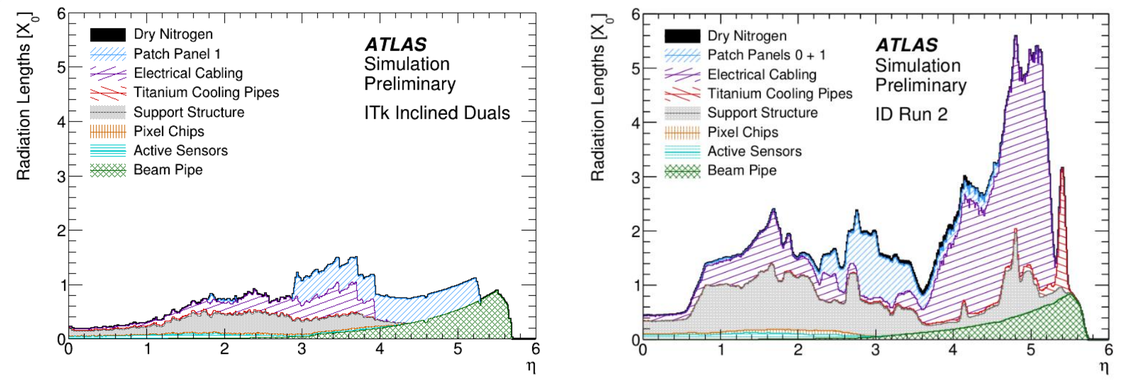
Pixel Technical Design Report (TDR), December 2017



ITk Inclined Duals layout from Pixel TDR (12/2017)



Number of Silicon Hits vs η
for the ITk Inclined Duals layout



Material (in radiation lengths) vs η for the proposed
ITk Inclined Duals layout [left] and the present Run 2 Inner Detector [right]

[L] The ITk Inclined Duals layout presented in the Pixel TDR has evolved from the ITk Inclined layout, further optimised for performance and cost. Changes are confined to the pixel detector. The pixel barrel is now longer by 40 cm such that the transition between the barrel and end-cap regions is not aligned in η for pixels and strips. In the inclined barrel region, most modules are now "duals" with 2 readout chips, the exceptions being "singles" (1 readout chip) in barrel 0 and "quads" (4 readout chips) in barrel 1; in addition the angle of inclination has been changed in layers 0 and 1. In the end-cap region an extra ring layer improves performance close to η = 4.0. [C] Beyond |η| = 2.7 the silicon (pixel plus strip) hit requirement has been reduced from 13 to 9, which has been shown to be sufficient for the rejection of fake tracks. [R] The optimised layout offers a significant reduction in material compared with the ATLAS ID which it shall replace, despite its increased segmentation. In part this is due to the use of serial powering (pixels) and DC-DC point of load conversion (strips) to allow power to be delivered through minimal cable mass. The pixel TDR is scheduled to be submitted to the LHCC/UCG on 15th December 2017.

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