

Radiation Tolerant RF-LDMOS Transistors, Integrated into a 0.25 μm SiGe-BICMOS Technology

R. Sorge, J. Schmidt, F. Reimer, Ch. Wipf, F. Korndörfer, R. Pliquet and R. Barth

Abstract— Mixed signal on-chip solutions for space applications and high energy physics experiments require high voltage RF-LDMOS transistors with sufficient ruggedness against ionizing radiation and single event burnout. We report on a novel hardening by design approach for radiation tolerant integrated RF NLD MOS transistors confirmed by single event burn out (SEB) and total ionizing dose (TID) radiation tests. In order to substantially decrease TID induced leakage currents the shallow trench isolation (STI) of MOS transistors was replaced by narrow junction isolated regions. For a significant increase of the SEB onset voltage a cascode arrangement consisting of an isolated NMOS and NLD MOS was chosen. The floating NMOS-drain/NLD MOS-source node in the cascode arrangement is always reverse biased what efficiently avoids a turn-on of the parasitic npn bipolar transistor. The rad-hard isolated NMOS/NLD MOS cascode features a breakdown voltage $BV_{DS} > 50\text{ V}$, a maximum cut off frequency $f_T = 5\text{ GHz}$ and a maximum oscillation frequency $f_{MAX} = 14\text{ GHz}$. In comparison with standard NLD MOS transistors the isolated NMOS/NLD MOS cascode device shows an increase of the SEB onset voltage from 14V to 30V at a linear energy transfer LET of 67.7 MeVcm²/mg and a negligible increase of source drain leakage currents up to a TID of 1.5 Mrad after irradiation with a ⁶⁰Co source.

Index Terms— Radiofrequency integrated circuits, Power MOSFET, Total ionizing dose, Radiation hardening (electronics)

I. INTRODUCTION

K EY challenges for integration of RF LDMOS transistors into highly scaled CMOS processes with a thin gate oxide are good RF performance, high break down voltage, low on resistance and small device parameter degradation due to hot carrier injection (HCI) [1]. RF-LDMOS power transistors are key components in highly efficient DC/DC converter circuits for integrated power management solutions in space applications and high energy physics experiments [2,3]. Similar to their NMOS transistor counterparts NLD MOS transistors also suffer from parameter degradations due to TID related leakage paths between source and drain originating from positive charges trapped in the thick oxide of the lateral STI region. As a second source of device malfunction the generation of electron hole pairs in the active device region during irradiation with charged high energy particles leads temporarily to a dramatic increase of the substrate current which can finally turn on the parasitic npn bipolar transistor. The resulting

thermal runaway can finally destroy the NLD MOS transistor. We address the radiation induced malfunctions of NLD MOS with a novel hardening by design (HBD) approach without process changes. The fabricated devices were evaluated by DC-, RF-S-parameter-, 1/f noise measurements. TID and SEB radiation tests were performed on standard NLD MOS (NLD_ST), NLD MOS with lateral junction isolation (NLD_JI) and an isolated NMOS/NLD MOS cascode with lateral junction isolation (NLD_CA) as the proposed target device construction.

II. DEVICE

Two constructive measures were applied for improvement of TID and SEB immunity of NLD MOS transistors. First, we introduced a lateral junction isolation to suppress the strong increase of source drain leakage in NMOS transistors after irradiation with a ⁶⁰Co source. Secondly an isolated NMOS/LDMOS cascode arrangement was used to substantially increase the SEB onset voltage. Fig. 1 shows the cross section scheme of the isolated NMOS/NLD MOS cascode arrangement. The increase of the SEB onset voltage relies on the fact that the common floating node of drain D1 and source S2 is always weakly reverse biased. This prevents that the base emitter junction of the NLD MOS parasitic npn gets forward biased, so that the blocking properties of the parasitic npn transistor can be maintained under irradiation with high energetic heavy ions.

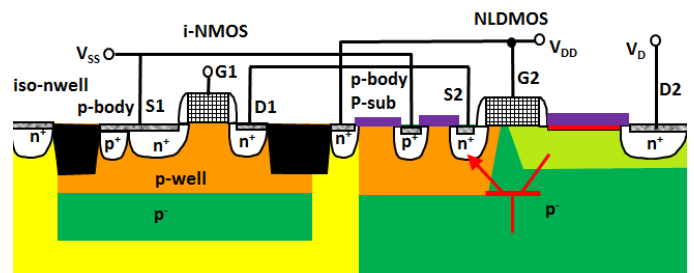


Figure 1: Cross section A'-A'' of isolated NMOS/NLD MOS cascode device (NLD_CA) according to the layout in Figure 4.

Figure 2 shows a standard NLD MOS (NLD_ST) layout with two gate fingers and STI isolation in the lateral channel regions. In the layout shown in Fig 3 the lateral STI isolation of the channel regions was replaced by junction isolation to prevent the source drain leakage resulting from the influence of trapped fixed positive charge in the thick STI layers after exposure of the device to ionizing radiation. Note, that the whole device lies now completely in ACTIVE silicon and the

poly silicon gate contacts are located also in the ACTIVE region.

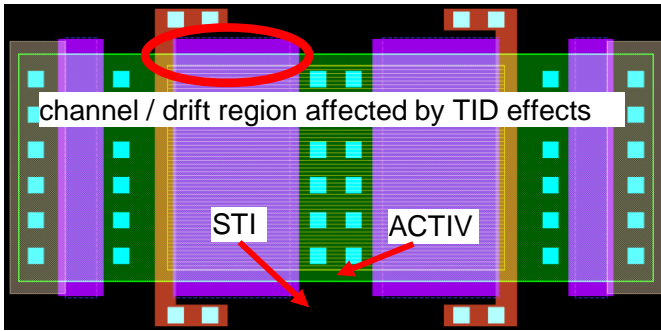


Figure 2: Layout of standard STI isolated NLD MOS (NLD_ST) with two gate fingers (color legend see Figure 4).

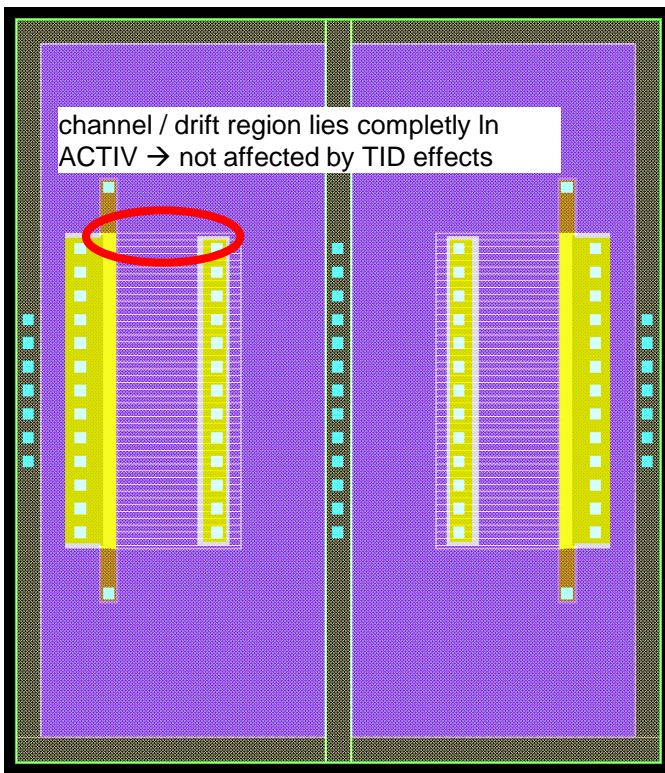


Figure 3: Layout of NLD MOS (NLD_JI) with lateral junction isolation (two gate finger device, color legend see Fig. 4).

The combination of these device construction measures, i.e. isolated NMOS/NLD MOS arrangement and lateral junction isolation, yields a substantial increase of the radiation hardness of LDMOS power devices in terms of TID and SEB. Fig 4 depicts a layout of the isolated NMOS/NLD MOS cascode arrangement corresponding to the cross section scheme of Fig 1. As shown in Fig. 4 lateral junction isolation (see Fig 3) instead of STI isolation is realized for both the isolated NMOS and the NLD MOS.

III. EXPERIMENTAL

In order to compare the vulnerability of the several LDMOS device constructions against radiation effects a standard STI isolated NLD MOS (NLD_ST), a NLD MOS (NLD_JI) with lateral junction and an isolated NMOS/NLD MOS cascode arrangement with lateral junction (NLD_CA) (see Figs 2,3,4) were prepared in one process flow using IHP's 0.25 μm SiGe BCD technology SGB25VGDA.

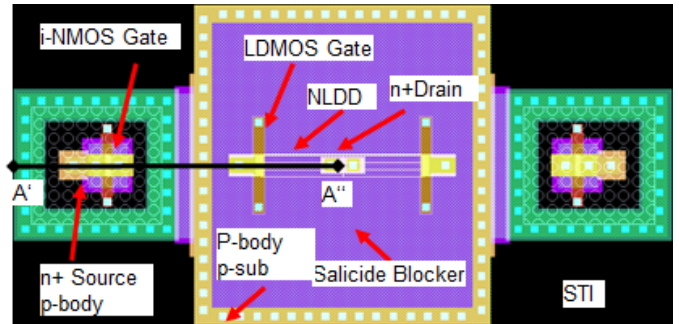


Figure 4: Layout of the target NLD MOS device construction with two gate fingers featuring an isolated NMOS/NLD MOS cascode arrangement with lateral junction isolation (NLD_CA).

The measured transfer and breakdown characteristics of the NLD_ST, NLD_JI and NLD_CA transistors are depicted in Figs. 5, 6 and 7.

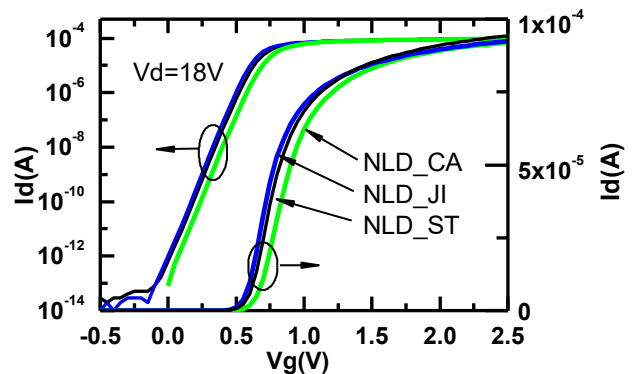


Figure 5: Transfer characteristics at $V_D=0.1$ V of standard NLD MOS (_ST), NLD MOS (_JI) with lateral junction isolation and isolated NMOS/NLD MOS (_CA) with lateral junction isolation in linear mode of operation. $w_G=10\mu\text{m}$.

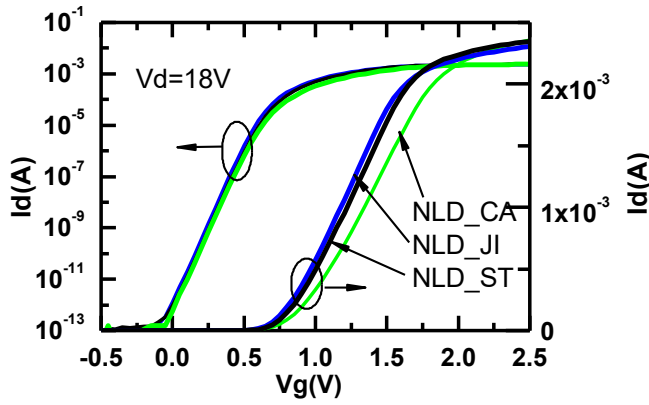


Figure 6: Transfer characteristics at $V_D=18$ V of standard NLD MOS (_ST), NLD MOS (_JI) with lateral junction isolation and isolated NMOS/NLD MOS (_CA) with lateral junction isolation in saturation mode of operation. $w_G=10\mu\text{m}$.

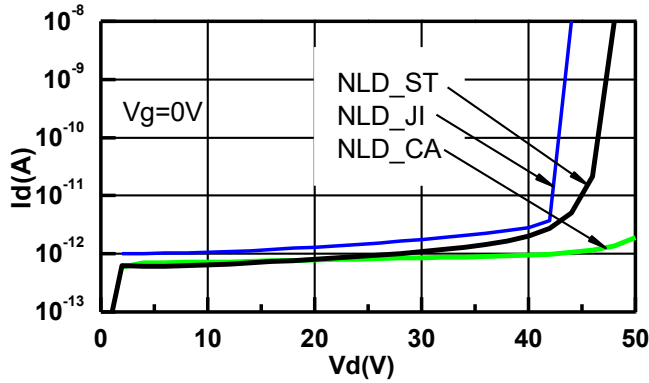


Figure 7: Breakdown characteristics of standard NLD MOS (_ST), NLD MOS (_JI) with lateral junction isolation and isolated NMOS/NLD MOS (_CA) with lateral junction isolation. $w_G=10\mu\text{m}$.

There are no significant differences in the DC characteristics of all three devices. An additional potential reliability issue for LDMOS devices is the degradation due to hot carrier injection (HCI). Due to the fact that the gate voltage V_{G2} of the NLD MOS in the cascode arrangement is connected always with $V_{DD}=2.5\text{V}$ of the underlying CMOS core the NLD MOS body current is far away from its maximum value at around $V_G=V_{DD}/2$ what gives a reduced HCI degradation of the NLD MOS. The HCI related degradation of the isolated NMOS transistor in the isolated NMOS/LDMOS cascode arrangement is also very small because it operates always in linear mode with $V_{DS1} \ll 2.5$ V. The resulting low level of body currents indicate very small HCI induced MOS transistor parameter degradations. Table I shows the maximum drain operation voltage for 10 years lifetime extracted from hot carrier induced drain current degradations in the linear and saturation mode of operation.

The maximum cut off frequency f_T and the maximum oscillation frequency f_{MAX} were extracted from S-parameter measurements at $V_D=8$ V. We obtained for the three devices NLD_ST: $f_T/f_{MAX}=15/34$ GHz/GHz, NLD_JI: $f_T/f_{MAX}=15/35$ GHz/GHz, NLD_CA: $f_T/f_{MAX}=5/14$ GHz/GHz.

Table I

MAXIMUM DRAIN VOLTAGE FOR 10 YEARS LIFETIME EXTRACTED FROM HOT CARRIER INJECTION RELATED DRAIN CURRENT DEGRADATION $\Delta I_D/I_{D0} < 0.1$ IN LINEAR (IDLIN) AND SATURATION (IDSAT) MODE OF OPERATION AT 100% DUTY CYCLE

Device	IDLIN	IDSAT
Standard NLD MOS (NLD_STA)	22 V	21 V
NLD MOS, lateral junction isolation (NLD_JI)	23 V	21 V
Isolated NMOS/NLD MOS Cascode, lateral junction isolation (NLD_CA)	36 V	33 V

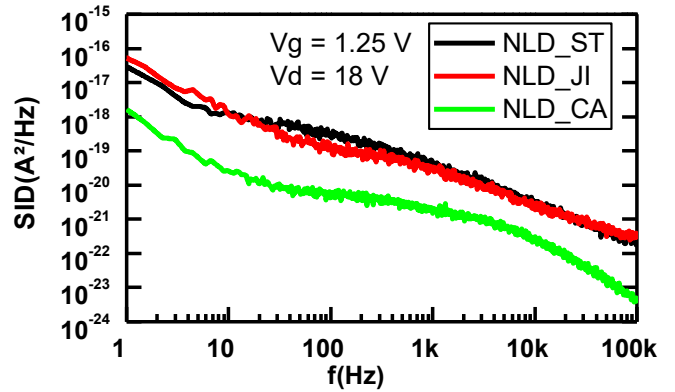


Figure 8: $1/f$ (Flicker) noise of standard NLD MOS (_ST), NLD MOS with lateral junction isolation (_JI) and isolated cascode NMOS/NLD MOS with lateral junction isolation (_CA).

Fig. 8 shows the results of $1/f$ (Flicker) noise measurements for the three investigated LDMOS devices performed with the AdMOS 3001B Flicker Noise Measurement System. STI and junction isolated LDMOS transistors exhibit a similar noise performance. In contrast, the isolated NMOS/NLD MOS cascode configuration shows a significantly decreased $1/f$ (Flicker) noise.

IV. RADIATION TESTS

We have evaluated the radiation hardness in terms of TID and SEB for a standard NLD MOS, a NLD MOS with lateral junction isolation and an isolated NMOS/LDMOS cascode arrangement with lateral junction isolation. The TID tests were performed at a dose rate of 10 krad(Si)/h, using the ^{60}Co source at the Helmholtz Zentrum Berlin (HZB). In contrast to the standard NLD MOS device (see Figure 9) we observed no TID induced increase of source drain leakage for the isolated NMOS/NLD MOS cascode arrangement with lateral junction isolation up to a radiation dose of 1.5 Mrad, which proves the effectiveness of the applied concept of lateral junction isolation

(see Figure 10). The leakage current remains unchanged at a very low level of $< 1\text{pA/edge}$.

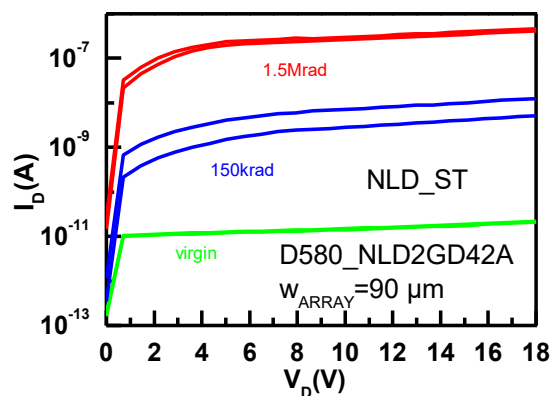


Figure 9: Source drain leakage of standard NLD MOS ($_{ST}$, $W_{G,ARRAY}=90\mu\text{m}$) before and after gamma irradiation.

SEB tests were performed in the Accelerator Laboratory at the University of Jyväskylä, Finland. The test conditions for determination of the SEB onset voltage of the NLD MOS devices were: $^{131}\text{Xe}^{+35}$ Xenon ions, energy 1217 MeV, Tilt 0° , LET at the surface $57.36\text{ MeVcm}^2/\text{mg}$, LET at $57\mu\text{m}$ depth $67.9\text{ MeVcm}^2/\text{mg}$, beam fluence 10^7cm^{-2} . For the proposed junction isolated NMOS/NLD MOS cascode arrangement (NLD_CA)) we measured a SEB onset voltage $V_{SEBTH} > 30\text{V}$. For the corresponding standard NLD MOS device NLD_ST and the NLD MOS NLD_JI with lateral junction isolation we obtained for $V_{SEBTH} < 14\text{V}$ only.

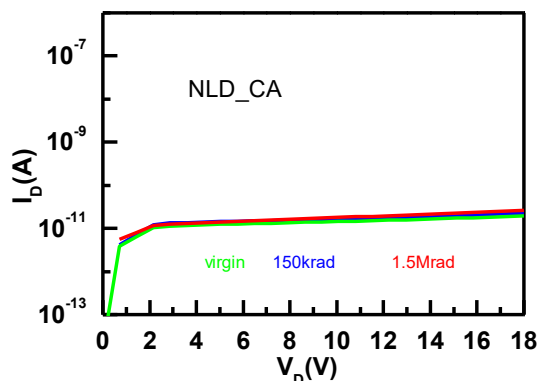


Figure 10: Source drain leakage of junction isolated NMOS/NLD MOS cascode ($_{CA}$, $W_{G,ARRAY}=180\mu\text{m}$).

V. SUMMARY AND OUTLOOK

A novel radiation hardening by design approach for NLD MOS transistors based on an isolated NMOS/NLD MOS cascode arrangement has been successfully verified. In order to suppress TID induced drain leakage currents in the lateral regions of the MOS transistor channel junction isolation was applied instead of shallow trench isolation. The chosen approach enables the fabrication of radiation tolerant RF LDMOS transistors with blocking

voltages $> 50\text{V}$ and a SEB onset voltage $> 30\text{V}$. The devices were fabricated in IHP's $0.25\mu\text{m}$ SiGe BCD SGB25VGDA process without process changes. In comparison to standard LDMOS transistors the isolated NMOS/NLD MOS cascode transistors with lateral junction isolation show a substantial improvement of radiation hardness in terms of TID and SEB. The substantial improvement of the radiation hardness was achieved together with a good DC and RF device performance, HCI stability and a very low Flicker noise level.

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REFERENCES

- [1] K.-E. Ehwald, et al., "High performance RF LDMOS transistors with 5 nm gate oxide in a $0.25\text{ }\mu\text{m}$ SiGe:C BiCMOS technology," in *IEDM Symp. Tech. Dig.*, Dec. (2001), 895
- [2] F. Faccio et al., TID and Displacement Damage Effects in Vertical and Lateral Power MOSFETs for Integrated DC-DC converters, *IEEE Trans. Nucl. Sci.* 57, (2010) 1790
- [3] F. Faccio et al., "Total ionizing dose effects in shallow trench isolation oxides", *Microel. Rel.* 48 (2008) 1000.