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FLAME readout ASIC for luminosity detector in future linear collider

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Future high energy physics experiments, like future linear collider ILC/CLIC, put new challenges for detector readout systems. One of such challenges is to develop a very low power multi-channel readout ASIC containing analog front-end and fast analog-to-digital converter (ADC) in each channel. This would allow the use of very simple and elegant readout architecture, comprising also an on-chip digital signal processing (DSP). In the past the main obstacle in realization of such readout architecture was the lack of fast ultra-low power ADC. Recently, with the availability of modern CMOS technologies and new power-efficient ADC architectures the development of fast low power mix-mode readout ASICs became possible. Such readout ASIC, FLAME (FcaL Asic for Multiplane rEadout), is being developed for the readout of luminosity detector (LumiCal) in future linear collider. It will work with radially segmented silicon pad sensors with capacitances in the range 5-20pF. It will operate either in low gain „physics"mode with signals up to several pC or in high gain „calibration" mode with minimum ionizing particles (MIPs). To relax requirements on cooling and further decrease the consumed power it will use power cycling, i.e. most of its functionalities will be active only during the beam trains and switched off between them.

The FLAME is a multi-channel ultra-low power readout ASIC in CMOS 130 nm, comprising an analog front-end and fast 10-bit ADC in each channel, followed by fast serialization and data transmission. In addition it contains all other necessary functionalities (DACs, interfaces). In the first development stage, two prototype ASICs have been designed, fabricated and tested: the FLAME ver.0 ASIC and the fast serializer ASIC. In the next step they will be integrated into the complete FLAME ASIC.

The FLAME ver.0 is an 8-channel readout ASIC comprising analog front-end and fast ultra-low power ADC in each channel. The front-end has variable gain, fully differential CR-RC shaper with peaking time 50ns and simulated noise ENC˜900el@20pF (calibration mode). The ADC has successive approximation (SAR) architecture and can sample the data with variable frequency, up to 40MSps. The total power consumption per channel is below 2mW. The serializer ASIC contains ultra-low power multi-phase PLL based serializer and fast Source-Series Termination (SST) output driver, which should work up to 20Gbps.

First tests of both ASICs have been performed confirming their basic functionalities and measurements of important parameters showed a good agreement with simulations. In particular, the shape and noise of the front-end pulses were measured before and after ADC conversion, for different input capacitances. For the serializer ASIC first eye diagrams were measured at 5Gbps output rate. Detailed measurements are still in progress.

In the presentation the design of the FLAME together with the results of first measurements of the prototype ASICs will be discussed.

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