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A Track Finder with Associative Memories and FPGAs for the L1 Trigger of the CMS experiment at HL-LHC

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The LHC accelerator at CERN is scheduled for an upgrade that will more than triple its instantaneous luminosity over the next decade. The Compact Muon Solenoid (CMS) experiment will have to cope with these new running conditions. The new tracking system under development will be capable of measuring the transverse momentum of charged particles down to 2-3 GeV/c at each bunch crossing (40 MHz), allowing for a Level-1 trigger decision that includes the precise tracking information. For this purpose, an architecture based on Associative Memories and FPGAs has been developed to identify hits and fit them into tracks in an overall processing latency of less than 4us. A hardware demonstrator system, based on a ATCA architecture, has been implemented to prove the feasibility of this approach and to measure its performances. We present the simulation/emulation framework utilized for the system optimization and the results from the hardware demonstrator.

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