11th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD11) in conjunction with 2nd Workshop on SOI Pixel Detectors (SOIPIX2017) at OIST, Okinawa, Japan

Contribution ID: **171** Type: **POSTER**

A Novel Pixel Region Architecture for Pixel detector at HL-LHC: the Central Buffer Architecture of RD53a prototype

Sunday, 10 December 2017 20:37 (1 minute)

The work focuses on the development of a novel digital architecture for the pixel chips for HEP experiments. The Pixel Detectors in HL-LHC experiments will have to maintain high efficiency under very high pixel hit rates (3GHz), and high trigger frequency (1MHz) and latency (12.5μs). As Column Drain architectures would need a very high bandwidth for data transfer between the Pixels and the Chip Periphery, research has moved onto decentralised buffering in the Pixel Matrix itself. Although working examples of this principle have already been documented, the long term pixel data retention is still a challenge for the anticipated high data rates, because of the amount of data to be stored in the pixels. Our approach tackles this problem by grouping pixels in large Pixel Regions and compressing their TOT data before saving. Every pixel has a core digital logic which manage the Analog Front-Ends, evaluates the TOT and latches its value for later processing. As the TOT computation length is unknown and different per-pixel, synchronisation is needed before the compression. A synchronisation stage achieves this with countdown timers, which in turn trigger data compression and writing. Compression is lossy, with a fixed number of TOTs that can be written per event. Already tested in the CHIPIX65_FE0 prototype, the architecture has been updated for the RD53a design in order to further reduce the inefficiencies and prepare the design to be scaled for larger pixel chips. The resulting reduction in area in the Pixel Regions makes this architecture flexible in terms of design parameters, scalable in the number of TOTs, TOT bits, and buffer depth: by tuning them, it's possible to achieve high efficiency on a wide range of applications.

Primary author: PATERNO, Andrea (Universita e INFN Torino (IT))

Co-authors: DEMARIA, Lino (Universita e INFN Torino (IT)); RIVETTI, Angelo (Universita e INFN Torino (IT))

Presenter: PATERNO, Andrea (Universita e INFN Torino (IT))

Session Classification: POSTER

Track Classification: ASICs