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# TIGER, a front-end ASIC for timing and energy measurement with radiation detectors

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We present a front-end ASIC that allows simultaneous time and energy measurements with radiation detectors. The chip, called TIGER, has been primarily developed to readout the Cylindrical Gas Electron Multiplier detector (CGEM), a novel ultra-light weight tracker to be installed in the inner part of the BESIII experiment in Beijing. Due to its characteristics and performance, the integrated circuit is also well suited to readout silicon strip sensors. In an area of 5 mm x 5 mm, the ASIC incorporates 64 channels. Each channel features a Charge Sensitive Amplifier followed by a dual shaper. The input stage can accommodate an input capacitance up to 150 pF. The bias of the input transistor can be adjusted through an on chip bias DAC to optimise the noise performance and the power consumption according to the sensor capacitance. The peaking time of the two shapers is respectively 60 and 180 ns. These values were chosen to optimise the time and energy resolution in the original application. All the core amplifiers employed in the front-end have rail-to-rail outputs to maximise the dynamic range.
Each shaper is followed by a discriminator with locally programmable threshold. A low power time-to-digital converter based on clock counters with analog interpolators allows to capture the firing time of the discriminator with a binning as low as 50 ps. The digitisation of the signal charge can be done either with Time-over-Threshold or with peak sampling, In the ToT mode, a second TDC measures the time corresponding to the falling edge of the discriminator signal. In the peak sampling mode, the output of the slow shaper is stored in a capacitor. The sampling signal is obtained by delaying properly the rising edge of the digital pulse generated by the discriminator connected to the fast shaper. The amount of delay can be programmed on a channel-per-channel basis. The value stored in the capacitor is then digitised with a 10-bit Wilkinson ADC. For derandomization purposes, four sampling capacitors are provided in each channel. The digitised data are sent out of chip through LVDS links. The ASIC can handle an event rate in excess of 60 kHz per channel. The digital logic runs with a clock frequency of 160 MHz. Protection against Single Event Upset has been also introduced.
Experimental data show a rms noise of 1500 rms electrons with 100 pF input capacitance, a charge linearity better than 0.2% over a range of 40 fC and an intrinsic time resolution of the TDC of 50 ps. The maximum power consumption is 13 mW/channel. The chip has been fabricated in a 110 nm CMOS technology. The ASIC has been produced in a dedicated engineering run, which allowed to accommodate different flavours, including one with current mode signal processing and programmable gain.
In the presentation, the chip design and the experimental results will be discussed in detail.

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