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Evaluation of Interrupted Finger SOIAPD array for soft X-ray detection

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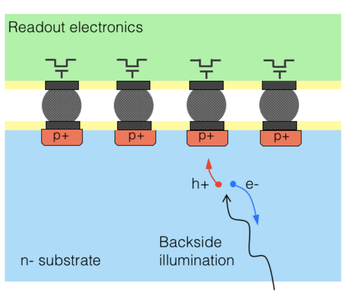
❑ Introduction

We have been developing Silicon On Insulator Avalanche PhotoDiode (SOIAPD) for synchrotron soft energy X-ray applications. The concepts of these new devices are SOI technology and linear mode APD. SOI technology has many advantages[1,2]. Especially read out circuits can be be implemented on each pixels. Linear mode APD is operated below breakdown voltage(Vb) but near breakdown voltage. In this mode, the incident single photon energy and the output charge are in a proportional relationship. In this study, we report on the evaluation of SOIAPD test chip which of this structure is a Interrupted Finger (FIN) APD [3,4] using 0.2 μm fully depleted SOI CMOS process.

❑ SOIAPD for soft X-ray

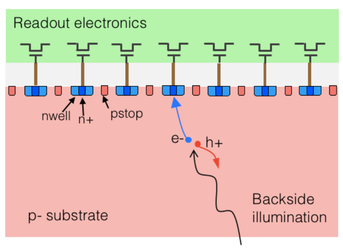
Motivation of SOIAPD for soft X-ray detection.

“ Hybrid pixel detector ”



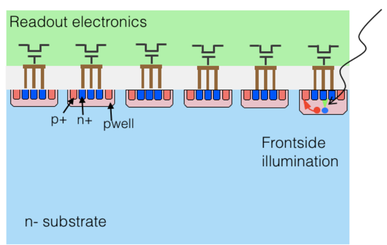
- Bump bonding
- Large pixel
- Complex readout electronics
- Photo diode

“ SOI pixel detector ” without internal gain



- No bump bonding
- **Small pixel**, low material budget
- **‘ SOI-CMOS ’ circuit on pixel**
- Photo diode

“ SOIAPD detector ” with internal gain



- No bump bonding
- **Small pixel,** low material budget
- **‘ SOI-CMOS ’ circuit on pixel**
- **Avalanche photo diode**

APD with readout CMOS circuit on pixel for soft X-ray single photon

❑ SOIAPD operated Linear mode

Normal mode vs. Linear mode

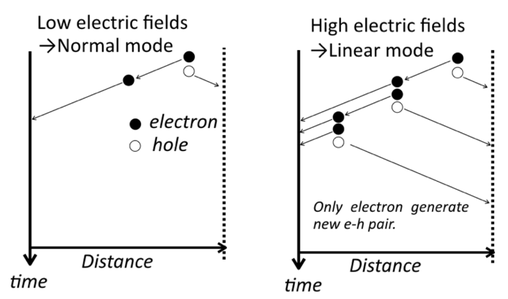
Normal mode (Multiplication Gain=1)

- Regular photon diode
- Operated low electric field bellow

Linear mode (Multiplication Gain~10)

- Operated high electric field around 100 [kV/cm]
- Better S/N and hight sensibility
- Proportional response with the absorbed energy
- Short collection time

Operation mode (Normal and Linear)

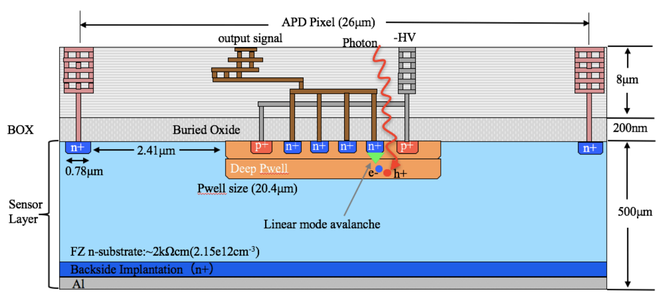


Linear mode operation: proportional response

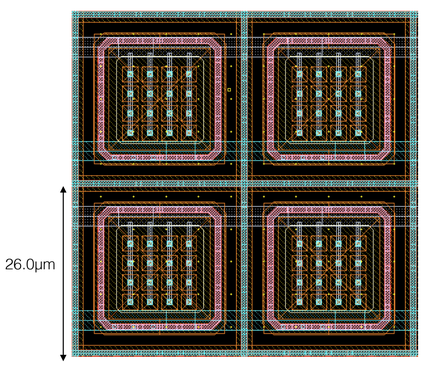
❑ 1st FIN-SOIAPD test chip

1st FIN-SOIAPD **without readout circuit** (fabricated)

10×10pixels with 26μm pixel pitch, The pwell active size is 20.4μm.



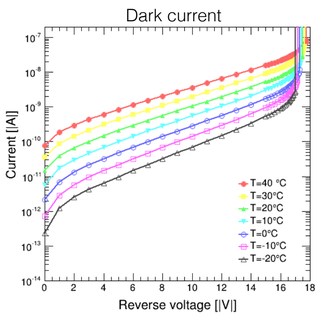
Cross section of 1st FIN-SOIAPD

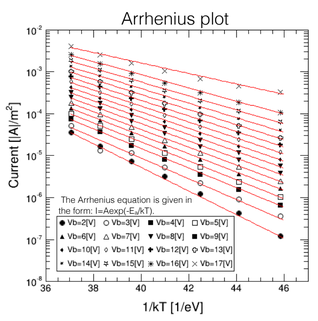


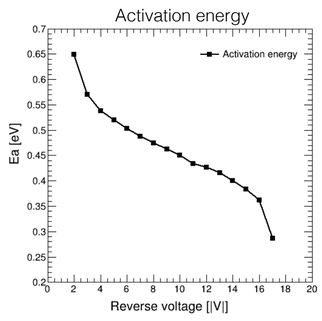
Layout of 1st FIN-SOIAPD (2×2 pixels)

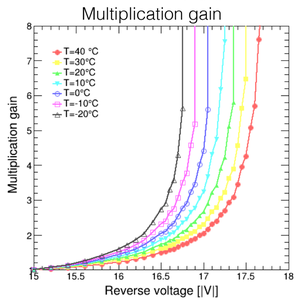
Evaluation

- To investigate the multiplication avalanche gain, photon I-V curve measured at every 10°C from +40 to -20°C.
- The amplification factor is obtained from the following equation, $M=S(V)/S(V_0)$, $S(V_i)=I_{ph}(V_i)-I_{dark}(V_i)$.
- Light characteristics: Wavelength:530nm, LED light intensity:1.42μW.









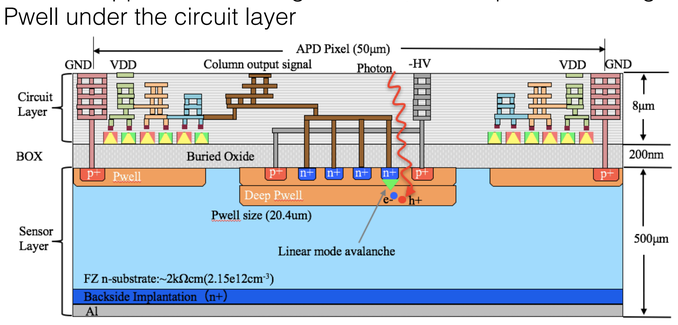
- Breakdown voltage(Vb) was -17.6[V]@20°C.
- The temperature dependence of Vb :dVb/dT~12.32[mV/°C].
- In near Vb, generation term is effective from activation energy.
- Multiplication gain~8.

1st FIN-SOIAPD test chip achieved multiplication gain around 8 times.

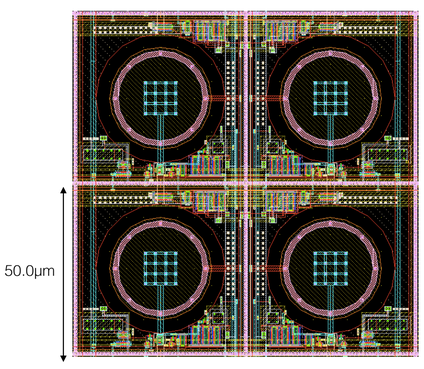
❑ 2nd FIN-SOIAPD test chip

2nd FIN-SOIAPD **with readout circuit** (submitted on Nov.29th, 2017)

To confirm the SOIAPD systems, readout circuit was implemented. 8×8pixels with 50μm pixel pitch.
In order to suppress the back gate effect, a fixed potential was given by Pwell under the circuit layer



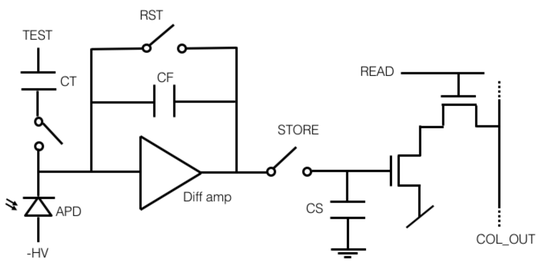
Cross section of 2nd FIN-SOIAPD

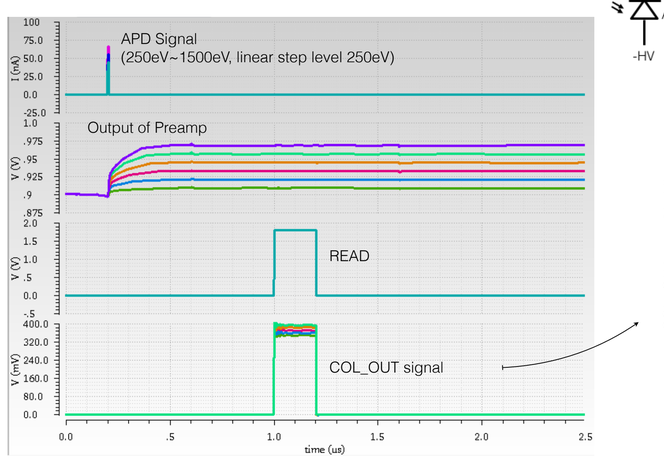


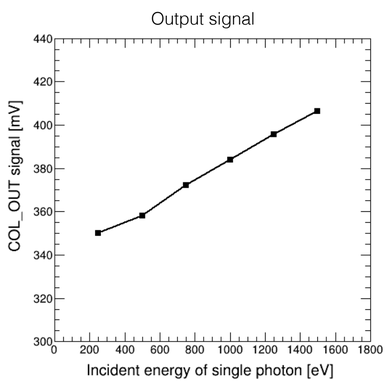
Layout of 2nd FIN-SOIAPD (2×2 pixels)

SPICE simulation

- In order to suppress the back gate effect, a fixed potential was given by Pwell under the circuit layer.
- Differential amp,Feedback cap =4.2fF (DMOS), Cstore = 100fF.







❑ Conclusion

- 1st FIN-SOIAPD test chip using 0.2μm FD-SOI CMOS process was fabricated.
- Photo current-voltage(I-V) characteristics was measured at every 10°C from +40 to -20°C. Vb-17.6[V]@20°C. dVb/dT~12.32[mV/°C].
  Interrupted finger 1st SOIAPD test chip achieved multiplication gain ~8
- 2nd FIN-SOIAPD test chip with readout circuit was submitted.
- In future study, we will evaluate the synchrotron X-ray response from Photon factory. Optimization of pwell concentration and pattern of N+ sense node by TCAD tools.

❑ Acknowledgement & Reference

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