The general performance of source-follower and charge-preamplifier SOI pixel detectors

Roma Bugiel
(AGH University of Science and Technology)
on behalf of the CLICdp collaboration

Chip overview

The presented chip has been fabricated in 200 nm Silicon-On-Insulator (SOI) CMOS technology, in which the handle wafer is separated from the electronics by the burried oxide (BOX) layer. Therefore, the high resistivity handle wafer can act as a radiation sensor with the readout electronics located just above sensor, forming a monolithic detector.

In this design, a general purpose pixel matrix was implemented (can be used either as X-ray detector or as a tracking detector for high energy physics) to study general performance of the SOI structure. The matrix size is 16 by 36 pixels, but in order to test different readout designs, it was splitted into two parts: one with a simple source follower architecture (SF), and the second one with a charge pre-amplifier (CPA) on the input stage (see Fig. 2).
The matrix operates in rolling shutter mode that reduces the dead time to 1%, but it also limits minimum integration time to around 100 us.

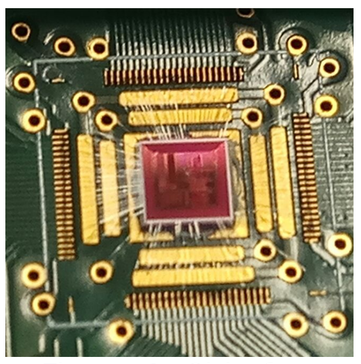

Figure 1. Chip foto

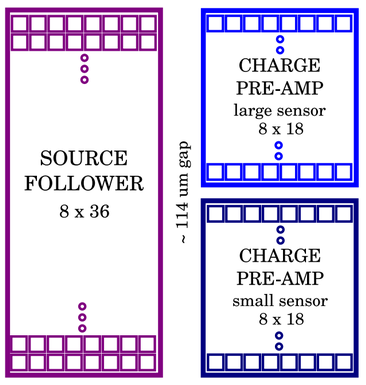

Figure 2. Matrix structure

Pixels design

In Fig. 3 and Fig. 4 schematics of both pixel readouts are shown. For the first one there is only a source follower in the input stage, whereas for the second one a telescopic amplifier with additional current source was used. To maximize the pixel gain a "T-shaped" capacitor structure was used in the feedback, that allows to get small effective capacitance (C_F~6 fF).

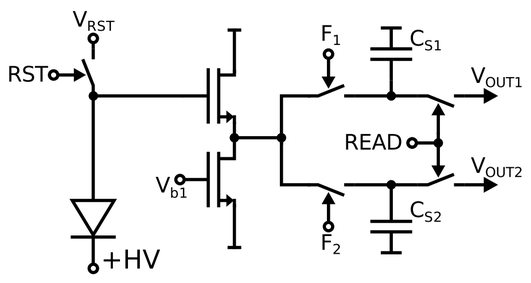

Figure 3. Source follower pixel schematic

In both designs the input stage is followed by the correlated double sampling circuit (F_1 and F_2 switches with storage capacitances C_{S1} and C_{S2}). This allows to store baseline on the first capacitance and baseline with signal on the second one. By using a differential output from the pixel only the signal value is propagated further.

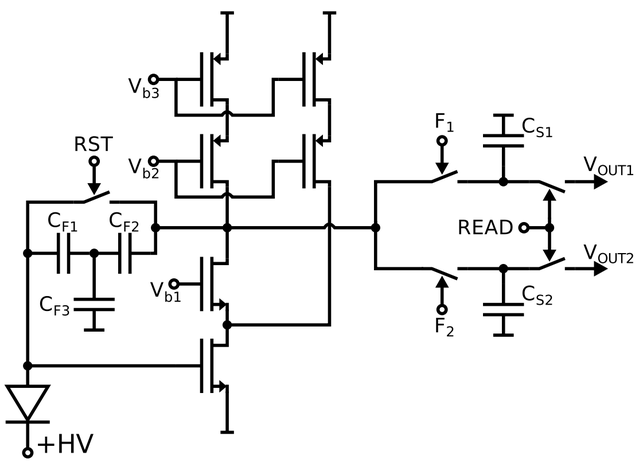

Figure 4. Charge pre-amplifier pixel schematic

For both architectures the pixel size is the same and it is 30 um by 30 um. Charge preamplifiers should not suffer from large pixel capacitance, so two different sensor layouts were used. The first one with the small (5x5um) burried p-well implementation (BPW) in the pixel centre and the second one with BPW over almost whole pixel (29x29um). For the source follower pixel sensor implant was 16x16um what was the minimum size allowing to cover all electronics above the sensor.

Measurements

The presented measurements were performed for two different sensor wafer types: floating zone n-type (FZN) and Double SOI with p-type handle wafer (DSOI). In the Double SOI structure there is another thin silicon layer between sensor and electronics that shields the electronics from sensor electric field.
For each chip the performance characterization was done with the Americium-241 source. The data were collected at room temperature and with the integration time of 100us.
To extract the signal a simple analysis including the pedestal subtraction and clusterization algorithm was applied. The exemplary spectra for each submatrix and each wafer type are shown on Fig. 5. For almost all cases the main X-ray energy lines (59.5, 26.3, 20.7, 17.8, 13.9, 8 keV) are clearly visible, especially for the single pixel clusters.
One can notice that there are two cases for which the performance is much worse and low energy peeks are no longer distinguishable: pre-amplifier pixel architecture with the small sensor implant on FZN wafer and source follower architecture on DSOI wafer. For the first one the performance loss is caused by the influence of the high voltage sensor bias on the electronics left without any shielding layer (no BPW or middle silicon under transistors). Whereas for the second case the reason is in much higher pixel capacitance for DSOI wafer than FZN wafer, which for the source follower pixel architecture leads to signal degradation.

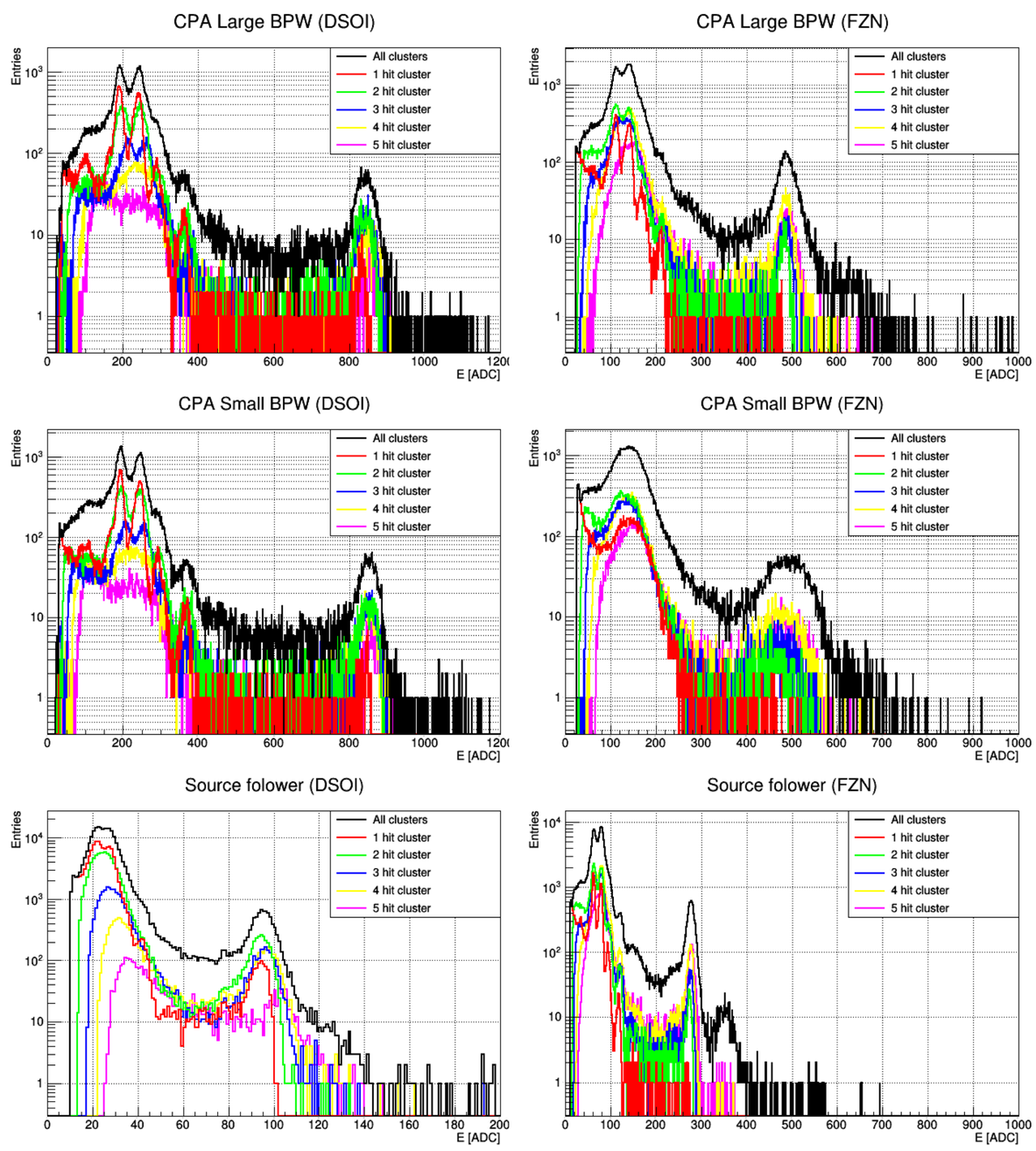

Figure 5. Exemplary Americium-241 spectra for each submatrix and wafer type

Summary

One of the key parameters describing the general detector performance is ENC (equivalent noise charge). Using the energy calibration (based on the Am-241 spectras) for each device the pixel noise was translated into ENC. The final results are shown in table 1. As expected for the Double SOI wafer where the sensor capacitance is significantly larger the best performance was obtained with charge pre-amplifiers and small sensor where the ENC value was 98 e^-. Whereas in case of FZN wafer, the pixel capacitance is only about two times larger than the feedback capacitance in pre-amplifier, so there is less profit from the preamplifier. In fact due to the lower pixel noise of the source follower architecture it shows slightly better general performance with the ENC of 113 e^-.

To conclude, all the results are very promising and further dedicated designs (X-ray, tracking) may become competitive to the current state of the art designs.

Table 1. ENC values for each submatrix

Submatrix \ Wafer	DSOI	FZN
Pre-Amp Large BPW	128 e^-	131 e^-
Pre-Amp Small BPW	**98** e^-	148 e^-
Source follower	321 e^-	**113** e^-