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The general performance of source-follower and charge-preamplifier SOI pixel detectors

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The SOI CMOS technology allows to fabricate monolithic pixel detectors in which the readout electronic and the sensor matrix are integrated on the same wafer. Characterization of a device designed in Cracow and produced in Lapis 0.2 μm Fully-Depleted, Low-Leakage SOI CMOS technology was performed. The tested matrix consists of two pixel types: source-follower and charge-preamplifier architecture. In addition, the charge preamplifiers are designed with two different sensor layouts. The whole matrix comprises an area of 16×36 squared pixels of 30 micron pitch. The detector is read out in rolling shutter mode.
In this presentation, the performance and measurement results of the prototypes produced on high resistivity floating zone (FZ-n) and novel Double SOI wafers are presented. Using Am^{241} and Fe^{55} radioactive sources the detector calibration was done and the noise was measured, giving the ENC (Equivalent Noise Charge) of about 100 e^{-}. In addition, the leakage currents were measured showing several pA per pixel for FZ(n) and almost zero (below 0.1 pA) for Double SOI.

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