# Monolithic Pixel Development in TowerJazz 180nm CMOS for the outer pixel layers in the ATLAS experiment

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On behalf of
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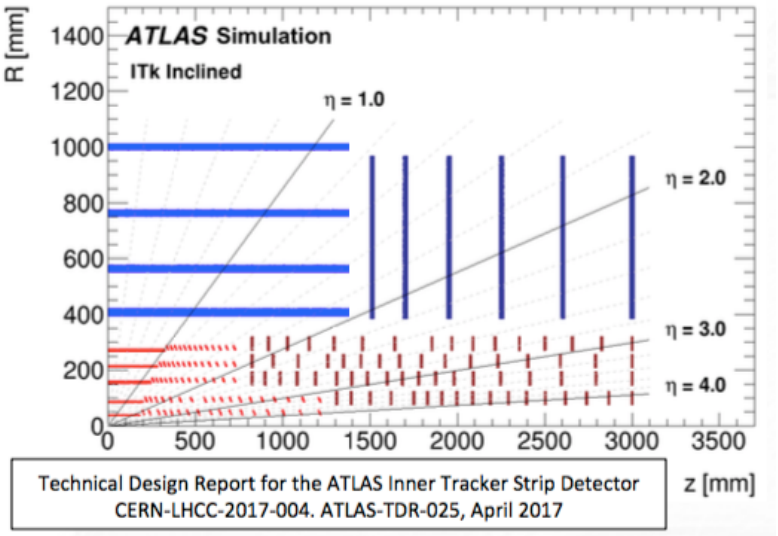
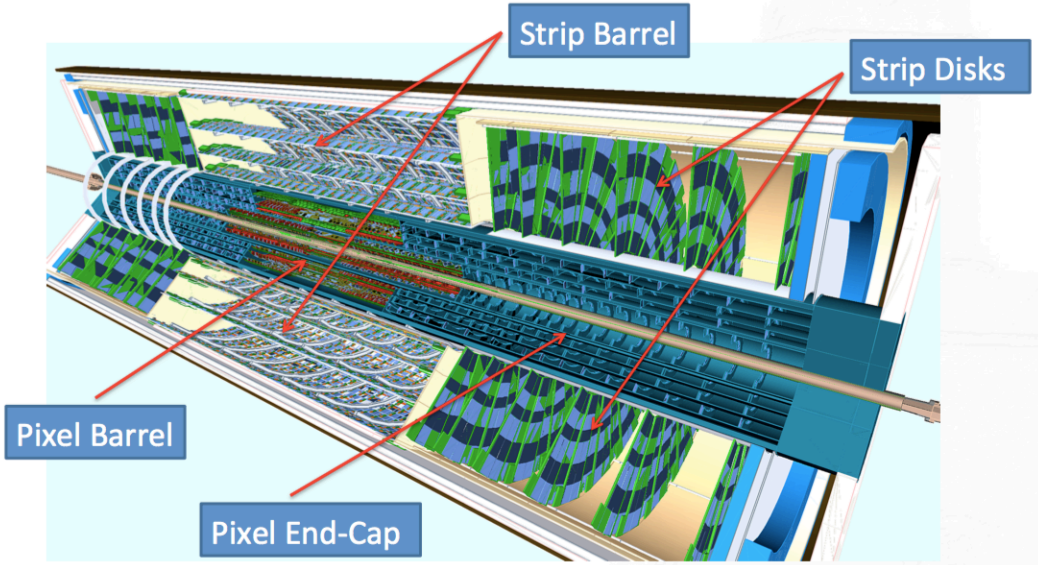
# ATLAS ITk Pixel Detector



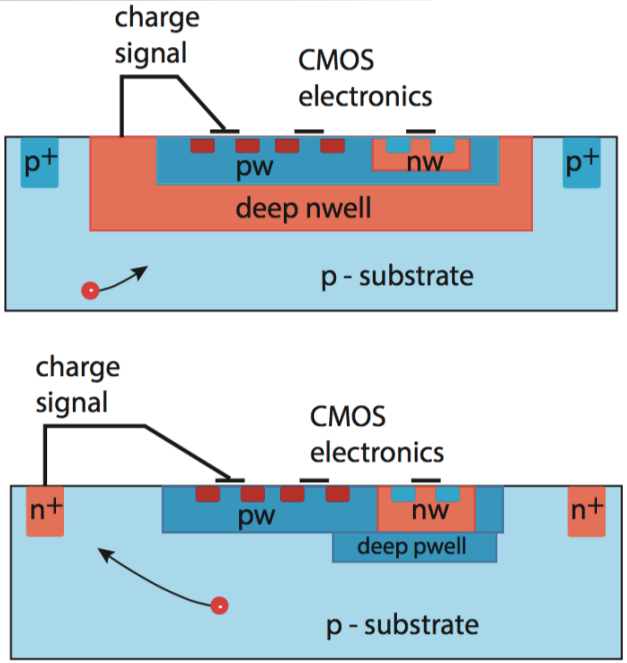




- All silicon design to replace present ATLAS Inner Detector for HL-LHC
- η coverage increased from 2.5 to 4
- Itk Pixel: 5 pixel barrel layers and 5 pixel rings
- 10,000 modules with 12 -14 m2 of pixel detectors
- Design of the pixel part is being finalized: inclined layout optimization

# Radiation hard CMOS sensors

**Advantages over "classic" n-in-n/n-in-p sensors or traditional Monolithic Active Pixel Sensors (MAPS)**

- Full CMOS allows complex electronics in active area of pixel matrix
- Thin and high-resolution trackers
- **Large depleted volume increases sensitivity and provides efficient detection after irradiation**




Kolanoski, Wermes / Springer 2016

**ATLAS CMOS Development Collaboration**

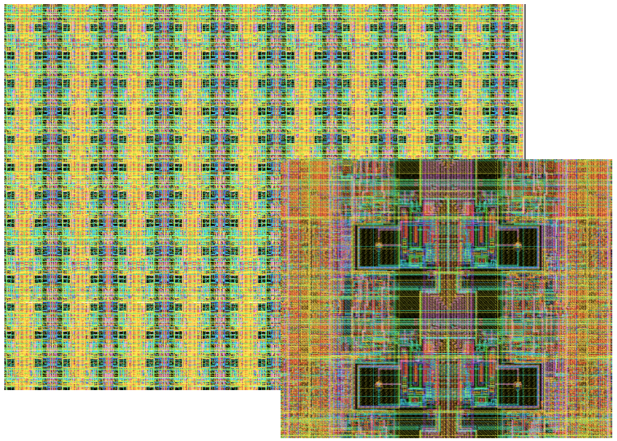
- 25 institutes – RD on radiation hard CMOS sensors since 4 years
- Monolithic CMOS sensors are developed as option for the **outermost ITK Pixel Barrel layer**

- CMOS is much higher volume and lower price than our present silicon sensors due to high volume and larger wafers
- CMOS Modules costs ~ factor ~4 less than hybrid (no bumpbonding, no extra FE-chip)

# ATLAS CMOS sensors

## TowerJazz

- Two large scale demonstrators MALTA and Monopix:
  - 20x20mm and 20x10mm
  - Focus on small electrodes
  - MALTA: Asynchronous matrix readout (no clock distribution over the matrix)
  - MonoPix : Column Drain Read-Out

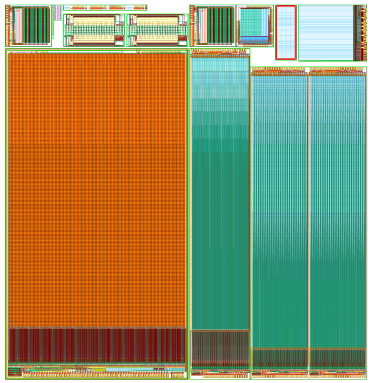


- Small electrode design

## AMS

ATLAS (monolithic)

- Additional production step – isolated PMOS
- 80 and 200 Ohm.cm wafers
- Reticle Size about 21mm x 23mm

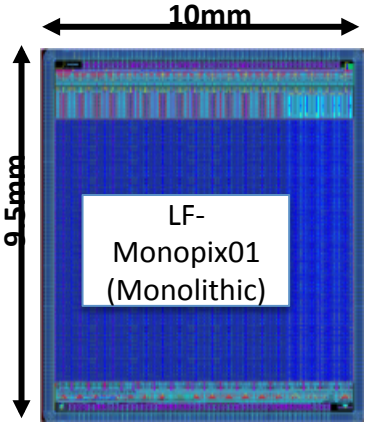


See talk by I. Peric

## LFoundry

Monopix01, LF2 and Coolpix1

- Received Apr. 2017
- "Demonstrator size"
- 50 x 250 $\mu m^2$ pixels
- Fast standalone R/O




See talk by T. Hirono

Sensors with large eletrode designs

# CMOS for Future Trackers

- **CMOS sensors for ATLAS: Radiation hardness, response time, hit rates**

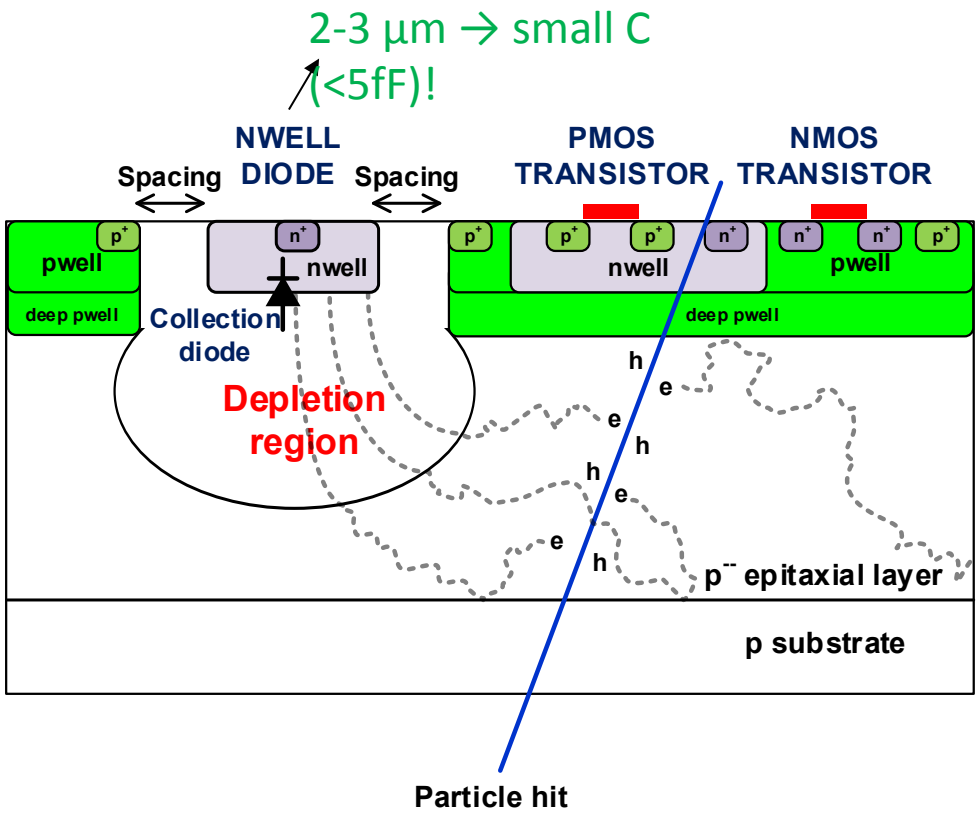
| | ALICE ITS | ATLAS Outer Pixel | ATLAS Inner Pixel |
|---|---|---|---|
| NIEL [$n_{eq}/cm^2$] | $10^{13}$ | $10^{15}$ | $10^{16}$ |
| TID | <1Mrad | 80 Mrad | 2x500Mrad |
| Response Time [ns] | 2000 | 25 | 25 |
| Hit rate [$MHz/cm^2$] | 10 + SF | 100-200 | 2000 |

Key parameters need factor up to ~100 Performance gain

- **Collect signal by drift through fully depleted sensor (DMAPS)**:
  - TowerJazz developments in close collaboration with ALICE and ATLAS for optimzed processes towards radiation hardness
- **Dedicated designs** for high hit rates and fast response
  - New architecture developments to cope with high hit rates
- **CMOS** sensor post processing and **module integration**
  - Large area module concept and new interconnects technology for dedicated CMOS modules

# Sensor technology

- TowerJazz **180nm CMOS imaging process** (6 metal layers)
- **High resistivity** (> 1kΩ cm) p-type epitaxial layer (25 µm thick)
- **Deep PWELL** shielding NWELL allowing in-pixel PMOS




**Large Q/C**

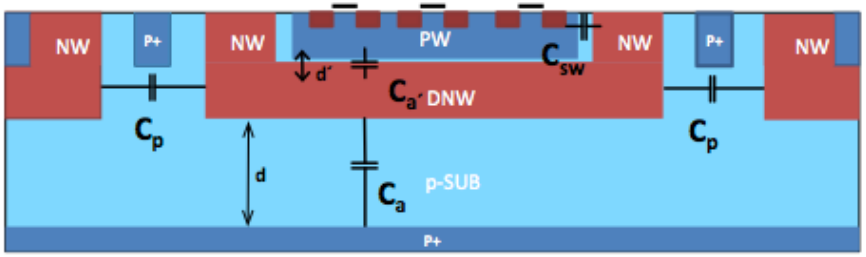
- **better analog** performance
- **lower power** consumption

- Reverse bias to further reduce input capacitance and increase depletion volume (still difficult to deplete under deep PWELL)

# Input capacitance is critical

- On sensors with large electrodes the **analog & digitial circuit is placed inside collection well**
- Input capacitance is dominated by additional capacitance between n-well and p-well

Hybrid planar pixels (e.g. ATLAS IBL): **Cin = 109 fF**
(Havranek et al, NIMA 714 (2013) 83-89
CMOS pixel extrapolation: **Cin ≈ 200 fF**




H. Krüger / Bonn

- Response time:

$$\tau_{CSA} \propto \frac{1}{g_m} \frac{\mathbf{C_d}}{C_f}$$

- Noise:

$$ENC^2_{thermal} \propto \frac{4}{3} \frac{kT}{g_m} \frac{\mathbf{C_d^2}}{\tau}$$

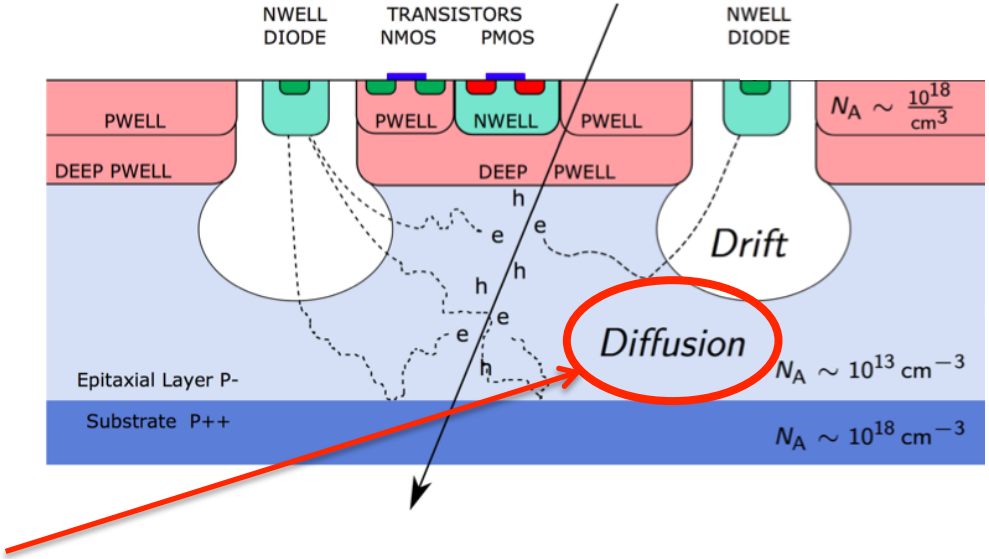
**Total input capacitance drives peaking time and ENC**

Counteract by increasing transconductance – but this increases power consumption significantly

- Additionally digital signals are contained in collection well – hence risk of severe cross-talk of digital signals to collection well
  - Can be minimzed by special source follower-> see talk by T. Hirono

# Limitations

- For tracking MAPS appear to be the ideal detector
- BUT…
- **Diffusion is the limiting factor:**
- At high radiation (>$10^{14}$ to $10^{15}$ $n_{eq}/cm^2$) ionization charge is trapped in non-depleted part – No more signal
- Diffusion makes signal collection slower than typical requirements for pp-colliders

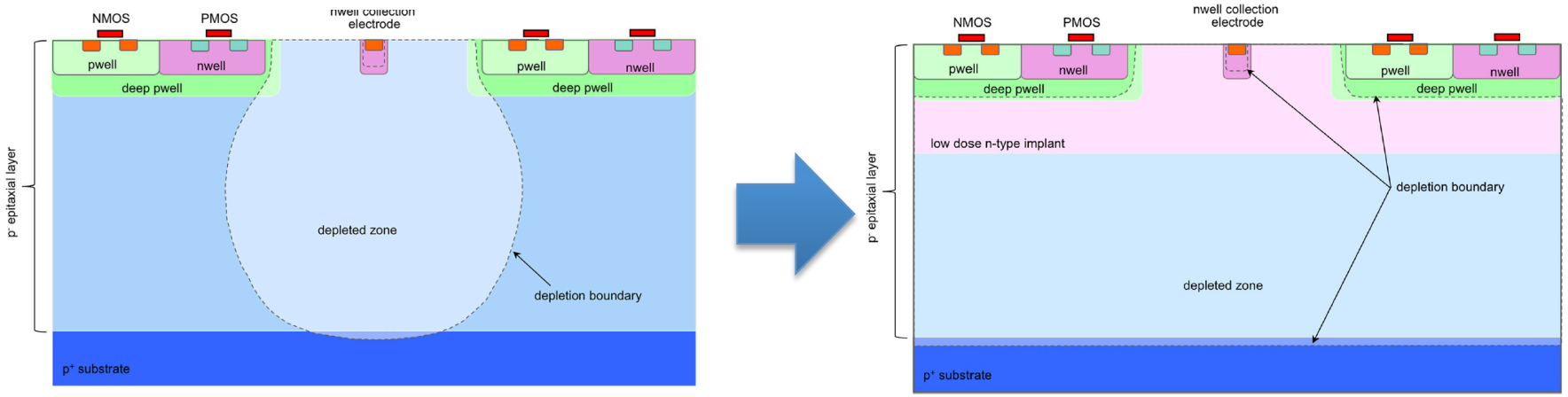



- Readout architectures are low power but not designed for high hit-rates like pp at HL-LHC

# TJ 180 nm modified process

- Novel modified process developed in collaboration of CERN with TJ foundry, originally developed in context of ALICE ITS
- We carried out initial charge collection studies at HL-LHC radiation levels (~$10^{15} n_{eq}/cm^2$) to study a possible application towards ATLAS ITk
- We pursue novel designs in this process to meet ATLAS requirements for ITK Pixel

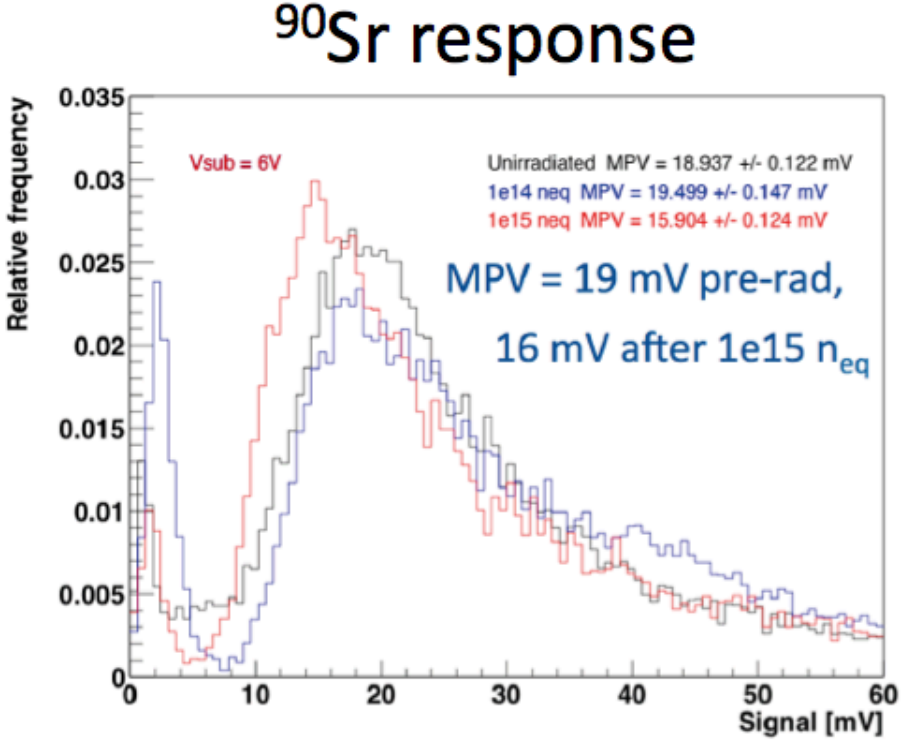
W. Snoeys et al. DOI 10.1016/j.nima.2017.07.046

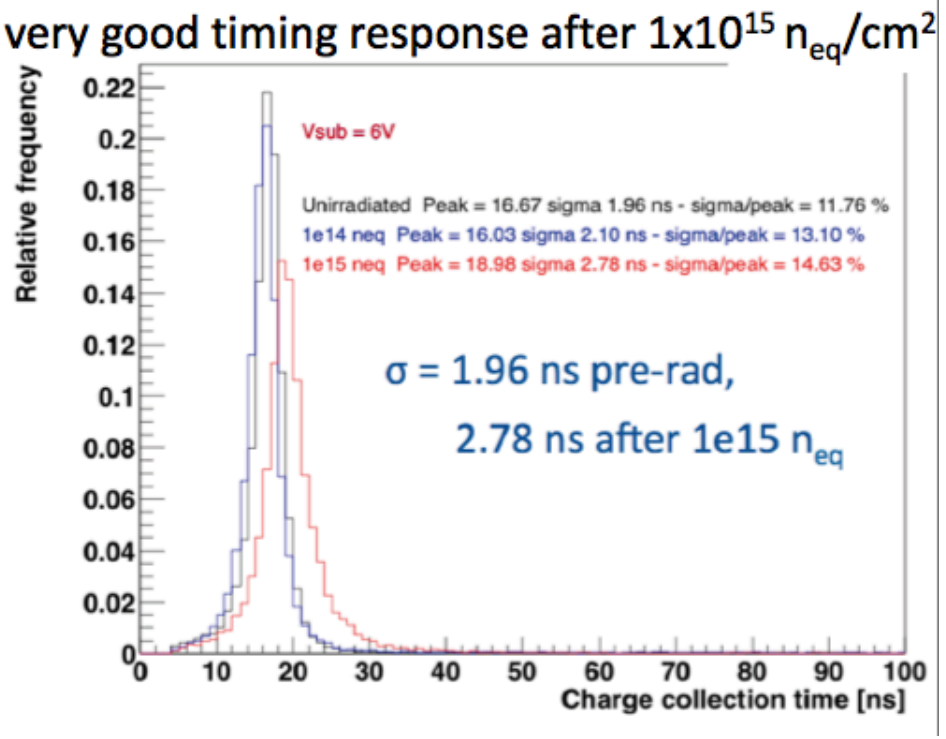



- Adding **a planar n-type layer** significantly improves depletion under deep PWELL
- Increased depletion volume → **fast charge collection by drift**
- better time resolution reduced probability of charge trapping (**radiation hardness**)
- Possibility to fully deplete sensing volume with no significant circuit or layout changes

# First Irradiation tests for HL-LHC

- TowerJazz 180nm Investigator sensor with small electrodes
- Neutron irradiated at Triga Reactor Slovenia
- Measure charge collection before and after irradiation

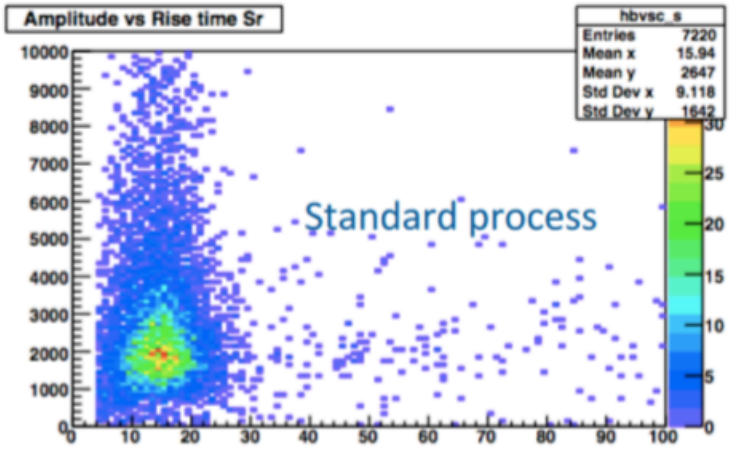


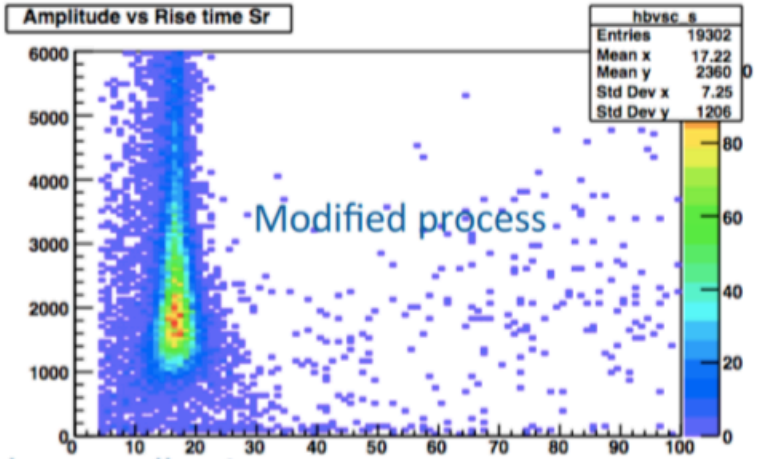




H. Pernegger et al 2017 JINST 12 P06008

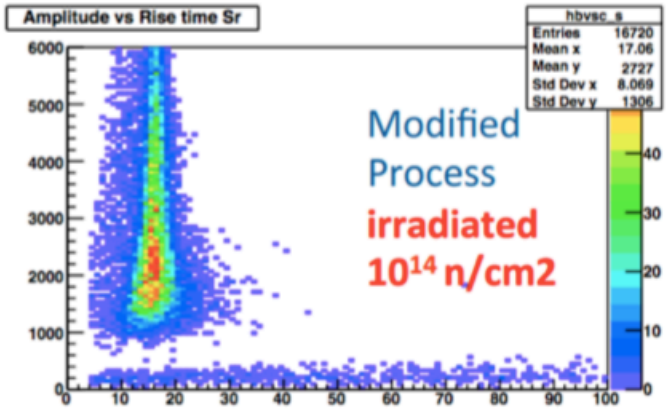
# Charge versus collection time

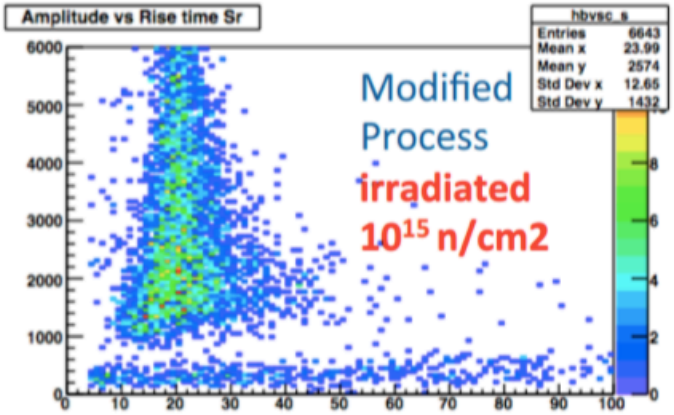
- Calibrated charge signal in $^{90}Sr$ source tests
  - Calibration of mV to e- by $^{55}Fe$ source tests and
    - Better timing with modified process (narrower collection time distribution)



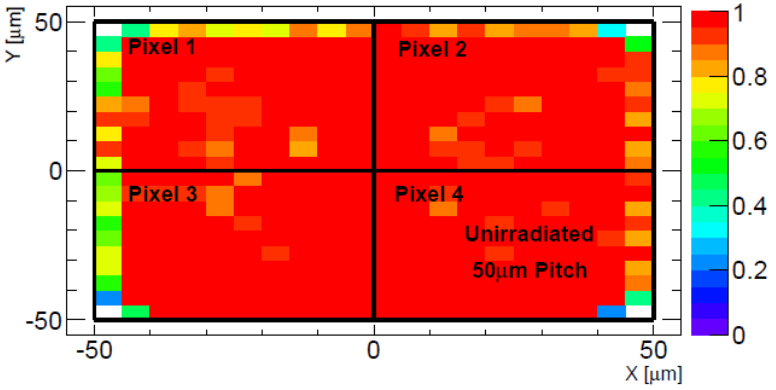

    - Modified process after irradiation maintains charge collection

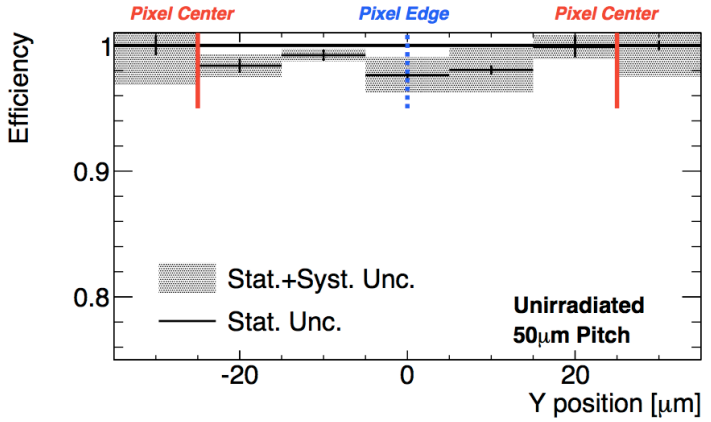


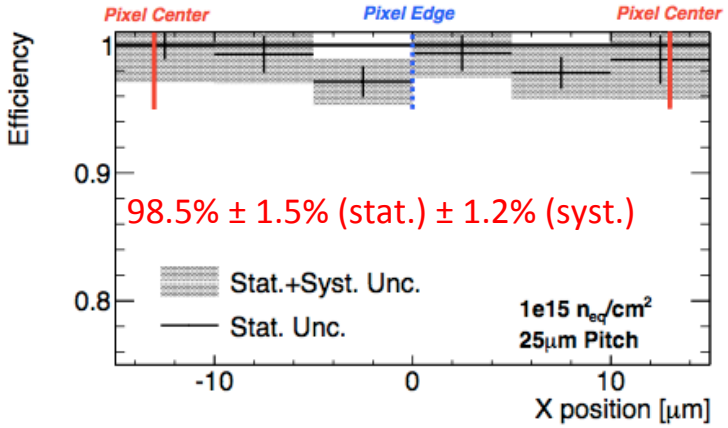
# Beam test results

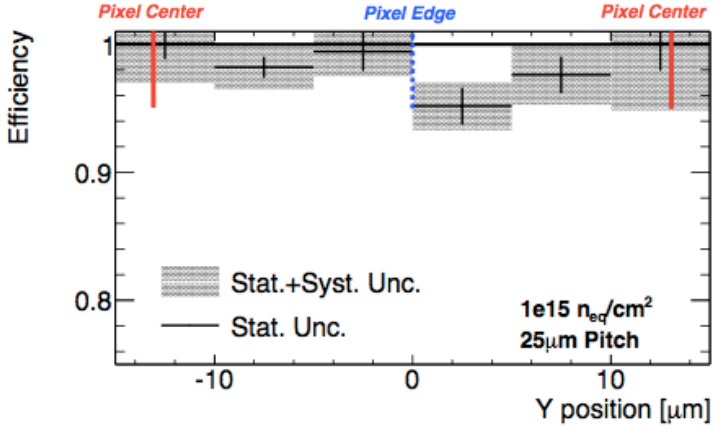
- Unirradiated sensor efficiency 98.5% ± 0.5% (stat.) ± 0.5% (sys.) (50x50 μm²)



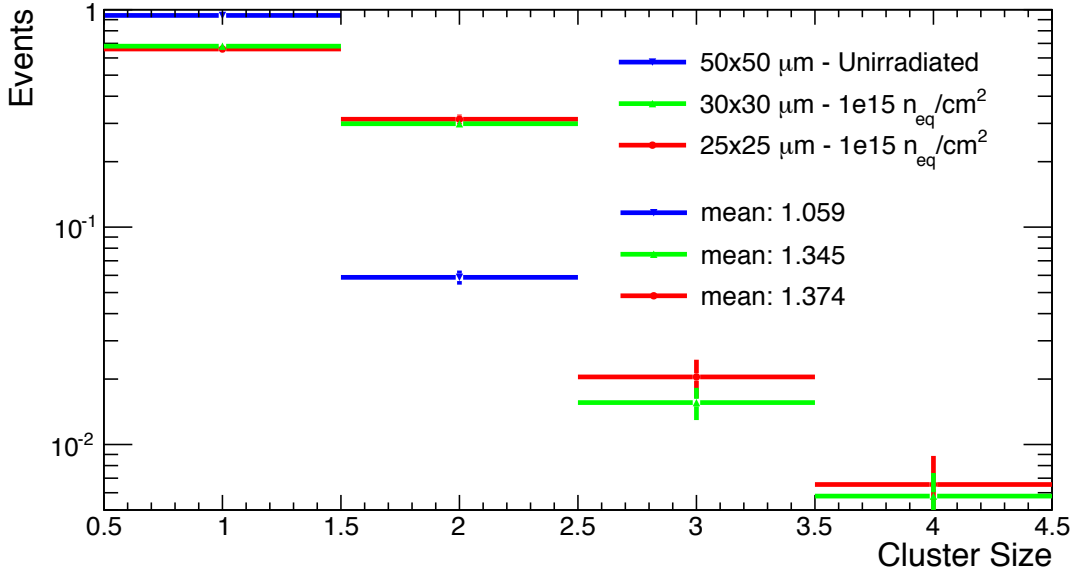

- Irradiated sensor also shows uniform efficiency across 25x25 μm² pixel



# Cluster size in beam & source tests

- Unirradiated 50x50um and $10^{15}$ n/cm$^2$ irradiated 25x25 and 30x30um pixel sensors in beam tests:

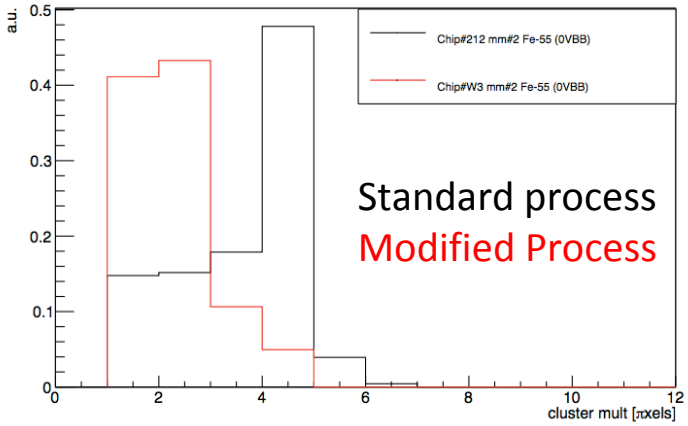



- Mean ~1.3 for 25x25 and 30x30um
- Spacing between DNW and DPW also influences charge sharing
  - 25x25 and 30x30um have spacing 3um
  - 50x50 has spacing 18.5um

20x20μm pixel pitch

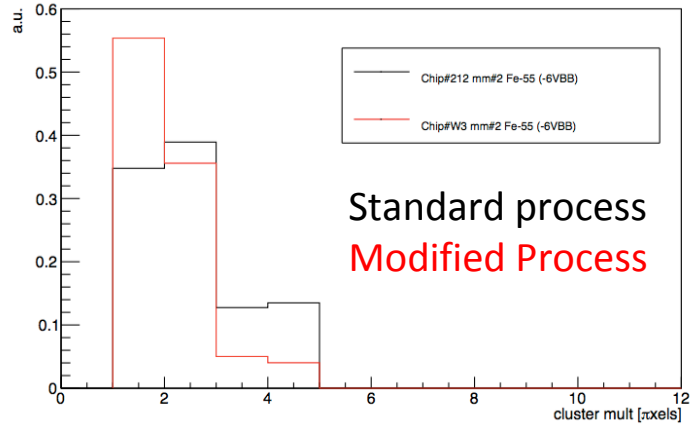
$V_{BB} = 0$ V

cluster mult plane_0,




$V_{BB} = 6$ V

cluster mult plane_0,




Jacobus van Hoorne ALICE/ITS

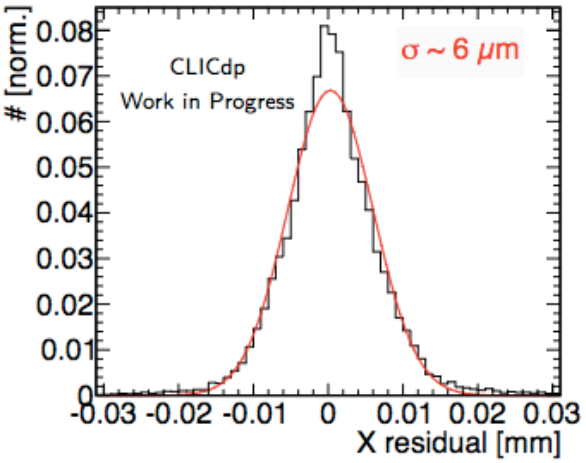
# Spatial & Time resolution

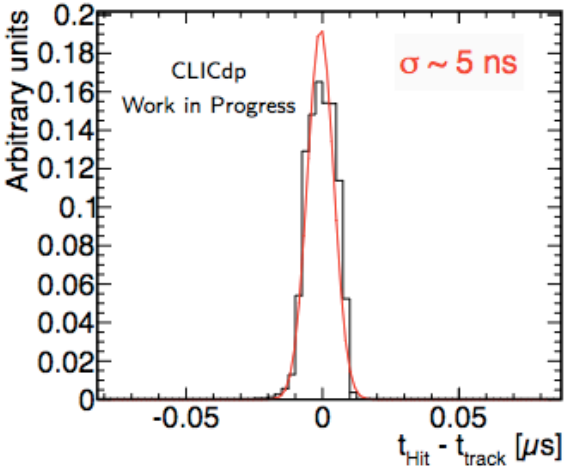
- Modified process unirradiated 28x28μm pixel sensors studied in beam tests with CLICdp TimePix3-telescope as development for the CLIC tracker:

## Resolution in space and time

A. Nürnberg , M. Munker
TREDI 2017 , Trento
https://cds.cern.ch/record/2284145

- 28 μm pixel size, 6 V bias, modified process



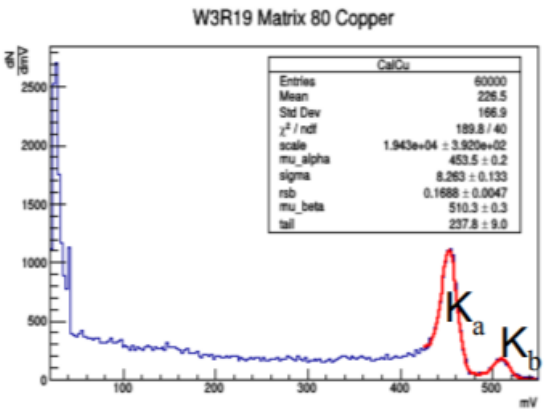

- Compare extrapolated track impact position to reconstructed position
- Spatial resolution ~ 6 μm, telescope resolution not unfolded

- Compare extrapolated track time to reconstructed time
- Timing resolution ~ 5 ns, dominated by the 65 MHz sampling of the readout

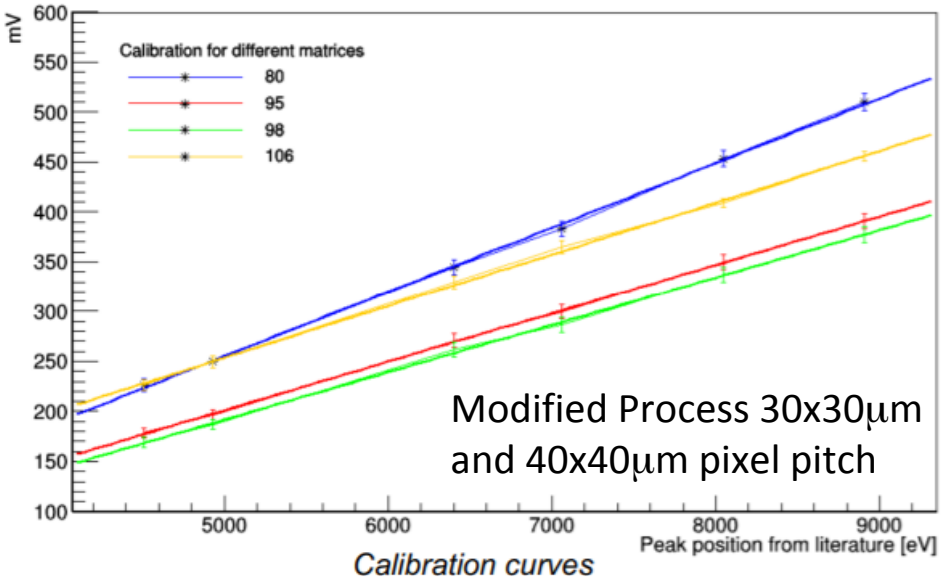
# Fluorescence X-ray: Calibration

- X-ray source with Ti, Fe, Cu targets for multi-energy X-ray tests:
- Used to optimize design of analog front-end circuit for best SNR

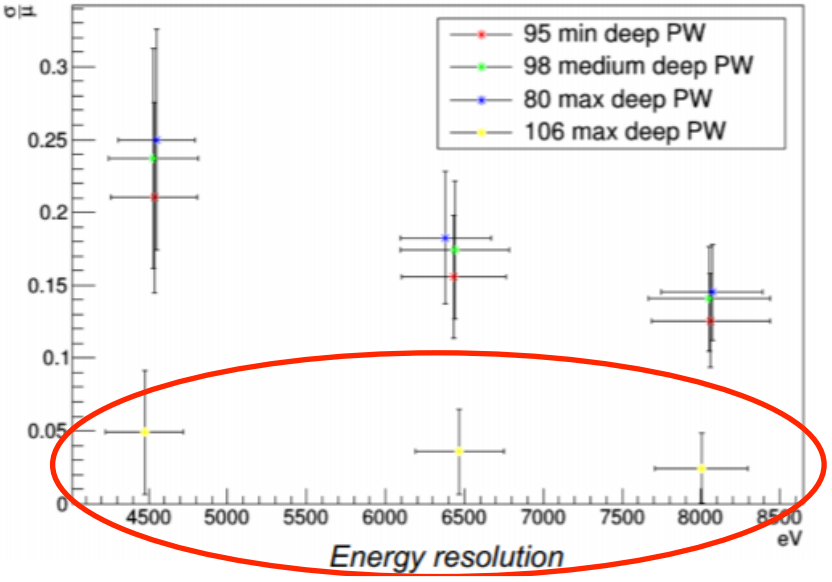
- $K_\alpha$ and $K_\beta$ peaks clearly separated
- Good energy resolution of $\sigma$~3.5% - 5%
- Due to very low capacitance (<5fF)



*Typical charge spectrum*



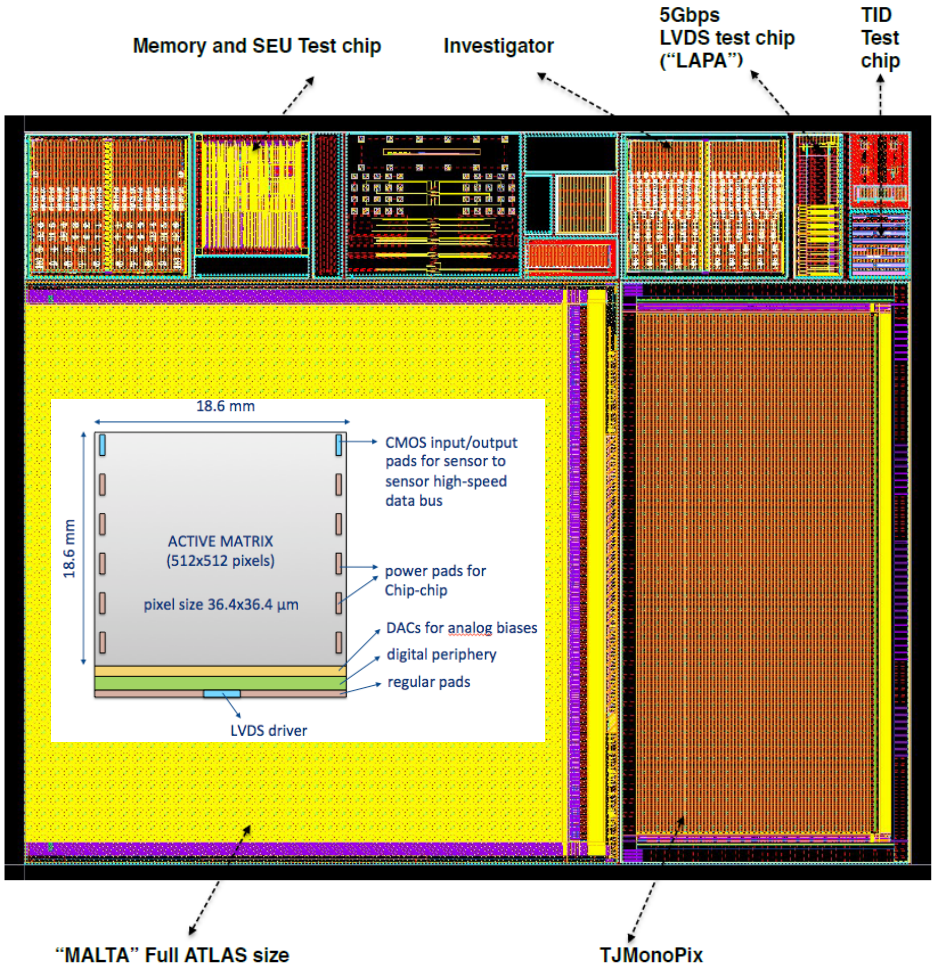
*Calibration curves*



*Energy resolution*

# TJ MALTA for ATLAS

- **Monolithic pixel sensor for the outer layers of the ATLAS Itk Pixel outer layer**
- Uses TJ180nm modified process
- **Full-scale demonstrators** with different readout architectures and optimized analog performance
  - MALTA: 20x22 mm (full size)
  - MonoPix : 20x10 mm (half size)
- **The ATLAS "MALTA" chip**
  - **Novel asynchronous readout** architecture for **high hit rate** capability with 40bit parallel data bus for streaming
  - Features Sensor-to-Sensor high-speed signal transmission
  - Chip-to-Chip power distribution




Lead design: CERN

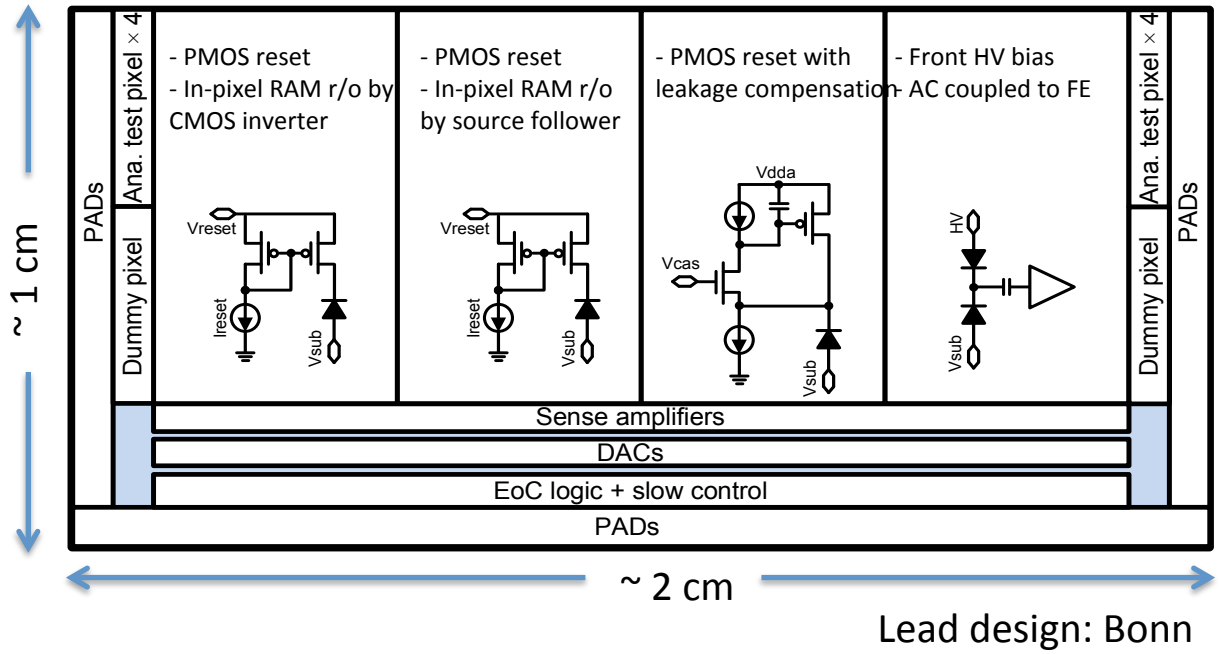
Currently in production and will receive chip back in January

# The “TJ-Monopix” chip

- MALTA and MonoPix are designed for minimal capacitance
- TJ Monopix FE based on “MALTA” front-end modified to provide ToT information
- Well established column-drain architecture:
  - Time stamp distributed in pixel array
  - Hit information stored in the pixel
  - Hit read out following a priority scan

T. Wang et al.
iWoRiD 2017

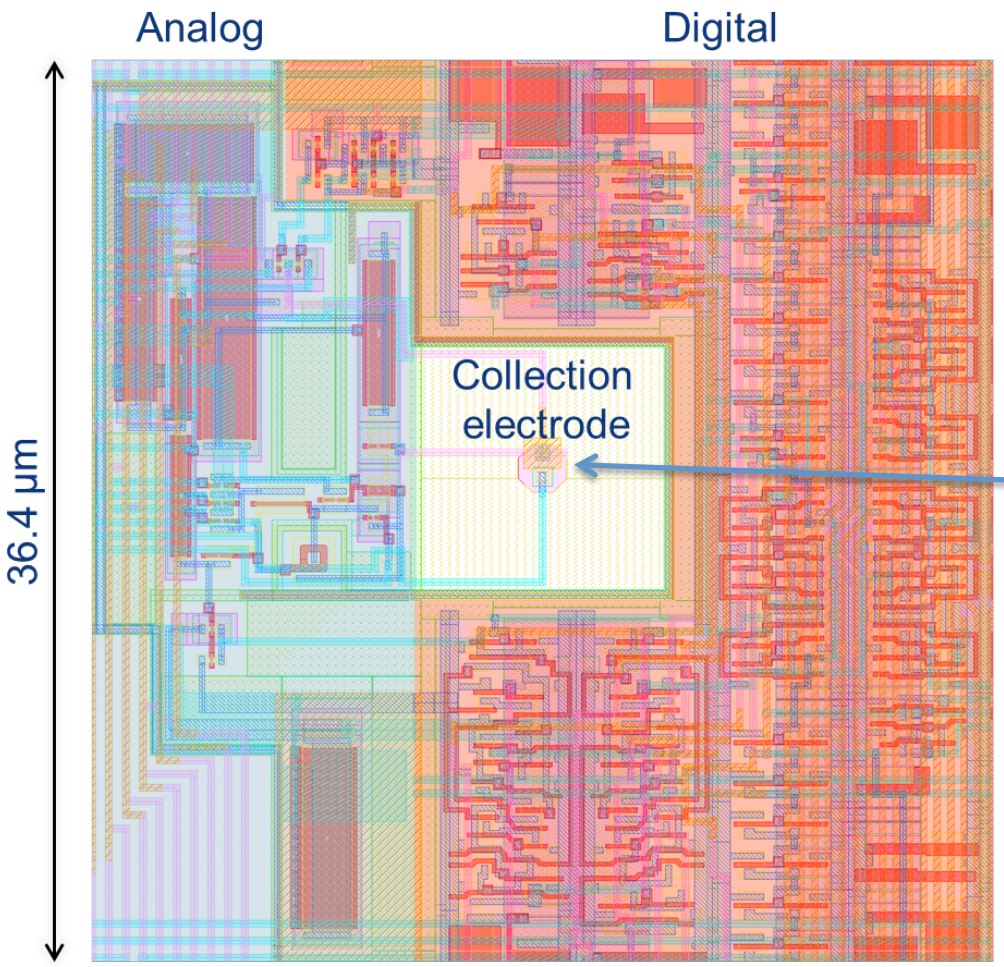
K. Moustakas
IEEE NIST
2017




Lead design: Bonn

# “MALTA” pixel

- Analog front-end and digital readout architecture separated inside the pixel

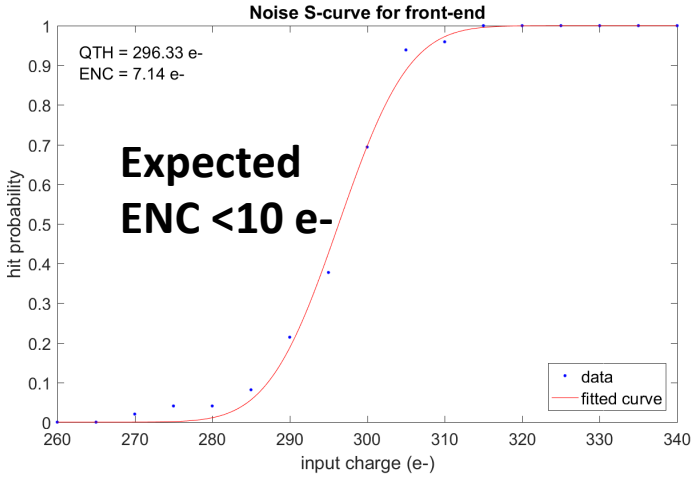


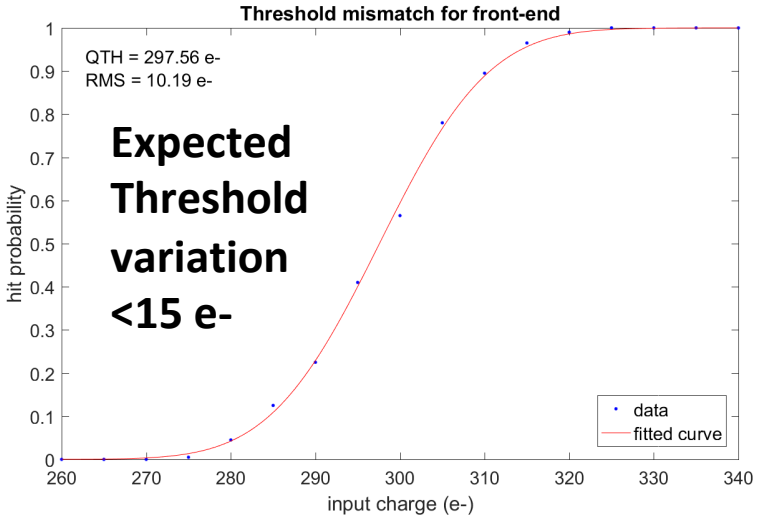

- Charge collection electrode separated from circuitry to avoid additional noise from cross-talk
- Small diameter electrode (3um diameters) to achieve minimal capacitance (<5fF)
- Analog power: bias current 500nA/pixel or <70mW/cm$^2$

# ENC Noise and Threshold

- Noise and transistor mismatch cause a variation in the charge threshold of the front-end (S-curve)

threshold/noise > 10 ✓




delay of rising edge (ns)

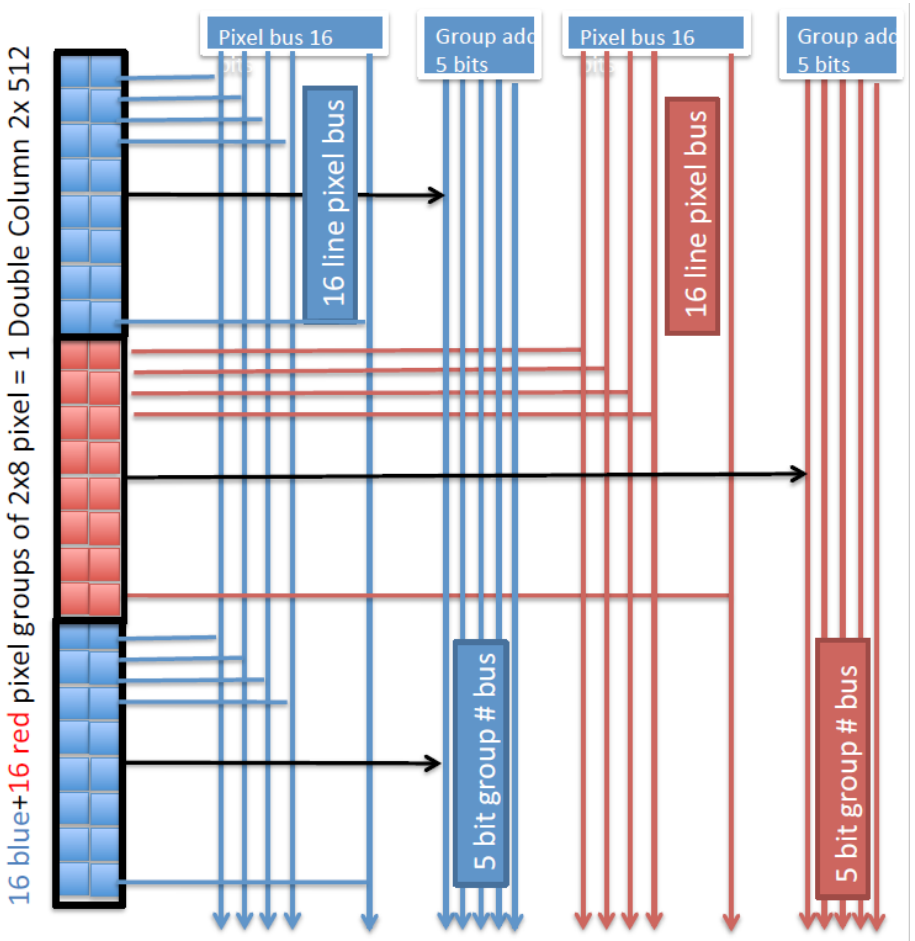

good threshold uniformity due to low capacitance

no need for in-pixel tuning

# Digital readout architecture

- Front-end output injected into double-column digital readout logic
- Hits are stored using in-pixel flip-flops and **transmitted asynchronously over high-speed buses to the end-of-column logic** (digital periphery)
- **No clock distribution** over the active matrix – **reduces power consumption**!

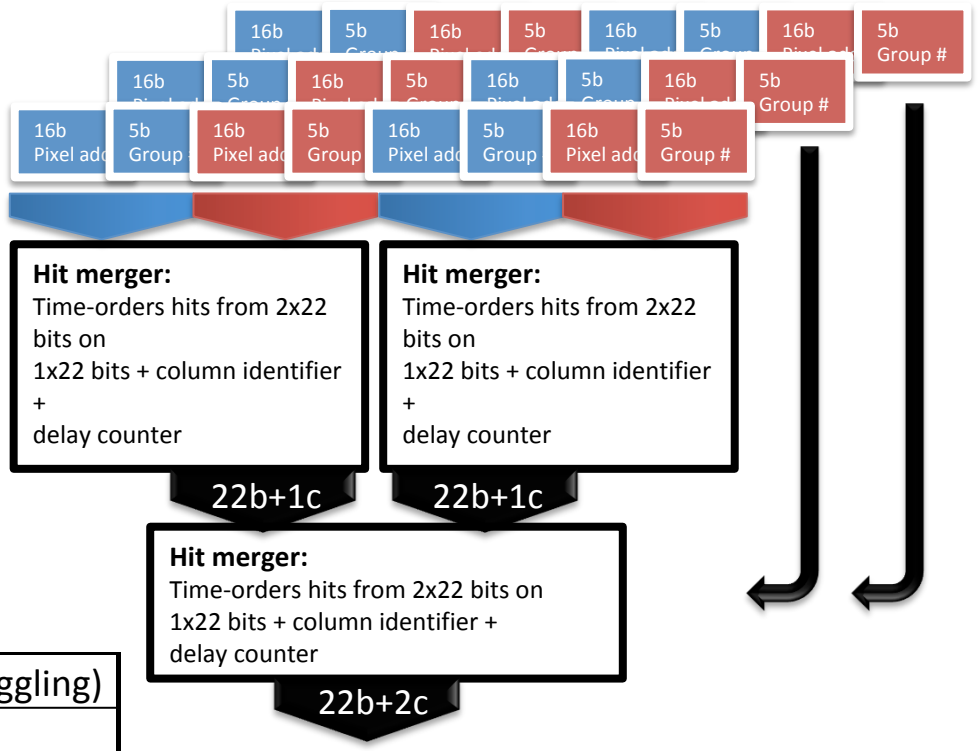
- Double-column divided into groups of 2x8 pixels ("red" and "blue")
- Buses shared by all groups of the same colour in the double-column
- Group number encoded on 5-bit group address bus



# MALTA Digital end-of-column logic

- At the periphery, signals of groups are merged together
- Simultaneous signals on two buses require additional arbitration logic
- Merging is repeated for all the double-columns and then continued until all outputs are merged into one parallel bus
- Digital power in matrix: Only 2.5 mW/cm$^2$ for outer and 80mW/cm$^2$ doe innermost layer

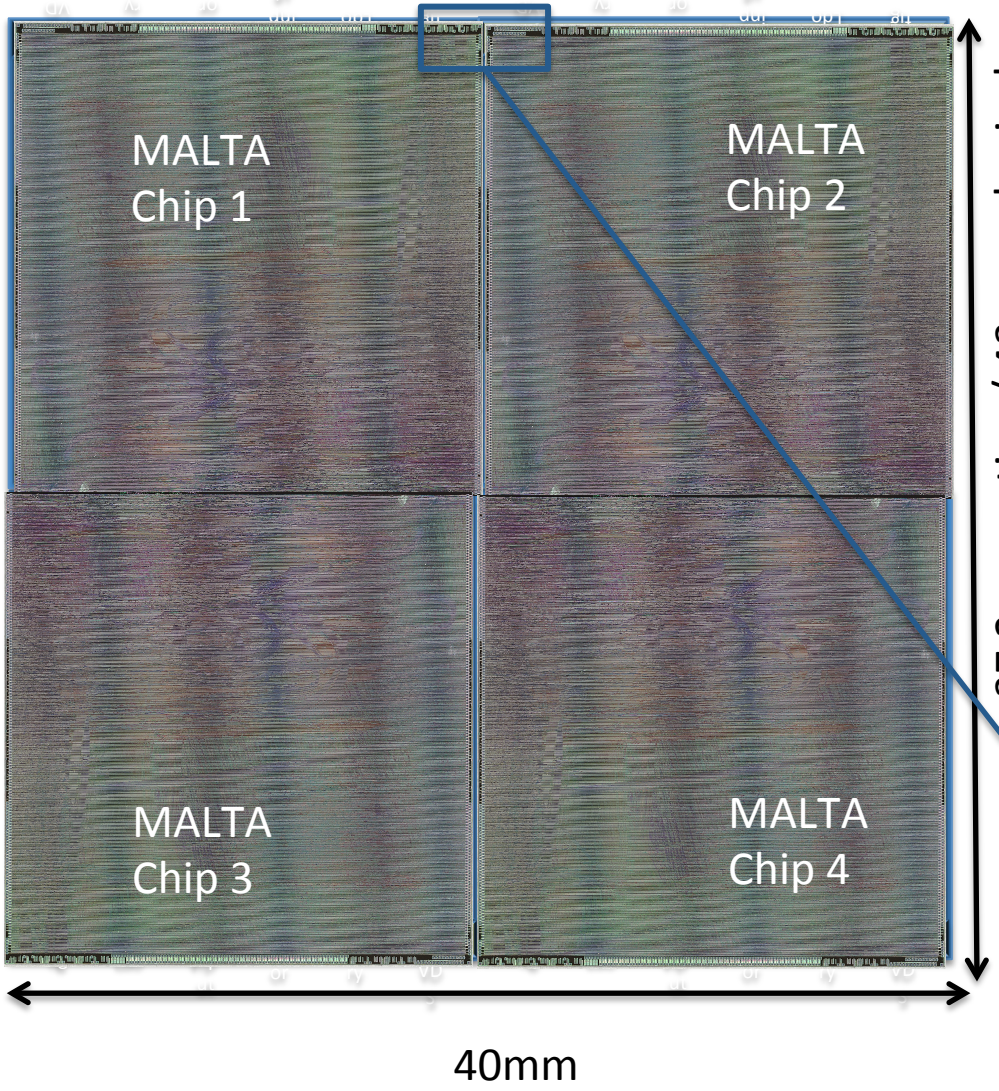
x256 double-columns




| | pixel hit rate | | Power (4.5 bit toggling) |
|---|---|---|---|
| Layer | hit/BC/mm$^2$ | Mhit/mm$^2$/s | mW/cm$^2$ |
| 0 | 0.68 | 27.2 | 79.6 |
| 1 | 0.21 | 8.4 | 24.6 |
| 2 | 0.043 | 1.72 | 5.0 |
| 3 | 0.029 | 1.16 | 3.4 |
| 4 | 0.021 | 0.84 | 2.5 |

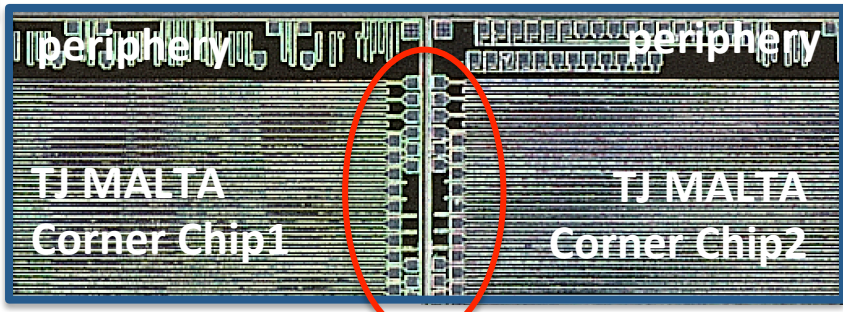
Novel asynchronous readout architecture for high hit rate capability with 40bit parallel data bus for data streaming

# ATLAS CMOS Module (MALTA)




- CMOS Module is assembly of "Quad" or "Double" chip arrangement
- Do not consider stitching for CMOS modules
- Aim at minimal gap region
- Trial assemblies in preparation with TJ- MALTA

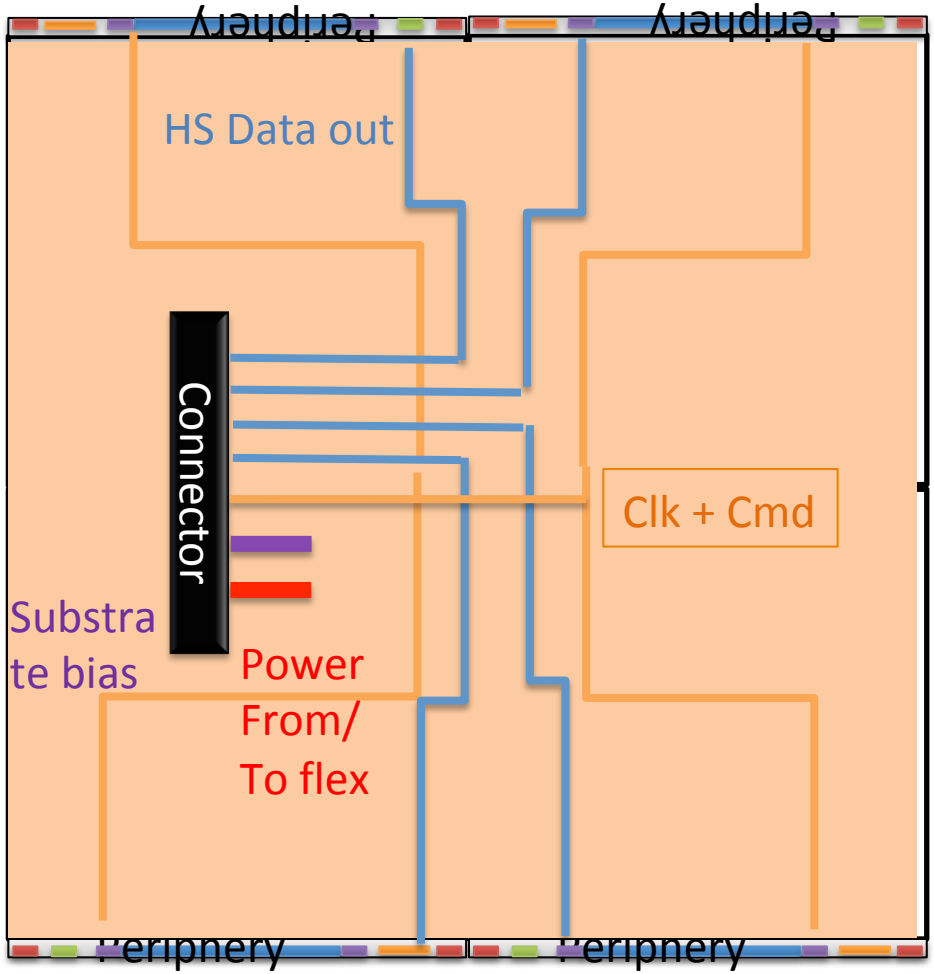
Corner area between 2 chips:



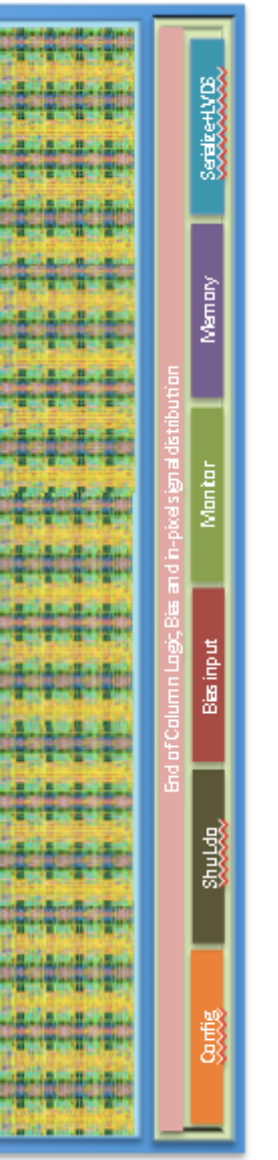

Chip-to-Chip data interconnection

# CMOS Quad Module for ITk

- Module flex
  - Carries 4 (2) pairs of LVDS outputs to connector and “aggregator” and receives Clk and CMD
  - Module powering through serial powering



# “ATLAS CMOS-1” Periphery




**Currently design ATLAS-CMOS-1 in TJ to implement full periphery needs for ATLAS ITK outermost layer:**

**Key topics : Hit data Memory and Trigger**

- Analysing memory design in order to efficiently use bandwidth, distribute power and use little space
- Consider to “pack” hit information of multiple hits into “clusters” to achieve more efficient storage

**Key topics : Serializer and output**

- Data out after trigger is serializer with 640 / 1280 Mbps (Data output is LVDS driver with pre-amphasis) - on sensor PLL
- Clk/CMD 160MHz to receive from aggregator chip

**Key topics : Power and bias**

- Prepare designs to generate bias voltages internally
- Serial power: TSMC65nm circuits can generate 1.8 but is ~120cm away (V-drops and regulation) -> consider to use on CMOS sensor Shuldo for serial powering

# Summary & Outlook

- We have investigated the radiation hardness of for monolithic active pixel sensors produced with a **modified process in TowerJazz180nm** to develop a monolithic CMOS sensor with a **small collection electrode while maintaining radiation tolerance**.

- Measurements in irradiated prototypes **up to $10^{15}$ n/cm$^2$** showed **nearly unchanged signal response and depletion of the epi layer.**

- Two large-size chip designs, **TJ MALTA and MonoPix** have been prepared to develop this approach towards radiation hard **monolithic CMOS sensors as an option for the ATLAS ITK Pixel Outer Layers**

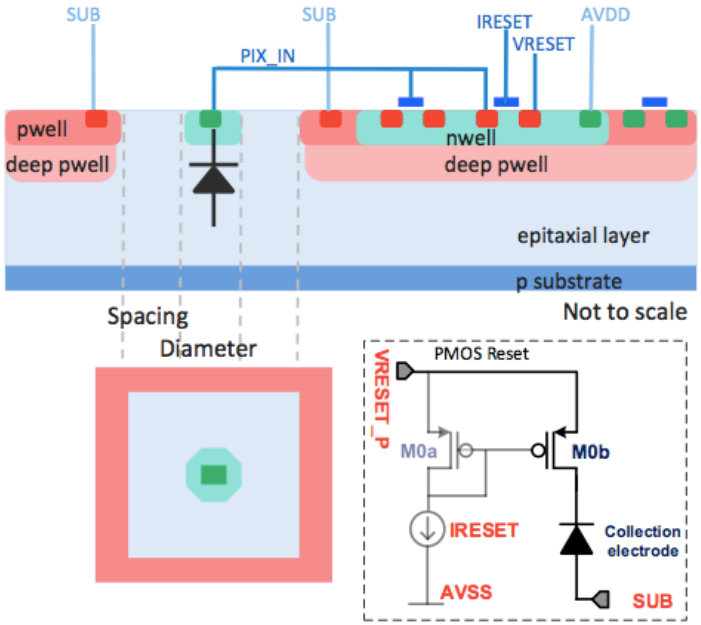
- This is an essential step in the progress of the ATLAS CMOS sensor project for dedicated **DMAPS designs** for the ATLAS ITK outer layers

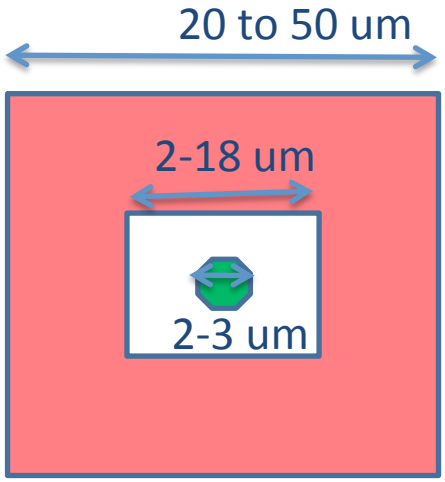
# Backup

# MALTA design consideration

- The key development goal for the ATLAS MALTA chip to **exploit the full advantages of depleted CMOS sensors**:
  - Radiation hardness $10^{15}$ $n_{eq}/cm^2$ / 80MRad and beyond
  - Capable of very high hit rate in the pixel matrix ~ O(1GHz/$cm^2$)
  - Low power in matrix : <<1$\mu$A/pixel with full 25ns in-time efficiency
  - Target high granularity with small pixels for optimal spatial resolution (<< 50x50$\mu m^2$)
  - Optimize materials to achieve really low X/X0 (<< 1%) with industrial packaging techniques

# TowerJazz 180nm Investigator




- **Pixel dimensions for these measurements:**
- 20x20 to 50x50um pixel size
- **3 um diameter electrodes** 25um EPI layer

Designed as part of the ALPIDE development for the ALICE ITS upgrade

**Emphasis on small electrodes and small capacitance enables low analog power designs** (and material reduction in consequence)

C. Gao et al., NIM A (2016) 831
http://www.sciencedirect.com/science/article/pii/S0168900216300985

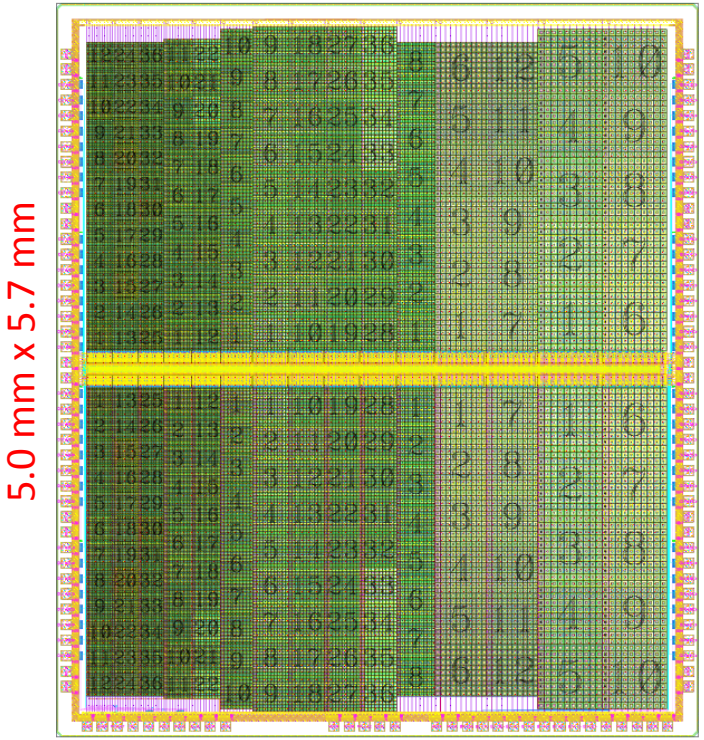
**Produced in TowerJazz 180nm on 25-30um thick epi layer**

Design: C. Gao, P. Yang, C. Marin Tobon, J. Rousset, T. Kugathasan and W. Snoeys

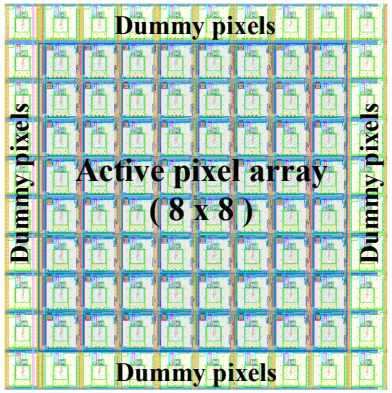
# The TowerJazz Investigator chip

- Developed by ALICE as test chip for the ITS upgrade development
- 134 pixel sub-matrices of different designs (electrode size, PWELL spacing)
- Each sub-matrix contains 8x8 pixels surrounded by dummies
- Possibility of simultaneously measuring the analog signals on 64 pixels

Investigator-1 layout

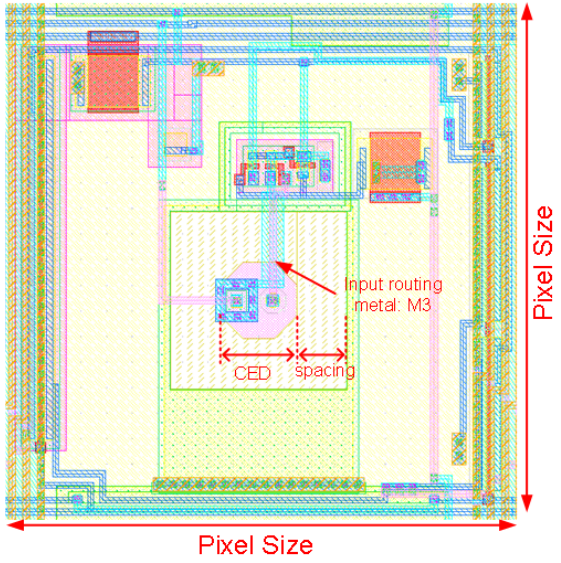



Mini-matrix



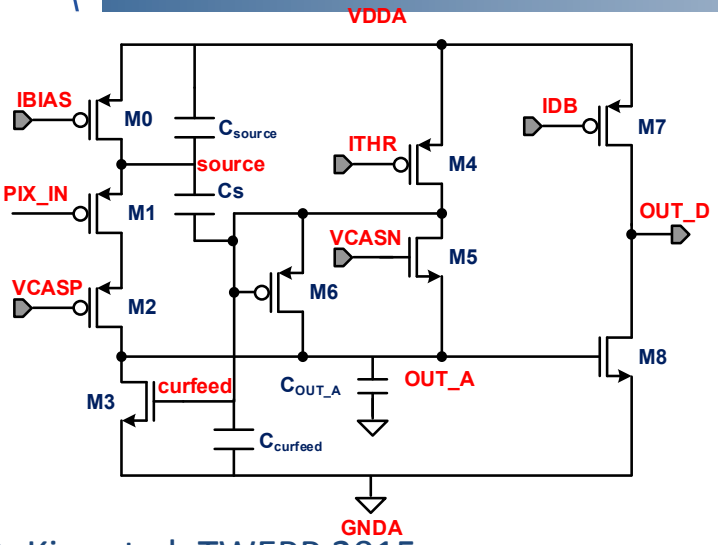

| Mini-Matrix number | Pixel size |
|---|---|
| 0 – 35 | **20 by 20 um²** |
| 36 – 57 | **22 by 22 um²** |
| 58 – 67 | **25 by 25 um²** |
| 68 – 103 | **28 by 28 um²** |
| 104 – 111 | **30 by 30 um²** |
| 112 – 123 | **40 by 40 um²** |
| 124 – 133 | **50 by 50 um²** |

Pixel layout



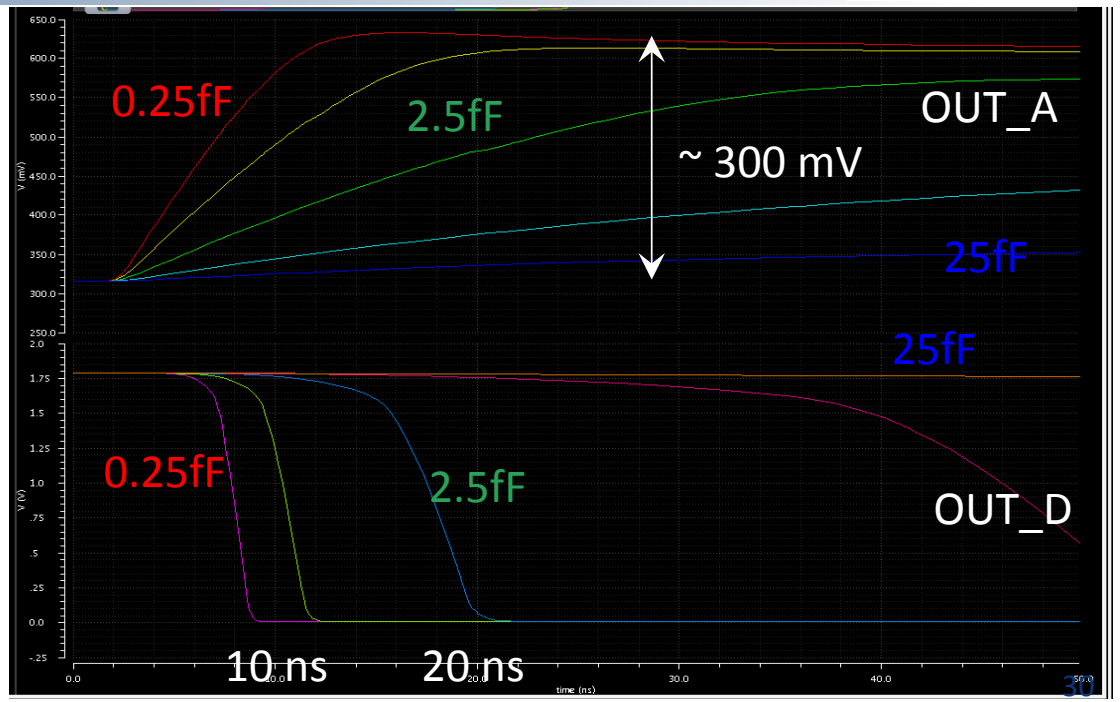

C. Gao et al.
DOI 10.1016/j.nima.2016.03.074

# Smaller capacitance => better Q/C




D. Kim et al. TWEPP 2015

T. Kugathasan, W. Snoeys / CERN




- Reducing the detector capacitance **increases the signal amplitude at the input (Q/C) and therefore yields better S/N and faster signal**
- Can be used to **reduce power consumption** (and therefore services and cooling material).
- Simulated a very similar front end increasing power consumption ~ To match ATLAS ITK requirements we use up to 500nA nA (= 70 mW/cm$^2$ for 36 µm pitch) aiming at timewalk of less than 15ns

# Design of large-scale demonstrators

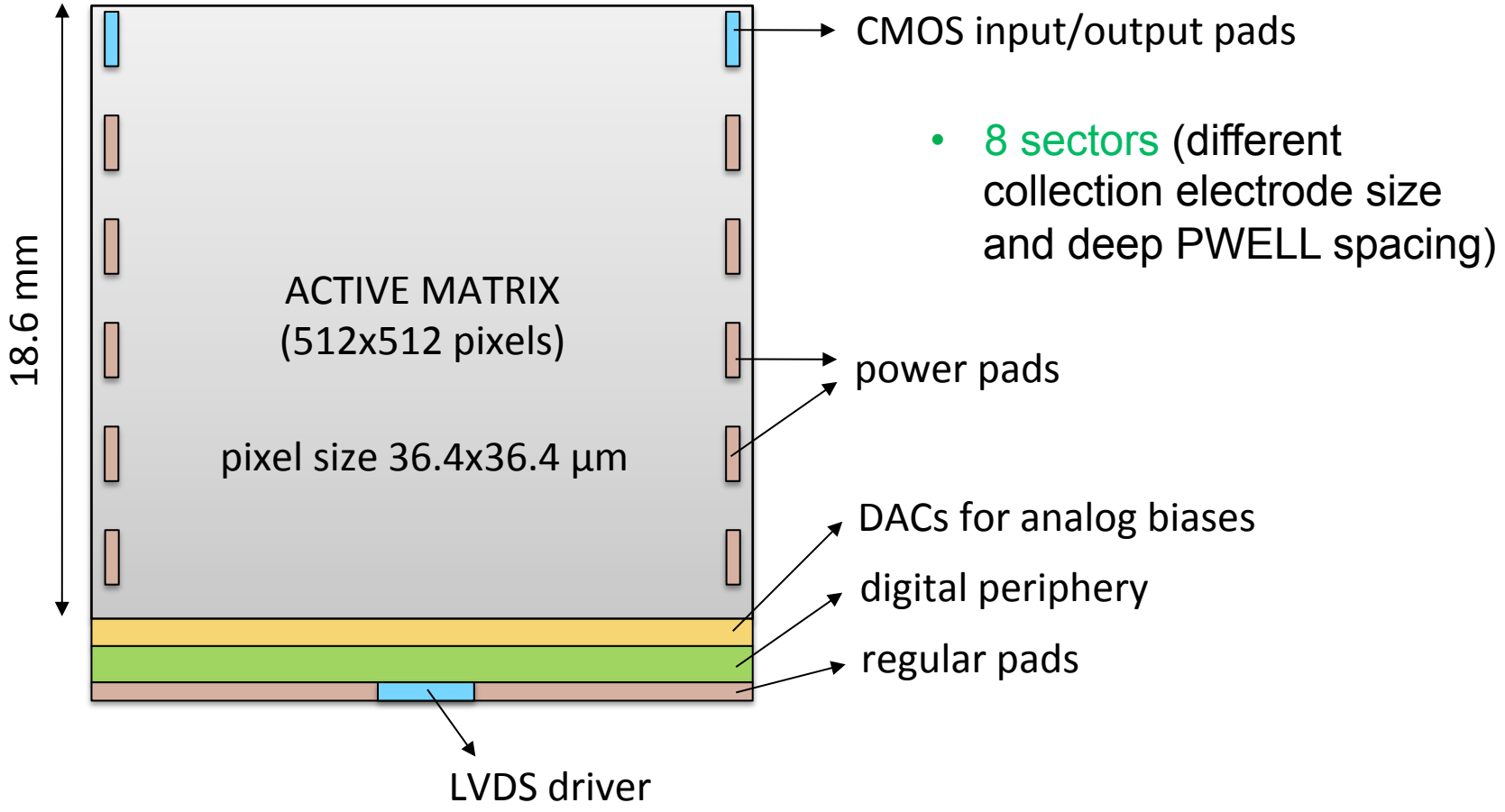
- Measurement results show improved **radiation hardness** for sensors manufactured using the modified process with **small capacitance**

Design of two full-scale demonstrators to match ATLAS specifications for outer pixel layers

- **The "MALTA" chip**
  - Analog front-end based on a previous design for the ALICE experiment
  - Novel asynchronous readout architecture to reduce digital power consumption and increase hit rate capability in the matrix
- **The "TJ-Monopix" chip**
  - Front-end similar to the "MALTA" chip
  - Uses the well-established column drain readout architecture (experience from LF-Monopix design Talk by T. Hirono)

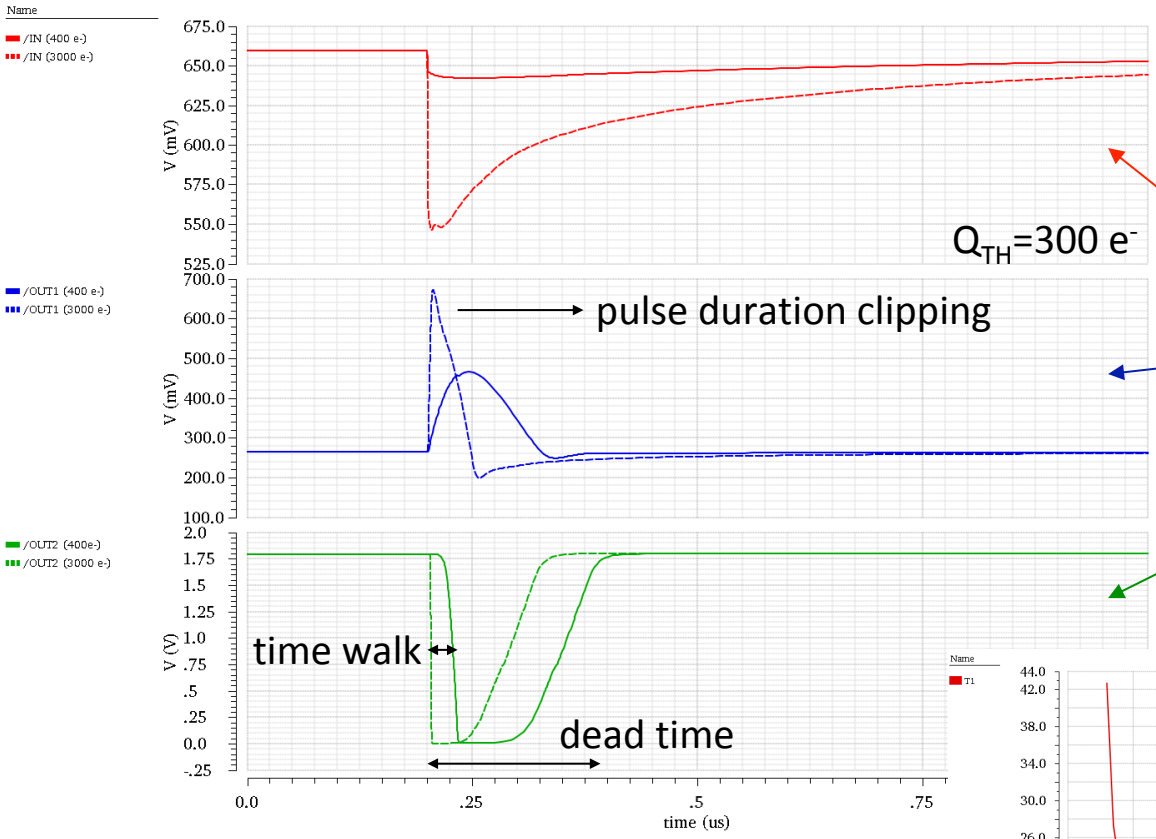
# The “MALTA” chip

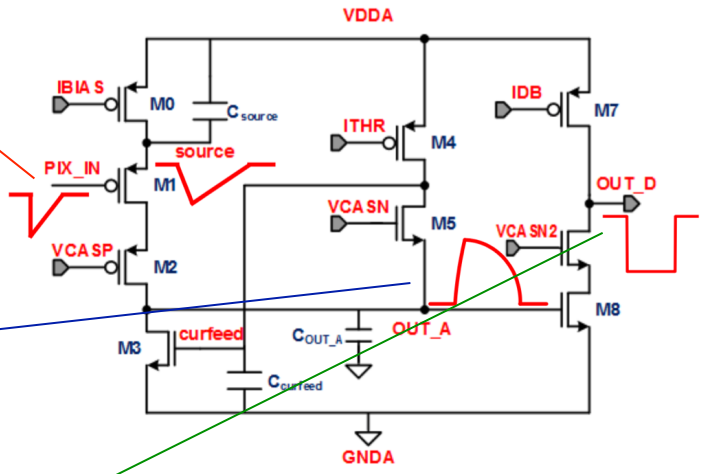
- “MALTA” (Monolithic from ALICE To ATLAS) chip under development at CERN



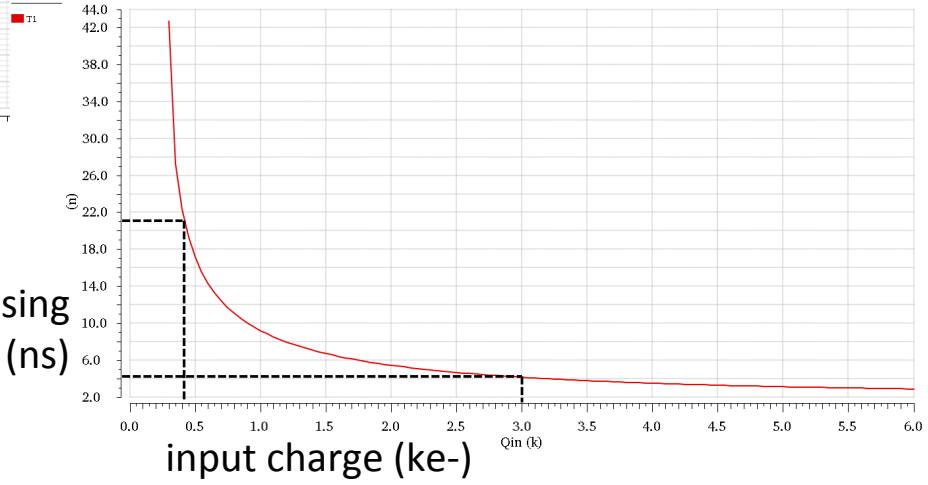

- 8 sectors (different collection electrode size and deep PWELL spacing)

# Front-end timing optimisation




- time-walk curve




delay of rising edge (ns)

input charge (ke-)

- simulated analog signals of the front-end

# MALTA R&D in Post Processing

P. Riedler, R. Cardella / EP-DT

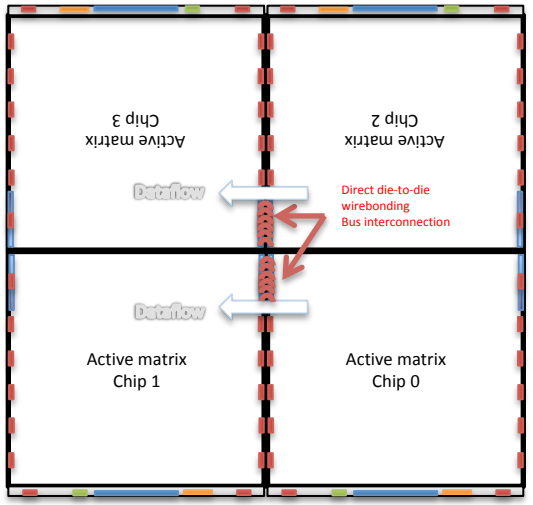
**CMOS sensor post-processing is key for integrated multi-sensor modules**

- High interconnection reliability using new industrial developments
- High throughput and assembly out-sourcing

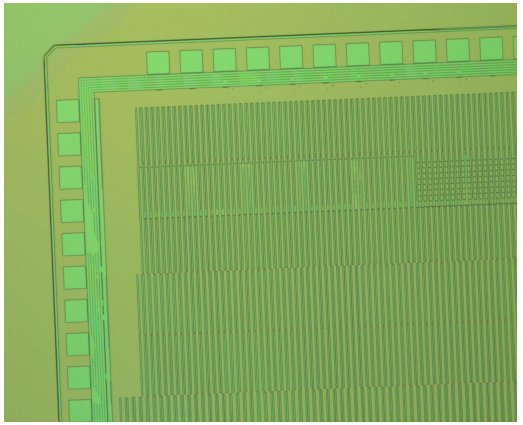
**In 2017 submission in modified 0.18 um TowerJazz CMOS imaging process including:**

- Design of dedicated test structures to study interconnection techniques and module assembly (chip-to-chip transfer on module level)
- Replace flex routing and wire bonding with On-silicon redistribution-layers (RDL) and direct solder bumping

**Delivery of first pad wafers this week**

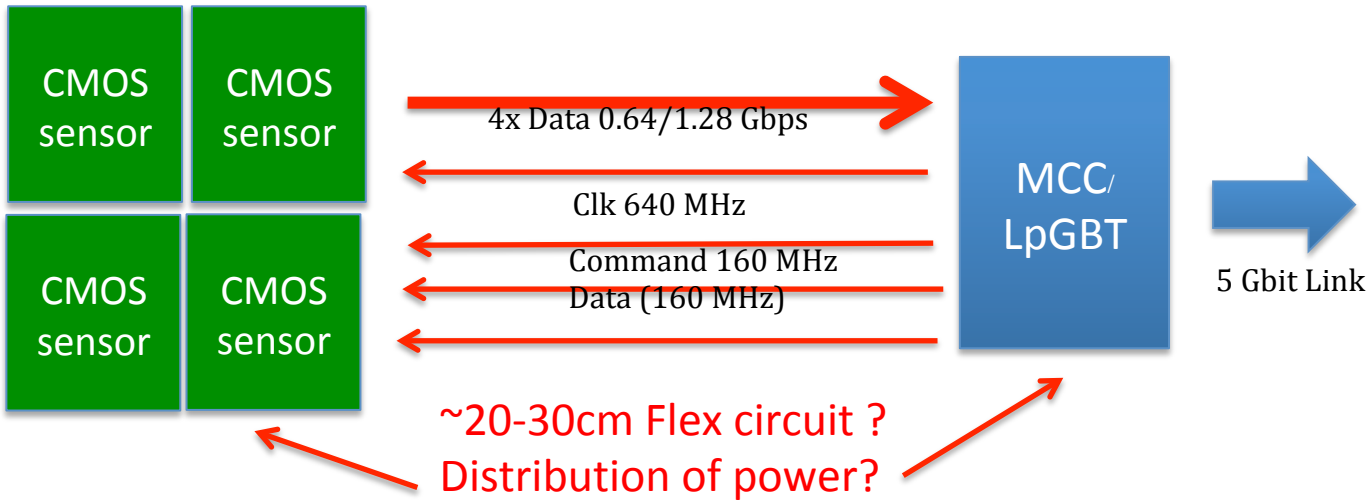



Quad module with chip-to-chip connections



MALTA Pad wafer for assembly tests

# Update on Readout integration




- Benefit from Development of RD53 and lpGBT chip developments in TSMC 65nm
- Use framework of lpGBT to “aggregate” data of 4 CMOS chips in one 5Gbps output line
- BUT: Comsider that Aggregator is NOT on module anymore but now located on “Active Cable” (about 20cm away)
- Important implications for chip and system design!