Performance of the CMS Phase 1 Pixel Detector

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HSTD11 – Okinawa, Japan

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CMS Phase 1 Pixel Upgrade

- Evolutionary upgrade with minimal disruption of data taking
- Detector unchanged: pixel size, sensor, readout architecture
- Performance improvements
- Higher rate capability of readout chips (ROC) and data transmission
- More robust tracking 3→4 pixel hits
- Optimized material budget
- Installed during 2016/2017 extended year-end technical stop

Barrel Pixel
- 3→4 barrel layers
- 48M→79M channels

Forward Pixel
- 2→3 forward disks
- 18M→44M channels

New beam pipe: R = 30→22.5 mm
CMS Phase 1 Pixel Upgrade

- No bandwidth limitation and reduced dynamic inefficiency up to PU\(\sim 110\): Designed for \(L \sim 2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}\) with 50ns bunch spacing
- Fully functional up to LS3
  - Possible to replace Layer1 if necessary
- New ROCs
  - Faster digital readout scheme
  - Higher hit rate capability
  - Lower thresholds
- New DAQ system
- Reduced material:
  - CO2 cooling
  - Light mechanics
  - Material moved outside tracking acceptance

Forward Pixel
3 layers on each end

Barrel Pixel
4 layers

BPix
Supply Tube

FPIX
Service Cylinder

Cooling

DCDC converters

optical links
CMS Phase 1 Pixel Module

- 285μm n⁺-in-n sensors
- 100μm x 150μm pixel size
- All modules in detector have the same size
  - 2x8 readout chips with 4160 pixels
- Two new readout chips
  - Layer 1: PROC600
  - Layer 2,3,4 & forward disks: PSI46digV2.1
- Improvements:
  - Faster digital readout scheme
  - Higher hit rate capability
  - Lower thresholds
- Data from ROCs merged in single output stream (400 Mbps) in token bit manager ASIC (TBM)
  - 1 single data stream per module in FPIX and BPIX Layer 3,4 (TBM08)
  - 2 single data streams per module in BPIX L2 (TBM09)
  - 4 single data streams per module in BPIX L1 (TBM10)
DC-DC Converters

• The upgrade detector has a factor of 1.9 times more channels, and requires more power than the original detector
• To avoid replacing power supply cables and large voltage drops
  • Adopt powering scheme w/ DC-DC converters
  • Power supplies deliver 10 V to the detector
  • Voltage to 2.5-3.6V (depending on application)
  • Radiation hard DC-DC converters used (CERN FEAST2 chip)
• Starting from early October many DC-DC converters started to malfunction
• Both analog and digital converters affected – but failures do not go in pairs
• Several converters came back and started to function normally
• Performed measurements at CMS during inter-fills and in the labs under different conditions
• Will take the detector out during year-end technical stop (YETS)
  • Study the failed converters
  • Replace the failed converters
Phase 1 Pixel DAQ

Completely new system

- Flex or twisted pair cables
- 12 ch fiber ribbon
- 10Gps
- AMC13 (4+8)
- TCDS (2+2)
- Port Card (B)
- Port Card (A)
- CCU
- X48 Dual Port Card (A)
- 4x DC-DC
- DC-DC
- Half Disk
- Service Cylinder
- Underground Service Cavern Racks - uTCA

- 14 ch
- 12 ch
- (672+1184)
- (28+80)
- (2+2)
- (8+8)
- (x4 link)
- (x4 link)
- (x4 link)
- Clk, L1A TTS
- 10Gps
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Phase 1 Pixel DAQ - FED

- Fully functional FED and FEC firmware delivered at time of DAQ system installation, further development is ongoing!
- FED receives and decodes data coming from the front-end and builds events that are sent to central DAQ of CMS
- FED needs to be able to handle all kinds of exceptions
  - Event Number Error (ENE)
  - Missing ROC information
  - Missing event trailers
  - Overflow
  - Timeouts
  - synchronization loss
  - misinterpreted data
  - missing data
  - very large events

TTS state transitions, simple example:
- READY
- OOS
- BUSY
- Lost synchronization
- Fixing OOS by resync

Back to running

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Detector Construction & Commissioning

For details: Poster ‘Construction and Commissioning of the CMS Phase 1 Pixel Detector’ by Miaoyuan Liu

- Several module production chains
- Single set of qualification criteria
- Results of module calibrations from test stands used as starting point for commissioning after installation
- Module production done in ~1 year

- Detector assemblies
  - BPIX in Switzerland (PSI+Zurich)
  - FPIX in US (Fermilab)
- After transportation to CERN full tests on the surface prior to installation
Installation and Checkout

FPIX

- 108 FEDs, 19 FECs, 12 AMC13s
- 70 power supply modules
- 96 connected pipes
- 272 connected fibers

BPIX

DAQ

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Detector Commissioning - Calibration

Threshold Minimization

- Bpix L1: $\sim 3000\text{e}^-$
- Bpix L2-4: $\sim 1750\text{e}^-$
- Fpix: $\sim 1750\text{e}^-$

Noise Measurement

In agreement w/ results from module testing

1Vcal=50e^{-}
Operational Experience
BPix Layer 1 and 2 Timing

- 12 ns shift between barrel layer 1 and 2 but delay chip shared in single φ sector
- PROC600 faster than PSI46dig
  - Speed up L2 with working point of 98% efficiency, e.g.:
    - Layer 2 100 → 250V gained 1-2 ns
Operational Experience
Single Event Upsets (SEUs)

- Stuck TBMs – TBM stops sending data
  - TBM08: ~0.5-1 per 100pb$^{-1}$
  - Solution: power-cycle
- Communication loss of port cards
  - Solution: Reprogram port card
- Conventional ROC SEUs
  - Solution: Reprogram ROCs
- To reduce dead time:
  - Automatization of power-cycling and reprogramming
Detector tuning during LHC run

Pixel HV bias increase to compensate rad effects:
- BPIX L1 → 350V
- BPIX L3-L4 → 200V
- FPIX → 300V

BPIX L2 HV bias → 250V to improve timing

BPIX L1 HV → 200V

BPIX thresholds:
L1 thresholds reduced by ~15%

BPIX pulse height and gain calibration

FPIX thresholds retuning

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Leakage Current

- The change in slope (~15fb⁻¹) is due to a change in operational temperature from -20°C to -22°C cooling plant set point
- The deviations from the linear behavior are due to thermal fluctuations
Alignment: Results

For details: Poster ‘Alignment of the upgraded CMS pixel detector’ by Matthias Schroeder

- FPIX and BPIX L2-L4 close to asymptotic accuracy, BPIX L1 still to be improved
- Final (Pixel + Strip Tracker) alignment eliminates φ-dependency of Z-mass
Performance: Cluster Occupancy

As of early October

Fully functioning channels, based on cluster occupancy ~ 95.7%

- Problem in readout group
- Problem in power group L2/3
Performance: Pixel Hit Efficiency

- Dynamic inefficiency is **much** smaller than in the original detector

Mind the x scale!!

2016
Original detector

August 2017
Performance: Pixel Hit Resolution

**FPIX D2**

- \( \sigma = 8.3 \, \mu m \)
- RMS = 21.3 \( \mu m \)

**BPIX L1**

- \( \sigma = 33.9 \, \mu m \)
- RMS = 41.3 \( \mu m \)

**BPIX L2**

- \( \sigma = 22.3 \, \mu m \)
- RMS = 31.7 \( \mu m \)

**BPIX L3**

- \( \sigma = 12.3 \, \mu m \)
- RMS = 20.1 \( \mu m \)
Summary

- New Pixel Detector installed in EYETS 2016/2017
- Evolutionary upgrade of front-end and software and complete replacement of DAQ back-end
  - The CMS phase I pixel system took data successfully in 2017
- 2017 pixel commissioning was challenging but performance benefits are visible
- DAQ is performing smoothly
- Detector shows good performance
  - Small residuals
  - Well aligned
  - High hit efficiency in all layers
- Detector will be taken out during YETS
  - DC-DC intervention
Backups
Cooling

• Two-phase CO$_2$ cooling system replaced single phase C$_6$F$_{14}$: a new entry in CMS
• Modules are mounted in carbon fiber plates – thermally connected to the cooling pipes
• Diameter: 1.6mm, Wall thickness: ~0.1mm
• Colling lines and connections
  • pressure tested @ 150 bar
  • leak tests @ 100 bar
  • operating pressure @ -20°C is 20-30 bar
Material Budget

- Light mechanical support
- Smaller coolant mass
- Supply tube has much more components, but shifted away from the interaction point

- Reduced mass, less multiple scattering and nuclear interactions
- Factor of two decrease in photon conversion between 1.1 and 2.6 in pseudo-rapidity w.r.t. original detector

50% fewer photons convert at $|\eta|=1.5$
Leakage Current in Phase-0 Pixel Detector

CMS Preliminary

Leakage Current in Phase-0 Pixel Detector

CMS Barrel Pixel Detector

Mar 2010 - Dec 2016

Layer 1
Layer 2
Layer 3

$\mathcal{L}_{\text{int}}$ (pb$^{-1}$)

Integrated Luminosity (pb$^{-1}$)

CMS Forward Pixel Detector

Mar 2015 - Dec 2016

Disk 1
Disk 2

$\mathcal{L}_{\text{int}}$ (pb$^{-1}$)
DC-DC Converters

- Continue tests to identify the cause of the failures
- It is possible that the issue is in the DCDC converter boards (common to BPIX & FPIX)
- Attempting to reproduce it in the lab as the debugging capability on the detector is limited
  - In the lab it is observed that DCDC converters can fail by applying a large overvoltage (~17-18V instead of 11-11.4V)
  - Monitoring the output of the power supplies (no anomaly observed) and measure the IV curve of sets of DCDC converters and, indeed, the ones with broken DCDC converters look anomalous
- Decided to extract the detector during YETS to further investigate, fix the broken DCDC converters, replace the fuses to allow lower input voltage operations in 2018, and, possibly fix the underlying problem for good
The whole plan was executed according to the schedule!

- Power and DAQ back end systems installation
- Extraction old detector
- Reworking cooling pipes and readout fibers
- Installation new detector
- Connection checkout

Cooling plant running cold: no problem → CMS can be closed

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Commissioning w/ beam: Timing Adjustment

- BPIX L3-L4 and FPIX time adjustment completed
- 1st attempt BPIX L1-L2 timing
- 2nd attempt BPIX L1-L2 timing
- Final BPIX L1-L2 timing

- Data collected with the first and the second timing setting are OK but the efficiency is lower
Alignment

- Long and intense alignment campaign
  - Preparatory work in 2016 on phase-1-geometry
  - Minimum data needed to align the new detector verified with MC studies: a few days of collisions would be sufficient
- First pixel alignment with cosmic tracks: at module level
- ~10 alignment updates during collisions
  - Often within 24-48 hours since data were collected
  - To be consistent with detector changes and template updates
- Complete alignment end of August
**μTCA Hardware**

DAQ hardware based on micro Telecom Computing Architecture standard
- Adopted in CMS for recent upgrades

FED & FECs:
- Custom μTCA Cards Based on FC7 with
  - Optical mezzanine
  - Firmware for FED (DAQ) & FEC (Control) functions

AMC13xg:
- CMS Custom μTCA Interface distributes
  - LHC Clock
  - Trigger
  - Commands

COTS Crates, MCH Power Modules (12)

Pixel FEDs 80/28 BPIX/FPIX

Pixel FECs 8/8 BPIX/FPIX

TK FECs 2/1 BPIX/FPIX
Phase 1 Pixel DAQ
System Implementation

- 12 μTCA crates in 3 racks to hold all components of the DAQ backend
  - 108 FEDs
  - 18 FECs
  - 2368 optical links
  - + spares
- Separated into 1 rack for FPIX and 2 racks for BPIX
- 1Gb/s Ethernet network access to all cards in one crate through MCH (MicroTCA Carrier Hub)
- Powered by AC/DC converters
  - 2 redundant power modules per crate
- Patch panels for 12-fibre optical cables coming from the detector (MPO connectors)
Phase 1 Pixel DAQ – FECs

- Pixel FEC and Tracker FEC are fully functional but some desirable features are still under development
- **PixFEC development**
  - Move to *Vivado* synthesized fw version
  - Storage of detector configuration on FC7 DDR memory
    - Less time spent in ‘Configuring’
    - First firmware implementation under test
    - Would make way for direct FED/FEC communication
- **TkFEC development**
  - Seldom communication to CCU ring is lost
    - Needs reset
  - Speed up of I²C communication w/ devices might cure problem
- **AMC13 improvements**
  - Optimizations made to settings
  - Deadtime reduction on resyncs and event counter resets
Phase 1 Pixel DAQ

- New readout links: 400 MHz fully digital
  - New de-serializer in the FEDs
- New back end standard: uTCA
  - New back end boards: FEDs, FECs, AMC13
  - New firmware
  - New software interface to hardware (IPBus/uHal)
- System ready for the detector since day 1
- Overall new DAQ led to smooth operations
  - Auto-masking of channels with readout problem has been very effective
    - Much less downtime for CMS
  - Soft Error Recovery procedure improved in several iterations
- Bandwidth limit improved with respect to original detector: ~80 pileup events at 100 kHz
  - Original detector: ~50-60 pileup events
  - It will increase above 110 pileup with the next FED f/w version
- A success due to a very careful planning
  - Wise exploitation of all the opportunities before the detector was completed
    - Pilot system, miniDAQ, FED emulator, bench test setup
Phase 1 Pixel DAQ System Monitoring

- Basic live signs like voltages, currents, temperatures, and network connection of the system are constantly monitored
- New Grafana based monitoring website has been commissioned and was put in production
- Automatic alarms (e-mail) are put in place when thresholds are passed or crates become unreachable
Phase 1 Pixel DAQ - FED Monitor

- Developed as a stand-alone XDAQ application that monitors the status of all Pixel FEDs and collects statistics about **TTS state** transitions and the status of the connected modules
  - Error statistics on modules are collected by each FED and monitored by software
  - Repeated offenders producing too much deadtime by requesting re-syncs or blocking triggers are eventually masked on module level
  - Global deadtime caused by the Pixel detector has been significantly decreased since first operations
Phase 1 Pixel DAQ – FED Throughput

- FED data throughput on 10Gbit/s optical Ethernet links via Slink protocol currently reaches \(~4.5\) Gbit/s
  - Only becomes bottle neck if LHC running conditions change drastically
  - Good until pile-up of \(~80\) at 100 kHz
- Development ongoing to make full use of available link bandwidth by an improved parallel FIFO draining scheme
Phase 1 Pixel DAQ – Software

- Evolutionary upgrade of Pixel Online Software (POS)
- General software architecture kept, underlying hardware access libraries adapted to IPBus communication with FC7 cards
- Fully functional since beginning to operate and calibrate detector
  - Collected operational experience in 2016 w/ Pilot Blade demonstrator and test stands
- Focus of software development
  - Parallelization
    - Software ‘supervisors’ run on crate level, most noticeable during start and stop of run
    - Gain factor 12 by running processes parallel
    - Deadtime reduction at beginning/end of run
  - SEU recovery
    - ‘Misbehaving’ channels need to be reconfigured
    - Software keeps track of number of errors seen and fixed, and reconfigured channels in FED
    - Some channels need a power cycle to recover from SEU
    - Now also automatized in software
Performance: Data Load on DAQ system

- Data load on single optical fiber varies greatly even among channels from the same layer
- Load balancing necessary
  - Implemented on auxiliary electronics
  - Freedom of connecting fiber channels freely on detector back-end
- Uniform data rate achieved across all FEDs in the DAQ system
- Few FEDs have lower data rate since less channels are connected for them