The CBC3 readout ASIC for CMS 2S-modules

K. UCHIDA, G. AUZINGER, J. BORG, G. HALL, M. PESARESI, M. RAYMOND (IMPERIAL COLLEGE LONDON)
S. BELL, M. CHARRIER, L. JONES, P. MURRAY, M. PRYDDERCH, D. BRAGA (STFC RAL)
J. GOLDSMITH, S. SEIF EL NASR (UNIVERSITY OF BRISTOL)
CBC development in phase-2 upgrade
Outer tracker phase-2 upgrade
2S module
CBC (CMS Binary Chip)

CBC3 architecture
CBC3 tests
Plan
CBC development in phase-2 upgrade
Outer tracker phase-2 upgrade

**Concept**

- Better radiation tolerance for 10 years of 7x luminosity
- Larger coverage
- Reduced material
- Higher granularity
- Track trigger – finding tracks with high pT > 2GeV η in < |2.4|

**Current tracker**

- Inner: pixel modules in green,
- Outer: strip modules in blue (double sided with 100 mrad stereo angle)
- in red (single sided)

**Tracker in phase-2**

- Inner: pixel silicon detector in green and yellow
- Outer: Stacked sensor modules for L1 trigger
- Pixel-strip (PS) modules in blue
- Strip-strip (2S) modules in red

Strips are parallel to the magnetic field
Top and bottom neighbor strips are read in a single ASIC.
High pT track candidates are identified and read out every BX.
Each 2S module consists of:
- 2-strip double layers
- Sensor area $2 \times 90\text{cm}^2$
- 16 CBCs, each reading 254 strips (127 from top & 127 bottom sensors)
- 4064 channels in total
- Output primitive trigger data & L1 triggered data

Spacing of the stacked sensors optimized:
- $\Delta r = 1.8 \text{ mm in the barrel,}$
- $\Delta z = 4.0 \text{ mm in the endcap}$

In total:
- 7680 2S modules with $\sim 31\text{M channels}$
CBC (CMS Binary Chip)

APV @ LHC
- 0.25 um CMOS
- analogue, unsparsified readout
- up to ~18 cm ~25 pF
- power ~ 2.7 mW/channel

CBC @ HL-LHC
- 130 nm CMOS
- binary, unsparsified readout
- for short strips, 2.5 - 5 cm < ~10 pF
- power ~ 300 uW/channel (analogue)
- triggering logic

- **Binary readout for the power consumption**
- **unsparsified for the simplicity**

APV
- binary readout

CBC1
- trigger logic

CBC2
- implementation

CBC3
- final specification
CBC3 architecture
CBC3 Architecture

Interface
- DAQ I/O at 320 Mbps inputs: ref. clock & command outputs: 1 triggered & 5 trigger
- AC (DC < 1uA) coupling analogue frontend
- Inter chip connections for hits at the border for trigger logic
- I2C for configuration registers

Analogue Front End
- 254
- Nearest Neighbour Signals (NNS)
- OR 254
- Band gap
- Bias Generator
- Chip ID & BG e-Fuses
- LDO 1.2V
- VDDA 1.0 V
- 12/12/2017
- KIRIKA UCHIDA @ HSTD11 & SOIPX2017

Test Pulse Generator
- DLL
- 40 MHz Recovery
- Fast Control
- 320 MHz Clock
- 320 Mbps Serial Command input
- Configuration Registers
- Slow Control
- I2C (1 MHz)
- Data Packet Assembly & Transmission
- Stub Gathering Logic
- Data Packet Assembly & Transmission
- 512 Deep Pipeline (12.8µs) + 32 Deep Buffer
- Stub Finding & Bend Calculation Logic
- Stub Gathering Logic
- Layer Swap
- Cluster Width Veto
- Hit Detect
- Channel Mask
- Nearest Neighbour Signals (NNS)
- Programmable Phase 40 MHz Domain
- OR 254
- Chip ID & BG e-Fuses
- LDO 1.2V
- VDDA 1.0 V
- 12/12/2017
- KIRIKA UCHIDA @ HSTD11 & SOIPX2017

320 MHz Domain
40 MHz Domain

40 MHz Domain
320 MHz Domain

Stub & Triggered Data on 6 SLVS

Fast Control

40 MHz Recovery

L1 Counter

Data Packet Assembly & Transmission

Stub Gathering Logic

Data Packet Assembly & Transmission

Programmable Phase 40 MHz Domain

OR 254

Chip ID & BG e-Fuses

LDO 1.2V

VDDA 1.0 V
Analogue frontend

Increase in bias FET allows 3x current range to deal with larger detector capacitance

No change in the basic architecture from CBC2. Small adjustments and improvements only.

New preamp cascode bias scheme to eliminate "shadow effect" (50 ns later in case of high occupancy)

Pre & postamp polarity switch options removed dedicated for electron mode (n-on-p)

To address CM noise in case of high occupancy, reduced by half for fast peaking time
decoupling VPLUS in postamp feedback FET biasing scheme (independently generated VPLUS2, not shown here)
current neutral comparator
Hit detect

three modes & HIP(highly ionizing particle) suppression logic are implemented

HIP suppression
In simulation, a pulse with 4 pC charge on a channel has a large impact on 4 neighbours.
2 of those channels have hit for > 1 us.
→ Those signals need to be suppressed for trigger logic.

Hit detect timing
Signal heights from threshold scan after hit detect vs. hit detect timing wrt. test pulse trigger

Hit detect output is binary, but still possible to obtain the signal shape for test pulse

test pulse DLL(δt:1ns; 0-24ns) trigger latency (δt: 25ns)
The peak stays for 1 clock cycle (25ns) at OR mode

12/12/2017
Trigger data path

Logic output was tested in the lab.

- Minor mistakes are found and corrected in the final version.
- No fatal logic bug is found.

Programmable configurations are optimized for the position from MC

2 & 4 strip clusters give 1/2 strip Stub Address

Programmable max. cluster width (up to 4)

Cluster width discrimination

Programmable correlation Window 1/2 strip step up to 7

Correlation and bend

8-bit address 5-bit bend x Max 3 Stubs

Programmable bend lookup table

8-bit address 4-bit bend x Max 3 Stubs

Correlation bit & 5-bit bend
Triggered data frame

Frame length 950 ns

Header contains:

- Buffer overflow
- Latency error detecting inconsistency between the latency setting at I2C register and read/write counter difference.
- Pipeline address from which the data originate
- L1 counter value (reset every orbit)

Total frame length (active data) = 276 bits = 862.5 ns

2 start bits
9 bits pipeline address
9 bits L1 count
254 bits strip readout data

Buffer overflow
Latency error

Triggered data packet format

Triggered data captured on oscilloscope

Data frame with on-chip test pulse for 32 channels (16 x pair of hits next to each other)
### Trigger data

- 3 stub information (36 bits)  
  - 8 bit address & 4 bit bend for each  
- A sync bit for deserialization  
- Flag bit for CBC errors  
- OR254 : hit OR if enabled  
- SoF : stub overflow to indicate more than 3 stubs are found

### Stub data packet format

- **Sync pulse every 25 nsec**:  
  - + stub 3 bend info

### Stub (trigger) data captured by DAQ

- **Stub 1 address** ➔  
- **Stub 2 address** ➔  
- **Stub 3 address** ➔  
- **Stub 1 & 2 bend info** ➔  
- **Sync pulse every 25 nsec + stub 3 bend info** ➔
CBC3 tests
<table>
<thead>
<tr>
<th>Year</th>
<th>Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>2016</td>
<td>Jul. CBC3 submission</td>
</tr>
<tr>
<td></td>
<td>Oct. 1st wafers with wirebond finish arrived</td>
</tr>
<tr>
<td></td>
<td>Nov. 1 wafer diced</td>
</tr>
<tr>
<td>2017</td>
<td>Feb. frontend test, wafer probing</td>
</tr>
<tr>
<td></td>
<td>Ionization test</td>
</tr>
<tr>
<td></td>
<td>SEU test</td>
</tr>
<tr>
<td></td>
<td>Oct. bumped CBC3s arrived</td>
</tr>
<tr>
<td></td>
<td>bump bonded PCB frontend modules and one was tested in a testbeam at CERN.</td>
</tr>
<tr>
<td></td>
<td>Nov. flexible hybrids for 2CBC3 and modules are produced and tested in a testbeam at FNAL</td>
</tr>
<tr>
<td></td>
<td>Another SEU test on a PCB frontend at CERN with Xe beam.</td>
</tr>
</tbody>
</table>

Wire bonded single chip

8 Analogue Inputs

Power & Digital I/O

CBC3

Wafer probing setup

Bump bonded single CBC on a PCB with a single layer sensor

Bump bonded 2 CBCs on a flexible hybrid with double layer sensor
Analogue frontend

VCTH & offset tuning

- Sweep global comparator threshold to generate s-curves
- Tune offsets to compensate for channel-to-channel differences
- After tuning, the pedestal distribution has $\sigma$ of ~50 electrons
Analogue frontend tests with external charge and capacitance

- ~15 ns of peaking time and < 50 ns to go back to the pedestal
- stable pulse shape up to 12 pF,
- noise < 1000 e up to 10 pF.
- ~350 uW / channel

Signal shapes to external charge injection

External capacitance & internal test pulse

Noise measurement with external capacitance
HIP test

HIP suppression
OFF

HIP suppression
ON

hip count:
the allowed max.
consecutive hits

HIP test with external 4pC

4 fC test pulse was added after the external 4pC
The test pulse timing was scanned.

4pC charge injection on ch 4

HIP tails are suppressed and everywhere else is sensitive to normal signals with hip suppression logic.
Radiation tests

Ionization Radiation test with X-ray at CERN
- No change in performance (noise, pedestals, …)
- ~1.3% max. increase in module power consumption @ HL-LHC dose-rate (9 Gy/hr) & temp (-15°)

SEU test with proton @ 62 MeV at Louvain
- Pipeline logic, read/write counter (Whitaker cell)
  upper limit 5.9x10^{-6} sec^{-1} per chip @ HL-LHC
  - This logic can be reset with fast command which takes just 1 BX regularly.
- I2C registers (Whitaker cell)
  1 order reduction from CBC2 (triplicated cell)
  ~ a few of % of CBC with a register bit-flip on global configuration of the chip in a day in a worst condition.
  - Continuous reading and fix on the error detection would be sufficient.
  - SEU sensitive nodes are identified in inverters used for reset/write.
  Plan to improve the nodes with minor change

Comprehensive scans over dose rate & temperature are performed and a model (built up positive charge at Si-SiO_{2} interface effect) is fit to the data to estimate the power consumption increase @ HL-LHC.
Beam tests

CERN beamtest at UA9 experiment in Oct. 2017

- A module with a single HPK n-on-p sensor, 2.0 cm length, 200 um thick, 90 um pitch, on PCB hybrid
- Pion at 180 GeV and Xe at 150 AGeV
  
  Good performance
  ✓ Stable pedestal with noise ~ 800 e over the week,
  ✓ excellent efficiency with > 99.5%
  ✓ expected resolution. ~ 25 um

FNAL beamtest in Nov. – Dec. 2017

- Flexible hybrid module with stacked Infinion n-on-p sensor, 5.0cm length, 300 um thick, 90 um pitch
- Excellent lab performance, with noise ~ 900 e, works well with high occupancy.

CERN beamtest at UA9 experiment in Dec. 2017

- SEU test with Xe at 50 AGeV
  
  We might have more statistics to confirm the sensitive nodes.
  ✓ more than 100 bit flips in I2C registers are observed. (45 at the test in the pion beam)
  → Each bit flip is going to be examined if those are the expected flips or not.
Some highlights from the UA9 beamtest

Late signal (wrong timing. beam particle is asynchronous) efficiency drop starts from the middle of the strips due to the small signals from charge sharing

DLL is used for LHC experiment to adjust to the particles from the collision chip by chip.

Telescope x [mm]  Telescope y [mm]

Hit efficiency
- Event cut: good TDC value
- CBC hits: hit clusters within 200 um from the track

Signal timing and efficiency
- The efficiency drop from the plateau for late signals with respect to CBC trigger timing for 25 ns

Tracks (beam shape)

HIP observation
- HIP events in Xe beam ~ 1.5 us tails in a couple of neighbours

The tails are detected by sending consecutive triggers

HIP like events with long tails were also observed in the pion data ~ 1 in 10⁴

Hit rate log₁₀

Time [us]

strip # from the center of the hits
Plan

CBC 3.1 – bug fix and minor update

- Add invalid Stub rejection function
  (The low pT stubs get invalid a bend code and sent out from CBC3)
- Verilog bug in stub address is corrected.
  (5 addresses are incorrectly assigned.)
- The order of one set of Nearest Neighbour I/O connection was found to be incorrect and this is corrected.
- Add Nearest Neighbour I/O test feature for wafer testing completeness
- Improve Triggered Data Serialiser robustness to Clock 40 DLL phase shifts
- Improve configuration register SEU robustness
backups
Current tracker in CMS consists of silicon detectors.
Inner tracker $r < 20 \text{ cm}$ are made of pixel sensors
Outer tracker $20 \text{ cm} < r < 110 \text{ cm}$ are made of microstrip sensors

Outer tracker
~15,000 modules with 22 different types,
~75,000 frontend chips (APV25)
Analogue readout for up to ~18 cm (~25pF), AC coupled strip sensors
**p_T module**

Modules in outer tracker – finding tracks with high pT > 2GeV η in < 2.4 |

The strips have to be parallel in the z-axis
no stereo module but strip-macro pixel module is introduced.

<table>
<thead>
<tr>
<th></th>
<th>2S module</th>
<th>PS module</th>
</tr>
</thead>
<tbody>
<tr>
<td>~ 2 x 90 cm² active area</td>
<td>~ 2 x 45 cm² active area</td>
<td></td>
</tr>
<tr>
<td>2 x 1016 strips: ~ 5 cm x 90 μm</td>
<td>2 x 960 strips: ~ 2.4 cm x 100 μm</td>
<td></td>
</tr>
<tr>
<td>2 x 1016 strips: ~ 5 cm x 90 μm</td>
<td>32 x 960 macro-pixels: ~ 1.5 mm x 100 μm</td>
<td></td>
</tr>
<tr>
<td>Front-end power ~ 5 W</td>
<td>Front-end power ~ 8 W</td>
<td></td>
</tr>
<tr>
<td>Sensor power (~20°C) ~ 1.0 W</td>
<td>Sensor power (~20°C) ~ 1.4 W</td>
<td></td>
</tr>
</tbody>
</table>

Stacked sensors
Lower and upper channels are connected to a single ASIC
and trigger signals (stubs) are generated by the correlation logic in the ASIC.
L1 trigger

➢ Current
   ▪ Event rate reduction: 40MHz to 100kHz
   ▪ Input: calorimeter and muon trigger every 25 ns
   ▪ Latency: 3.2 us (128 bunch crossing)

➢ Phase-2
   ▪ Event rate reduction: 40MHz to 750kHz
   ▪ Input: calorimeter, muon & track trigger every 25 ns
   ▪ Latency: 12.5 us (500 bunch crossing)
CBC1 (2011)

Features
- IBM 130 nm CMOS
- 50 um pitch wire bonded
- full size chip with binary unsparsified readout
- I2C interface
- powering test features
  - DC-DC converter (2.5 V → 1.2 V)
  - LDO for analogue power
  - bandgap for biases
- For different sensor configurations
  - for short strips, ~2.5 – 5 cm < ~10 pF
  - Designed for DC coupling
  - 128 channels for both sensor polarities, n-in-p & p-in-n
- 20 ns peaking time
- Global comparator threshold with individual channel offsets
- Hit detection logic
  - 40MHz sampling
  - asynchronous hit detect with single clock pulse out
- 256 deep (6.4 us) pipeline + 32 deep buffer for triggered events
- SLVS I/O for control input and serial data output at 40MHz
- Analog test input

Tested performance
- works for both sensor polarities, can be DC coupled (1 uA leakage)
- front end performance close to expectation (noise, gain, …)
- 800 electrons noise @ < 300 uW/channel for 5 pF sensor capacitance
- The performance was also tested in test beam
  - TWEPP 2011 [link](https://indico.cern.ch/event/120853/contributions/1333922/)
  - WIT 2012 [link](https://indico.cern.ch/event/154525/contributions/1395357/)
CBC1 frontend

**preamp**
Resistive feedback absorbs $I_{\text{leak}}$
T network for holes
Rf.Cf implements short 20ns diff. time constant (good for no pile-up)

**postamp**
Provides gain and int. time constant
~ 50 mV / fC
AC coupling removes $I_{\text{leak}}$ DC shift
Individually programmable O/P DC level
Implements channel threshold tuning
8-bits, 0.8 mV / bit, 200 mV range

**comparator**
Global threshold (indiv. tuning at postamp O/P)
Programmable hysteresis
Features (Highlighted in blue are new)
- IBM 130 nm CMOS
- 250um C4 bump-bonding with wire-bond pad for wafer probing
- Full size chip with binary unsparsified readout
- I2C interface
- Powering
  - DC-DC converter (2.5 V → 1.2 V)
  - LDO for analogue power
  - Bandgap for biases
- For different sensor configurations
  - For short strips, ~2.5 – 5 cm < ~10 pF
  - Designed for DC coupling
- **254 channels from 2 sensor layers** for both sensor polarities, n-in-p & p-in-n
- 20 ns peaking time
- **Front-end circuit improvements**
  - Global comparator threshold with individual channel offsets
  - Hit detection logic
    - 40MHz sampling
    - Asynchronous hit detect with single clock pulse out
  - 256 deep (6.4 us) pipeline + 32 deep buffer for triggered events
  - SLVS I/O for control input and serial data output at 40MHz

**CBC2 (2013)**

- Chip testing features
  - Analogue MUX for bias monitoring
  - Internal test pulse, programmable amplitude and delay in 8 groups of ~32 channels each at once
- Digital logics for trigger
  - Channel mask, cluster width discrimination, window cluster offset correction and correlation, stub shift register, trigger output

**Tested performance**
- Power < 500 uW/channel for 5 pF strips
- No performance degradation and reasonable power increase in ionization radiation test.
- Good SEU tolerance of pipeline logic but I2C registers found to be sensitive to SEU and design revised.
- Other tests results are found in
  - HSTD9 2013 [https://indico.cern.ch/event/228876/contributions/1539120/](https://indico.cern.ch/event/228876/contributions/1539120/)
  - TWEPP 2013 [https://indico.cern.ch/event/228972/contributions/1539574/](https://indico.cern.ch/event/228972/contributions/1539574/)
  - TWEPP 2013 [https://indico.cern.ch/event/228972/contributions/1539574/](https://indico.cern.ch/event/228972/contributions/1539574/)
  - WIT 2014 [http://indico.cern.ch/event/293354/contributions/672348/](http://indico.cern.ch/event/293354/contributions/672348/)
  - FEE 2014 [https://indico.cern.ch/event/276611/contributions/622901/](https://indico.cern.ch/event/276611/contributions/622901/)
CBC2 architecture

FE amp    comp.                                                         pipeline    shift reg.

v_{th}    v_{th}    v_{th}    v_{th}

256 deep pipeline + 32 deep buffer

stub shift register

offset correction & correlation

cluster width discrimination

nearest neighbour signals

test pulse

bias gen.

OR254

40 MHz diff. clock

T1 trigger

fast reset

test pulse

I2C refresh

all signals in blue are single-ended - only travel short distance on hybrid

I2C refresh

trig’d data out

stub shift reg. O/P

trigger O/P

I2C O/P

reset

nearest neighbour signals

chan.  mask

4

4

11

11

signal

cluster width discrimination

offset correction & correlation

pipeline

shift reg.
CBC3 – final specification

Inherited features from the previous prototypes
- 130 nm CMOS
- bump pad pitch : 250 um
- wire-bond pad for wafer probe
- binary, unparsified readout
- I2C interface
- powering
- analogue frontend for DC coupling with 254 channels from 2 sensor layers
- 32 deep buffers for triggered events
- trigger logic
- chip testing features, internal test pulse with DLL and pulse size adjustment, analogue MUX for bias monitoring

Summary of new features
- Further improvement on the frontend for only n-on-p
- SEU tolerant design revised
- Hit detection logic extended
- Extended pipeline 512 (12.8 us) for longer L1 latency
- Full trigger data readout
- 320MHz serial I/O
- e-Fuse to set chip-id and bandgap

TWEPP 2017 https://indico.cern.ch/event/608587/contributions/2614077/
Input signals

320MHz external clock

Fast command serial input
- Fast reset
- L1 trigger
- Test pulse trigger
- Orbit reset resets the trigger counter in CBC

7 fast command combination for each bunch crossing (40MHz)

<table>
<thead>
<tr>
<th>Fast Command</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast Reset</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Trigger</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Test Pulse Trigger</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Orbit Reset</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Orbit Reset &amp; Fast Reset</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Orbit Reset &amp; Trigger</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Orbit Reset &amp; Test Pulse Trigger</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Only orbit reset can be sent with another command
Hit detect

Comparator Output
Fixed-Pulse-Width Output
40MHz Sampled Output
Logical OR Output
HIP Suppressed Output

40MHz DLL adjusted clock

Hip Count Value (3 bits)

I2C Reg

3 Bit Counter

40MHz Sampled

Fixed Pulse Width

40MHz DLL

Comparator

Channel Mask

Mux

Mux

Pipeline Select (2 Bits)

To Pipeline

To Stub Logic

I2C Reg

Compare Logic

HIP Enable

HIP Suppression

40MHz DLL adjusted clock

HIP Suppressed after count of 3

40MHz clock period

1 2 3
HIP simulation

4 pC injected at t=100 nsec
2.5 fC injected on all channels at t = 2.6 usec
all channels recovered within ~2 usec
Ionizing radiation test

In CBC2, SRAM in pipeline cell was identified to contribute to the leakage current increase up to below 20 kGy which decays away with time.

The effect is not significant in the HL-LHC environment, but the cells are replaced with PMOS and enclosed NMOS devices.

The increase of leakage current in HL-LHC condition is extrapolated by fit to data in different temperature and the dose rate.
SEU tolerant design and the test

Pipeline logic
- counters for read/write pointers
- the difference of the counters are compared all times with I2C register setting and error is sent with data in case of the inconsistency.
- unchanged – Whitaker cells

I2C registers
- 330 x 8-bit registers (2640 bits in total)
- SEU tolerant design – Whitaker cells

SEU tolerance in I2C registers in CBC2
- Triplicated cells were used.
- Estimated bit-flips at HL-LHC from proton test beam @ 62MeV
  \[0.6\pm0.2\text{ per chip per hour}\]

The triplicated cells were not apart from each other well (2.4 um).

SEU tolerance in I2C registers in CBC3
- Switched to Whitaker cells
  The cell was used in pipeline logic in CBC2 and showed good tolerance to SEU.
- Estimated bit-flips at HL-LHC from proton test beam @ 62MeV
  ✓ One order smaller rate than CBC2,
  ~ a few of % of CBC may have a register bit-flip on global configuration of the chip in a day. → This level of bit-flips could be fixed by automated regular reading and fix in parallel with the data taking.
  ✓ Data indicate the bit-flips on inverters for reset and write nodes attached to the Whitaker cells.
  → Small change in those inverter in the next version of the chip
UA9 beamtest layout