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The CBC3 readout ASIC for CMS 2S-modules

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The CBC3 is the latest version of the CMS Binary Chip ASIC for readout of the outer radial region of the upgraded CMS Tracker at HL-LHC. It will instrument double-layer 2S-modules, consisting of two overlaid silicon microstrip sensors with aligned microstrips. On-chip logic identifies L1 trigger primitives from high transverse-momentum tracks by selecting correlated hits in the two sensors, so-called "stubs".

The CBC3 is a 254 channel binary readout ASIC, designed in 130nm CMOS, with each channel comprising preamplifier, shaper and comparator. The comparator outputs are stored in a 512-deep digital pipeline to accommodate trigger latencies of up to 12.8 μs. The CBC3 pipeline was redesigned to reduce radiation induced leakage effects observed in the previous version (CBC2). The CBC3 will instrument double-layer 2S-modules and includes coincidence logic for identifying potential stubs, along with programmable cluster-width discrimination and programmable geometric-offset correction. The channels are divided equally between top and bottom sensors, allowing the logic to identify coincidences between hit strips on both. The CBC3 design improves on the original stub recognition logic by increasing the resolution to half-strip and providing bend information associated with the stub direction. Additional logic is included to assign an 8-bit address to each identified stub and assemble a data packet containing up to three stub addresses per bunch-crossing, along with their corresponding 4-bit bend information and status flags. This data packet is divided into five bytes and output from the ASIC via five differential SLVS output drivers operating at 320 Mb/s, thus allowing the complete data packet to be sent in one bunch crossing.

The CBC3 retains an I2C compatible slow control interface for programming configuration registers, but adopted a 320 Mb/s serial command interface for fast commands such as the L1 trigger. These commands are now received in the form of a serial 8-bit word via a differential SLVS input. Whereas the CBC2 was able to operate off a single 40 MHz clock, the CBC3 required an additional 320 MHz clock domain for the fast I/O. To simplify module design, the CBC3 derives its 40 MHz clock from a synchronisation pattern contained within the fast command-word data stream. This derived clock can be phase shifted by a programmable Delay-Locked-Loop in order to optimise timing relative to the bunch-crossing.

The CBC3 was delivered in late 2016, and wire-bonded chips have been under test for several months, during which time total ionising dose performance and SEU sensitivity was studied using x-rays and proton beams. Results and performance will be reported. Probe testing of wafers was carried out before they were sent to be processed with bumps, in readiness for mounting on a dual-chip hybrid. Results will be presented from electrical characterization, including x-ray irradiations and SEU results, and the current status of 2S-modules instrumented with CBC3s will be described.

Primary authors: RAYMOND, David Mark (Imperial College (GB)); BRAGA, Davide (RAL/STFC); HALL, Geoff (Imperial College (GB)); AUZINGER, Georg (Imperial College (GB)); GOLDSTEIN, Joel (University of Bristol (GB)); BORG, Johan (Imperial College (GB)); Dr UCHIDA, Kirika (Imperial College London); JONES, Lawrence (Science and Technology Facilities Council); PESARESI, Mark (Imperial College); PRYDDERCH, Mark (STFC Rutherford Appleton Lab); KEY-CHARRIERE, Michelle (RAL); MURRAY, Peter (STFC); Dr SEIF EL NASR, Sarah (University of Bristol (GB)); BELL, Stephen Jean-Marc (STFC - Rutherford Appleton Lab. (GB))

Presenter: Dr UCHIDA, Kirika (Imperial College London)

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