

11th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD11) in conjunction with 2nd Workshop on SOI Pixel Detectors (SOIPIX2017) at OIST, Okinawa, Japan

Contribution ID: 73

Type: ORAL

OVERMOS - CMOS Hi-Res MAPS detectors for HEP applications

Tuesday 12 December 2017 14:00 (20 minutes)

The OVERMOS project investigates the use of MAPS, fabricated using a standard low voltage and high resistivity substrate 180nm CMOS technology, for tracking and vertexing in HEP applications.

Following a description of the main features of the proposed CMOS technology, which should guarantee high charge collection efficiency even after high level of dose of radiation, we will detail the design of the OVERMOS test pixel structures, which include active pixels, with in-pixel RO electronics, and basic pixel arrays. Alongside, 3D TCAD simulation results related to charge collection and DC characteristics of the pixel structures will be shown.

Next, we will present experimental results for the fabricated OVERMOS test structures, including charge collection efficiency obtained using laser injection, and comparison of performances before and after neutron irradiation.

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Session Classification: Session7

Track Classification: Large scale applications