The upgrade of LHCb VELO

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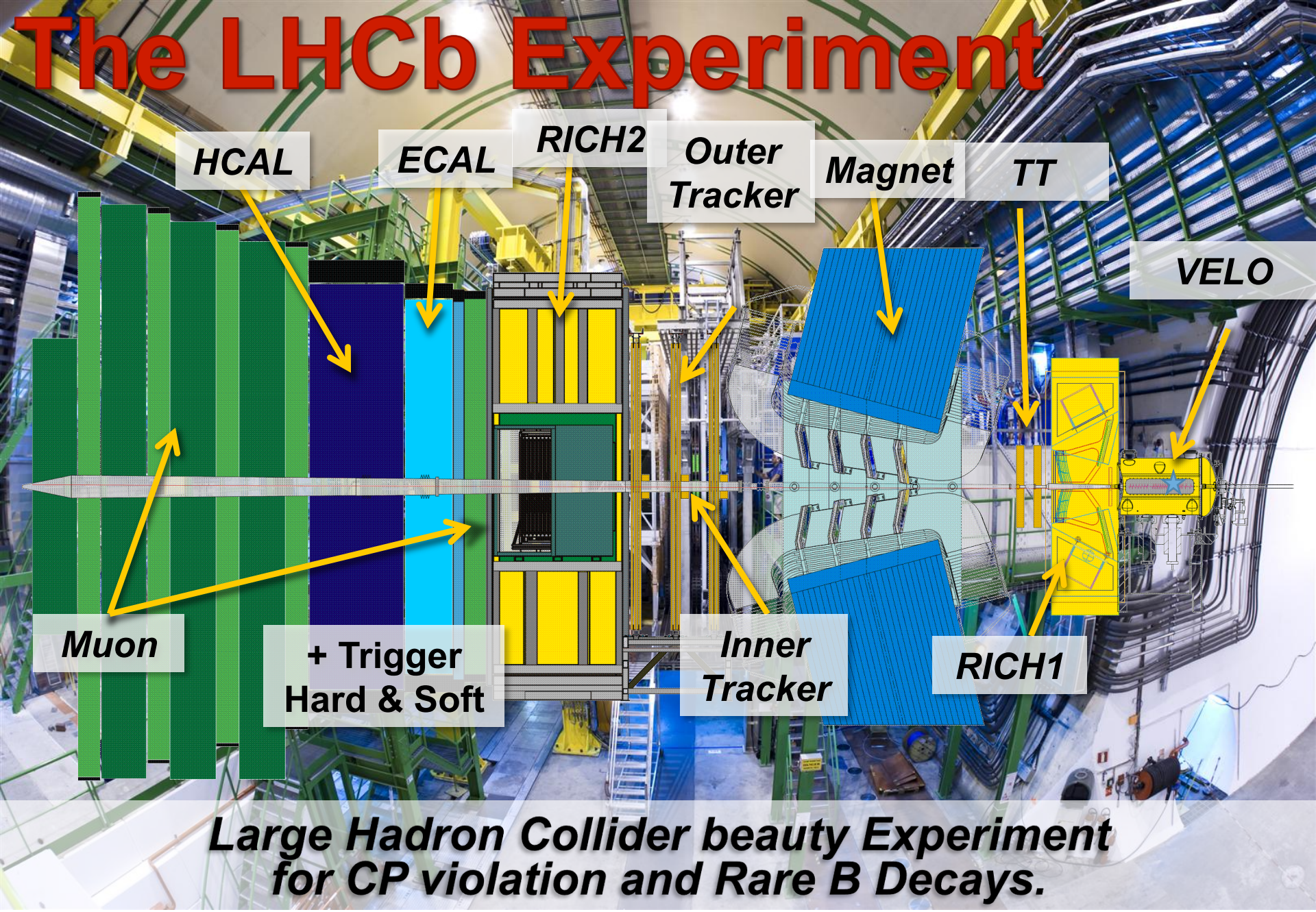
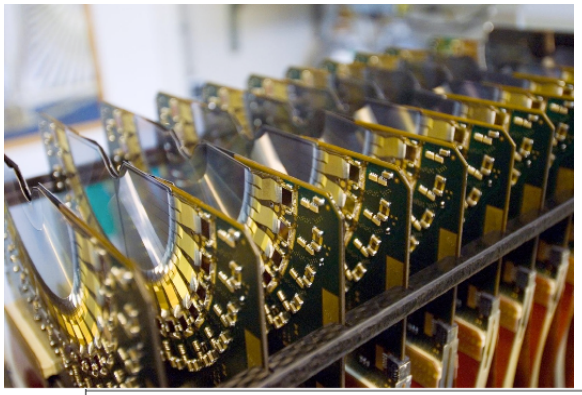
Universidade Federal do Rio de Janeiro

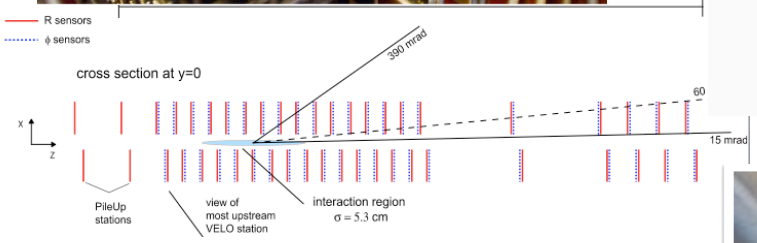
The LHCb Experiment

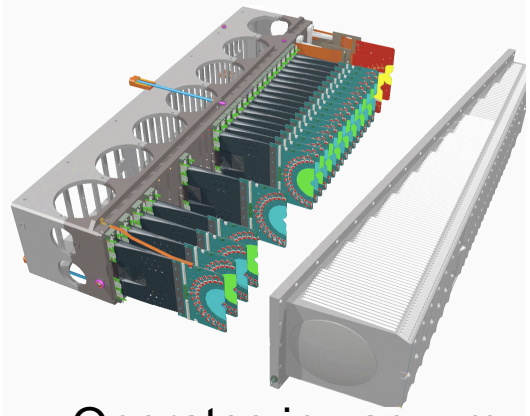


Large Hadron Collider beauty Experiment for CP violation and Rare B Decays.

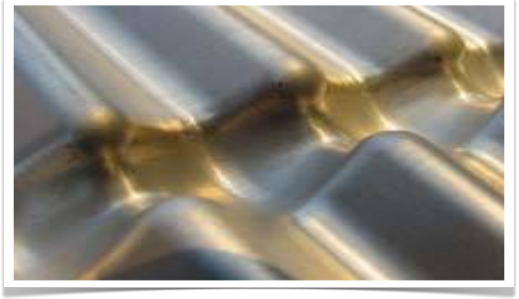
The current Vertex Locator (VELO):







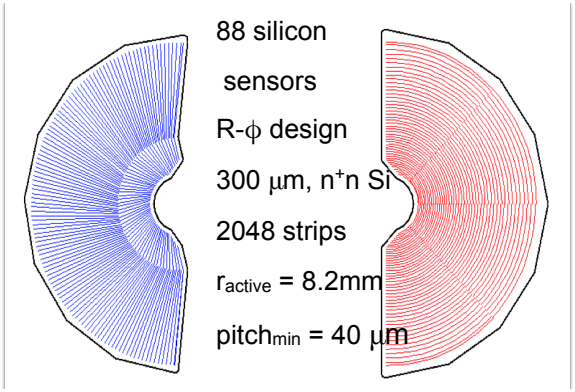
Operates in vacuum



Separated from primary vacuum by thin ***RF foil*** with complex shape
– Protection from beam pickup

biphase cooling

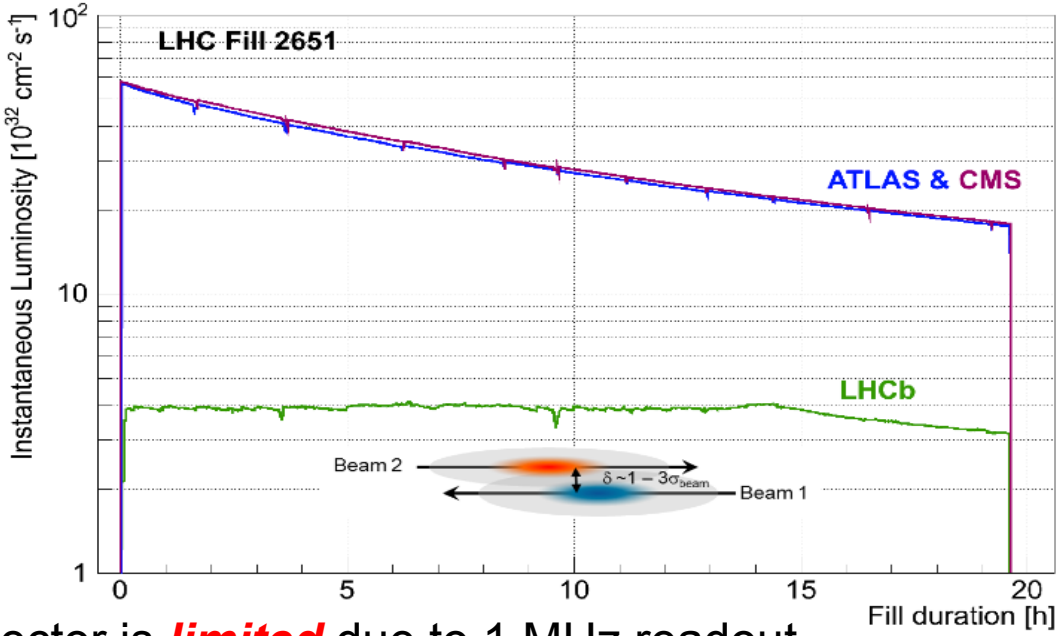
Evaporation of CO_2 keeps the temperature stable.



Moves away every fill and ***centers around the beam*** with self measured vertices

Why upgrade LHCb – Phase 1 (LS2)

- Currently LHCb can cope with a inst. lumi. higher than design
  - LHC still provides more than what we can handle:



  - ***Current*** detector is ***limited*** due to 1 MHz readout.
  - Higher Luminosities do not translate to higher physics: need smart Trigger.
- The upgrade is planned as a major Trigger/Readout upgrade:
  - From 1 to ***40 MHz*** full readout ➔ Every collision read out to a computing farm
  - Higher instantaneous Luminosity ➔ Higher occupancies/***Faster Ageing***
  - Change all the front-end!

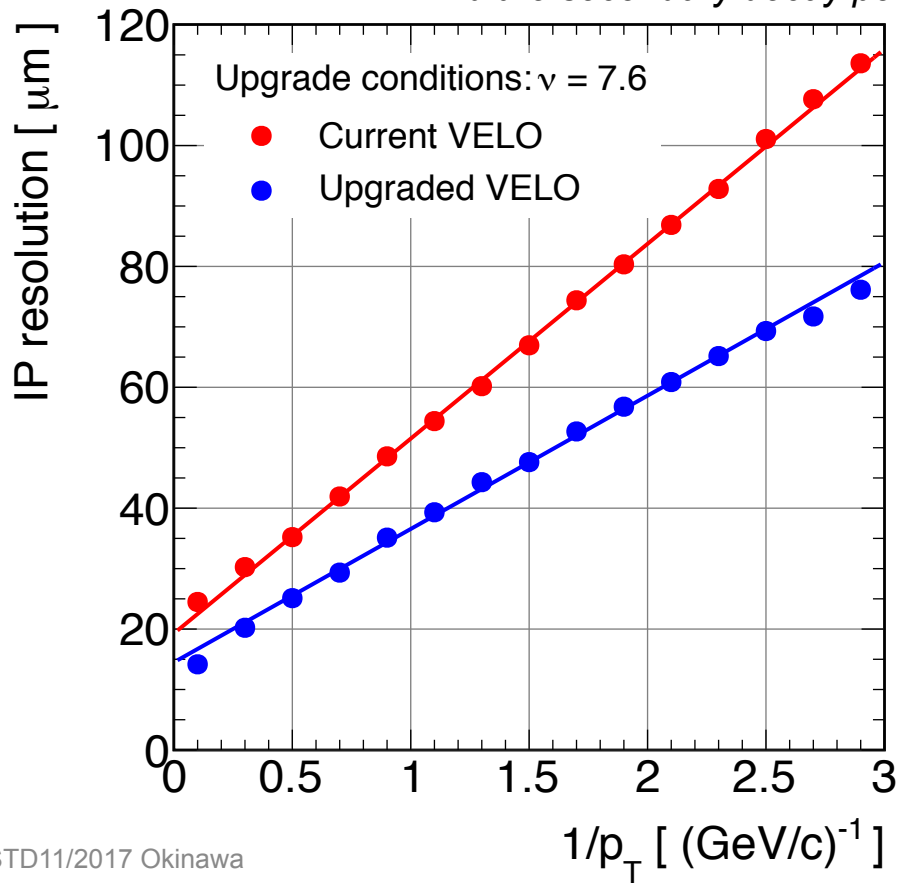
Main challenges for the Velo Upgrade

Non uniform ***Radiation*** exposure	8 x 10^{15} n_{eq}/cm^2 @ tip close to IP, ~0.1 x 10^{15} n_{eq}/cm^2 @ outer edge
Sensor ***HV*** tolerance	1000V after 50 fb^{-1}
Readout data ***rate***	~33tracks/Event/module. (LHC: 40 MHz/25 ns)
Low ***Temperature*** operation	-20 C @ tip close to the beam
ASIC power consumption	3W/ASIC; up to 36 W/module;
Material budget	Good IP and tracking resolution currently: • Proper time resolution ~ 50 fs • IP resolution ~ 40 mm (p_T=1GeV)

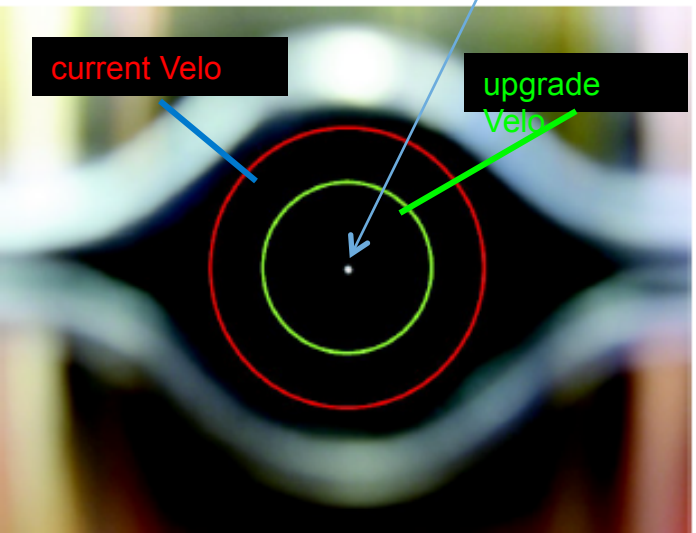
Changes to improve: Closer, lighter, more segmented

- From strips to pixels: ***55x55 μm^2*** pixel.
  - Fast and robust pattern recognition. – better signal to noise
- Cooling interface needs to come closer to the tip.
  - Plan to use ***μ-channels*** etched in silicon.
- First active element at ***5.1 mm from beam*** (was 8.2 mm)
- New RF-foil required.

Impact parameter resolution wrt Collision Point helps to find the secondary decay points

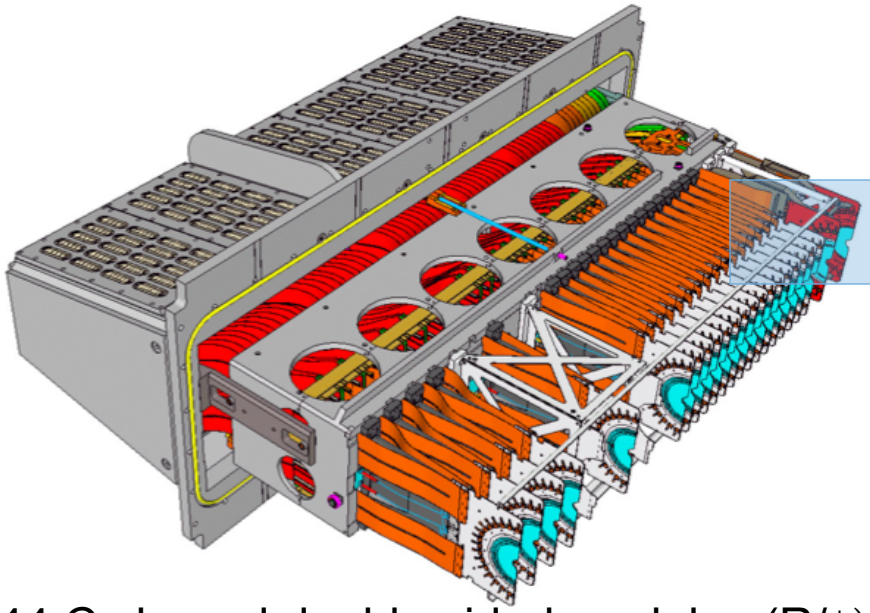


Collision point "proton view"



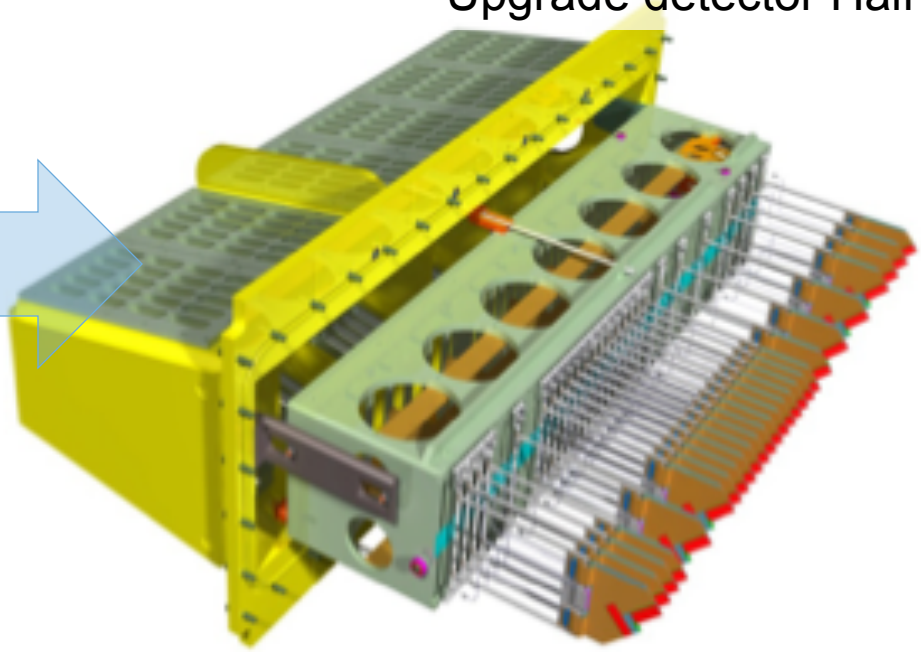
Upgrade Plan

Current detector Half

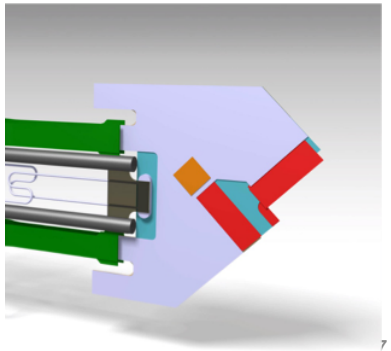


44 C shaped double sided modules (R/ϕ)
➔88 sensors.

Upgrade detector Half

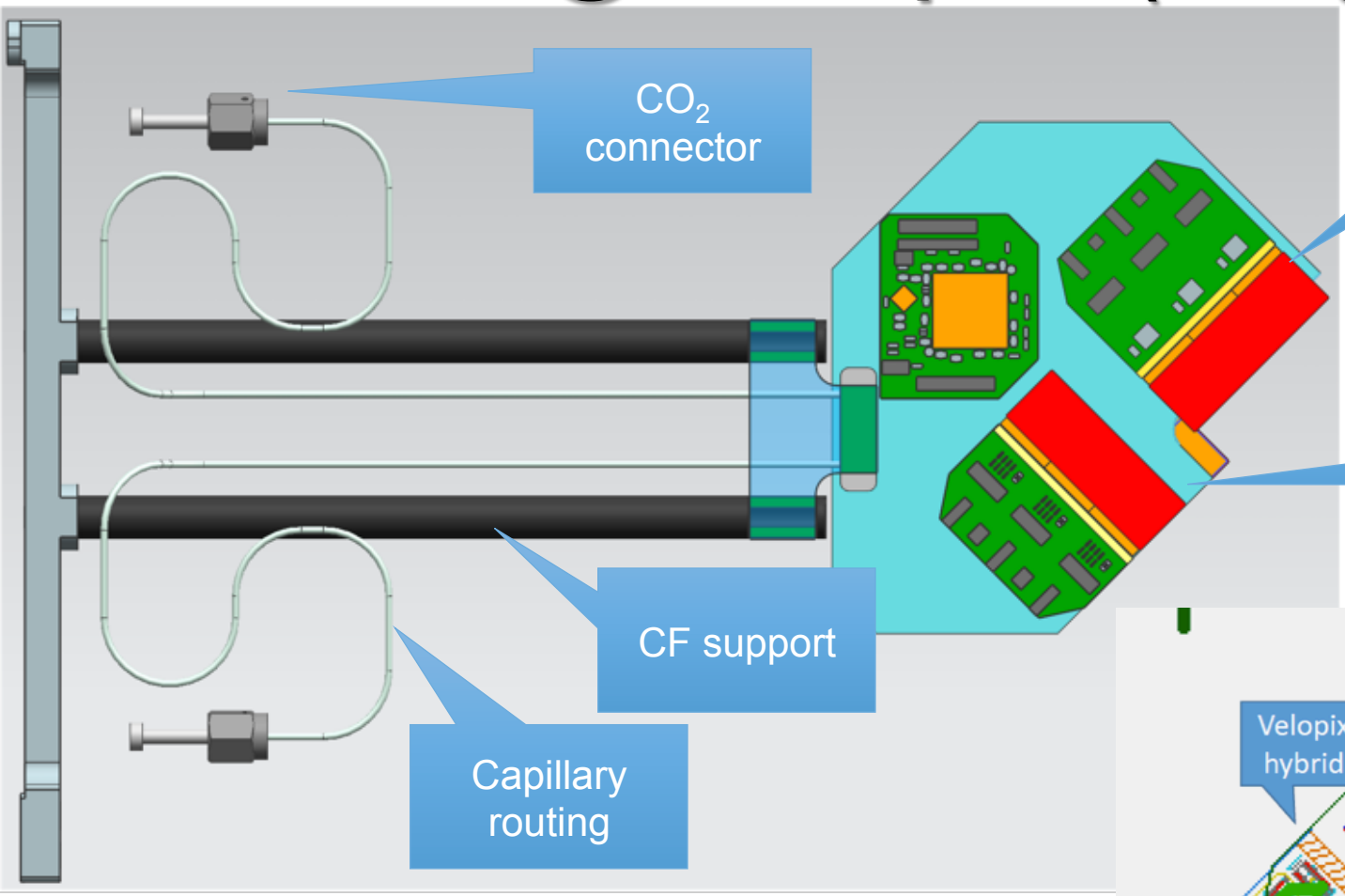


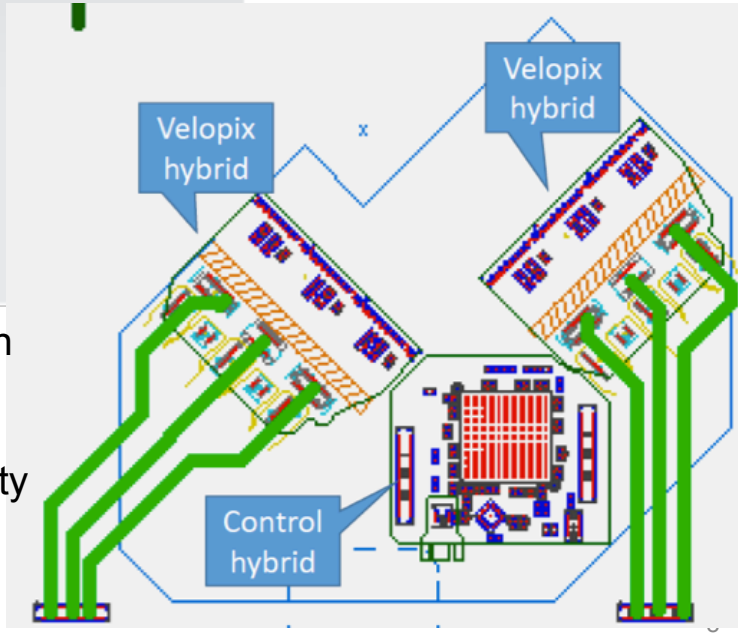
52 L (K) shaped pixel modules
➔208 sensors.



Keep vacuum and motion features.

Modules: 52 @ 25mm pitch (along beam)

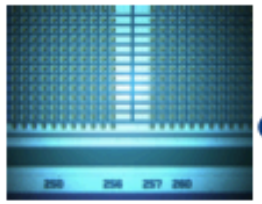




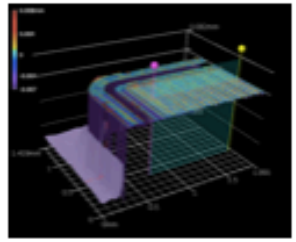
Substrate should provide efficient and stable cooling, withstand high pressures, be radiation hard with low outgassing, and be planar i.e. suitable for gluing and wire bonding
The physics performance requires low mass and mechanical stability

Silicon sensors

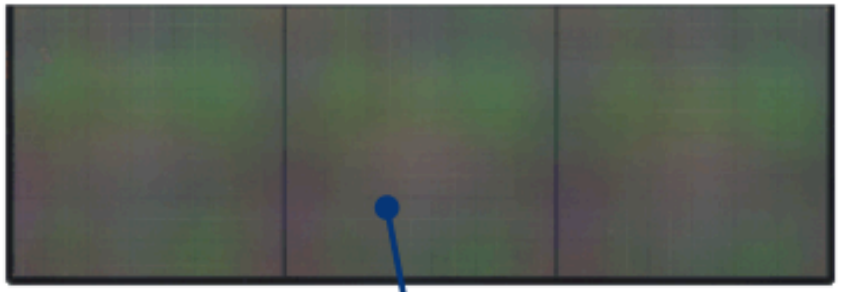
- n-in-p
- Tile for 3 ASIC chips
- 200 μm thick
- 55x55 μm^2 pixels
- Non uniform irradiation (~ r-2.1)
- Tip close to beam: 8 x 10^{15} n_{eq} , far corner only at 0.8 x 10^{14} n_{eq}
- guard ring width ~450 μm
- Bias of 1000V after 50 fb^{-1}

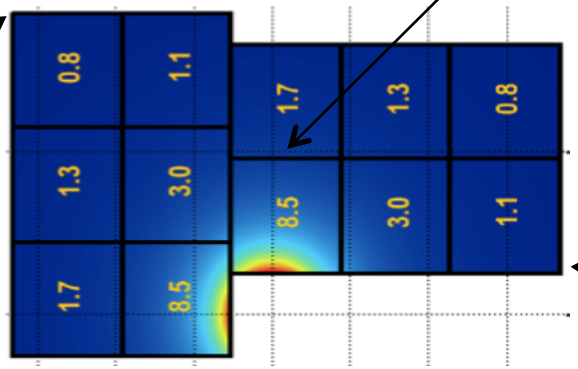


elongated pixels between ASICs



Sensor Thickness 200 μm

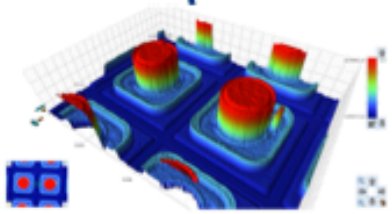




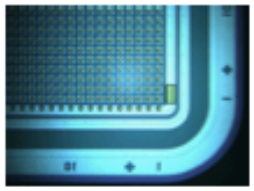
factor 1/7

factor 1/100

factor 1/20



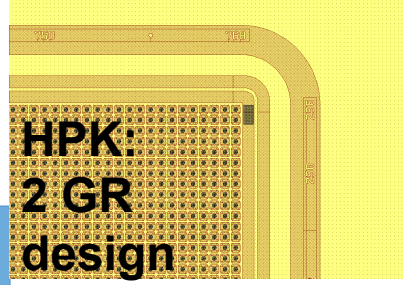
sensor UBM pads

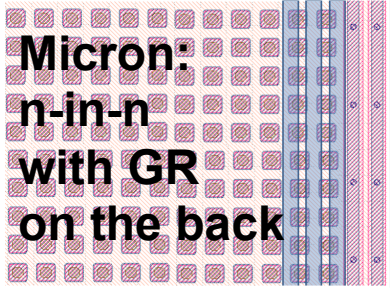


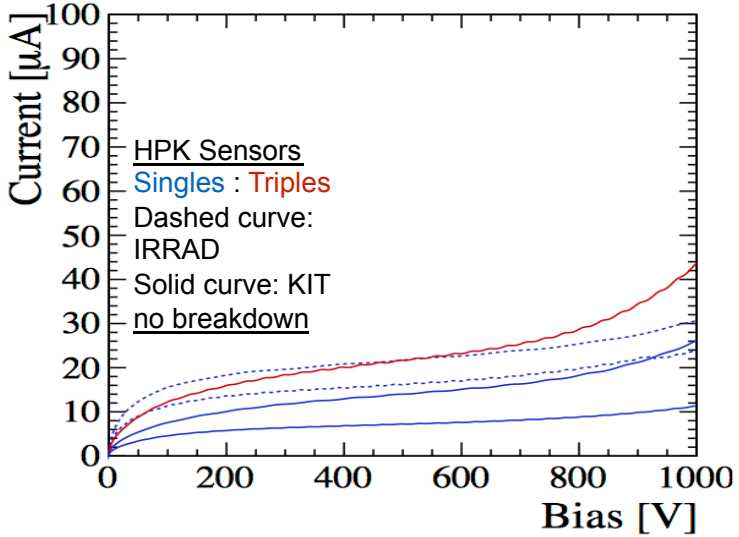
rounded, DRIE etched corners

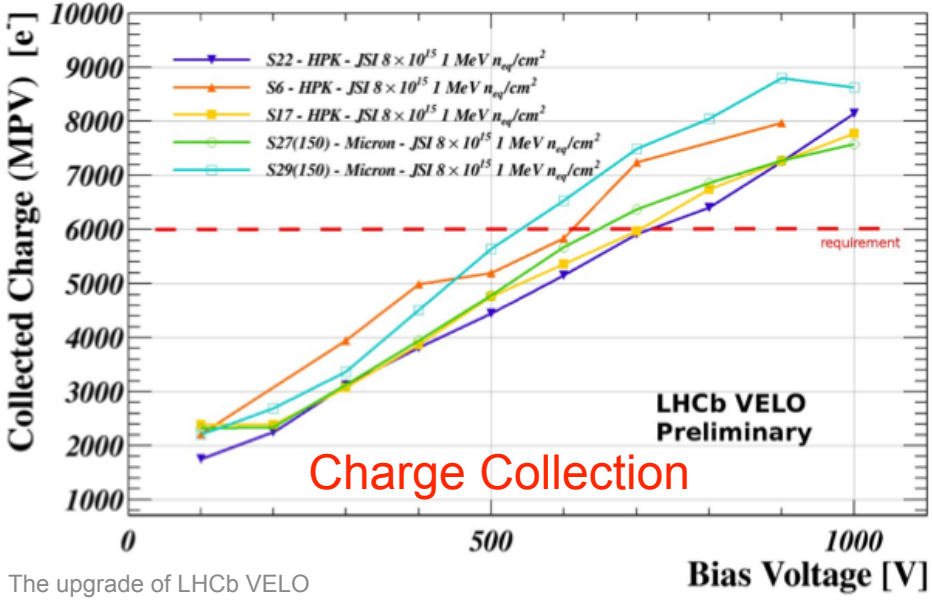
Sensor: Prototyping

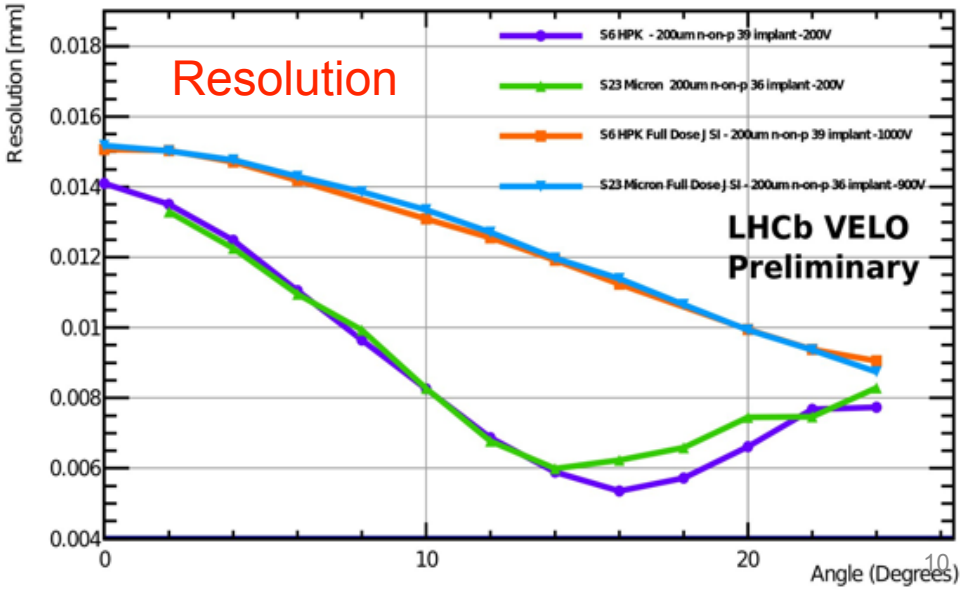
	Micron n-on-n	Micron n-on-p	Hamamatsu n-on-p
Thickness	150 µm	200 µm	200 µm
Implant size	36 µm	36 µm	39 µm 35 µm
Guard ring pixel to edge	450, 250, 150 µm	450, 250, 150 µm	450, 600 µm





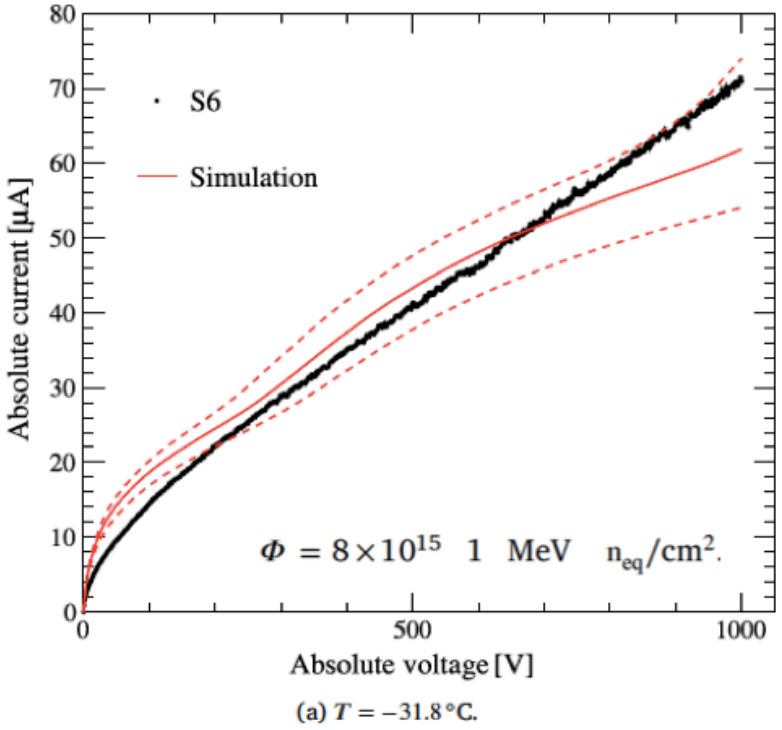


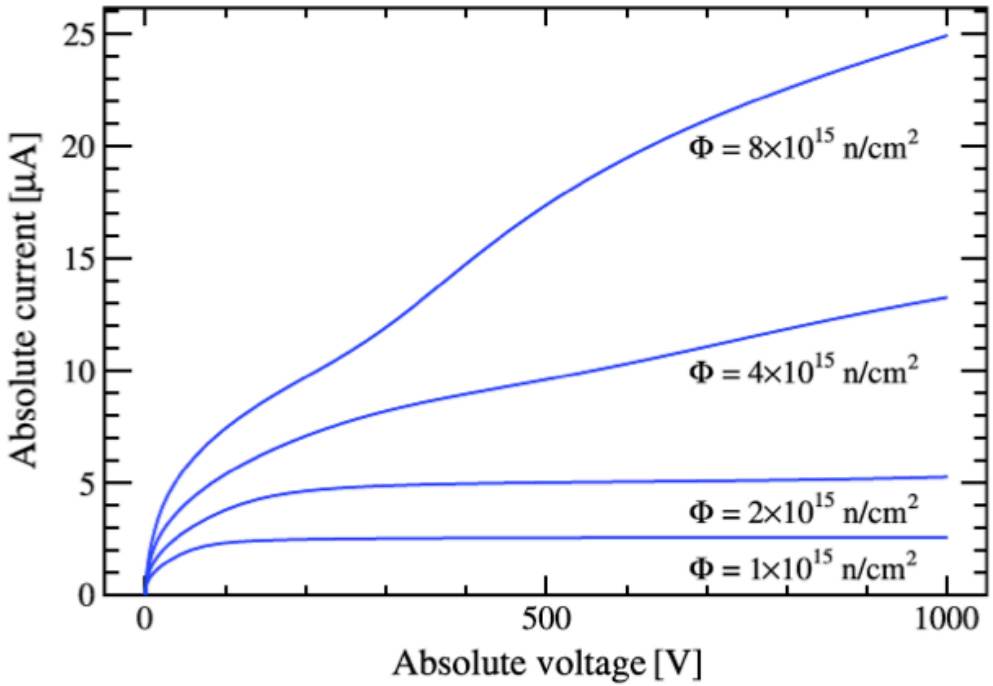




Current model for irradiated sensors

- ***need a model***
  - valid for our irradiation range
  - capable of describing the changing IV curves we see
  - focus on bulk effects
- ***Folkestad-LHCb model:***
  - ***Nucl. Inst. and Meth. A 874 (2017) p94-102***



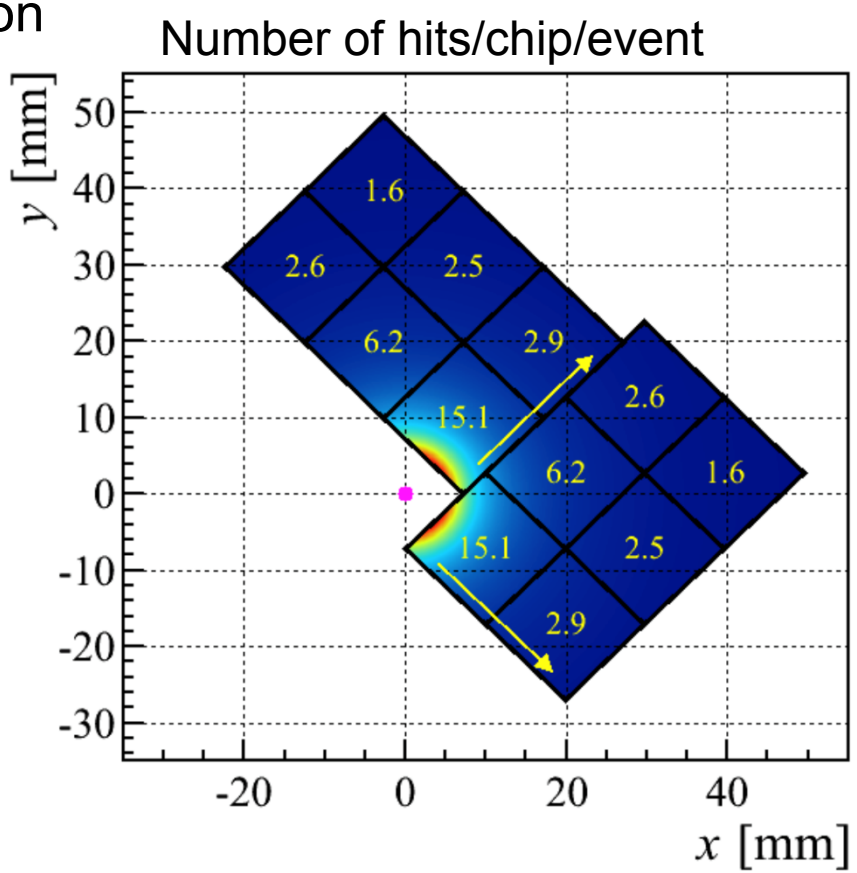


- inspired by Perugia and EVL models
- contains one donor level, one shallow and one deep acceptor
- TCAD simulations show Reasonable agreement with data

Linear Increase in current for heavily Irradiated substrates Due to avalanche

ASIC Challenges

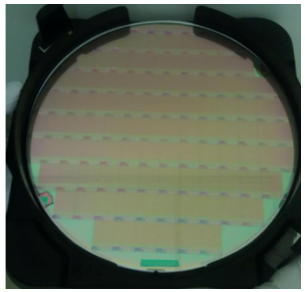
- Average # particles / chip / event
  - average (peak) rate: multiply by 26.8 (40) MHz
- Hottest chip →230 (320) Mtracks/s ~ 600 (900) Mhits/s per chip
  - grouping of pixel hits
    2x4 super pixels→30 % data reduction
- Output bandwidth of (hottest) VeloPix:
  - Average: 13 Gbit/s ; peak: 20 Gbit/s
  - 4 links at ~ 5 Gbit/s
- High radiation enviroment:
  - SEU protection: triple redundancy
  - Extensive tests with heavy Ion irradiation



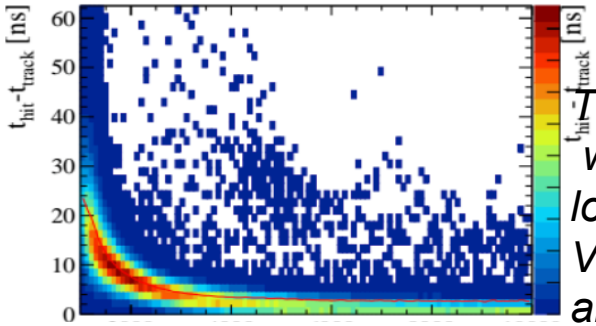
VeloPix ASIC

- Key features
  - Data driven readout:
    Each hit ***time-stamped***,
    sent off chip immediately
  - Fast front-end: ***time walk < 25 ns***
  - Binary readout –
    but optional Amplitude (slow)
    for calibration
  - Technology (130 nm TSMC)

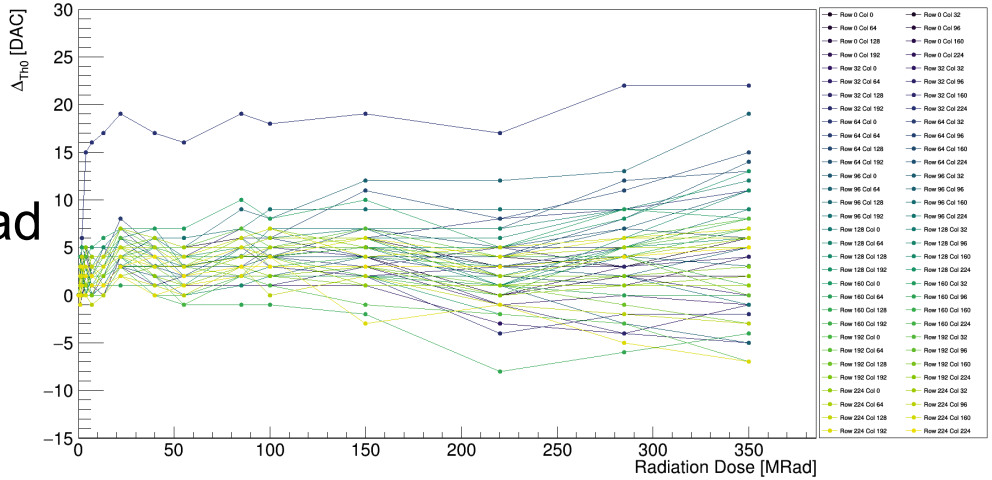
- **Chips will be *thinned* to 200 µm:**
  ➔ minimize material
- Test done with X-ray up to 400 MRad
  - No change in digital
    power consumption
  - No drift in analogue parameters:
  - pixel thresholds,
    noise and global DACs remain stable



VeloPix Wafer: Probe test station ready



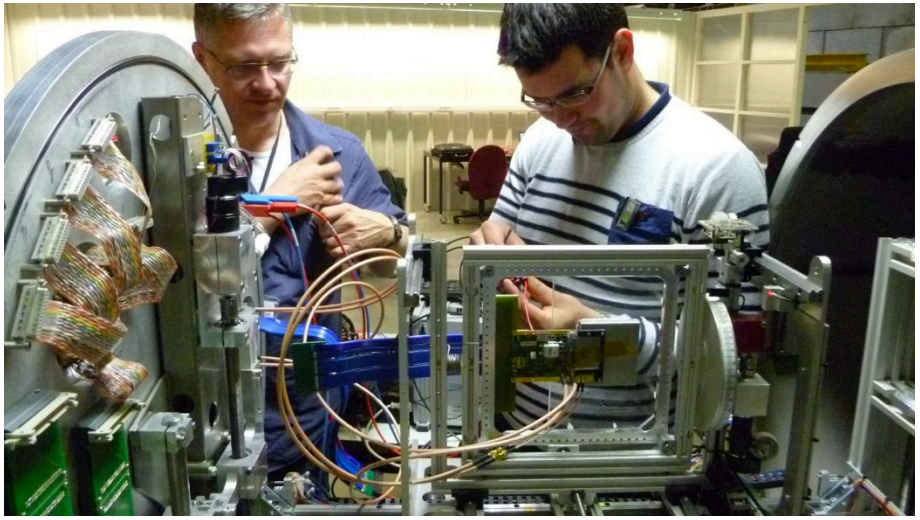
Time walk measured with Timepix3: lower signals are slower. VeloPix has a very simila analog design



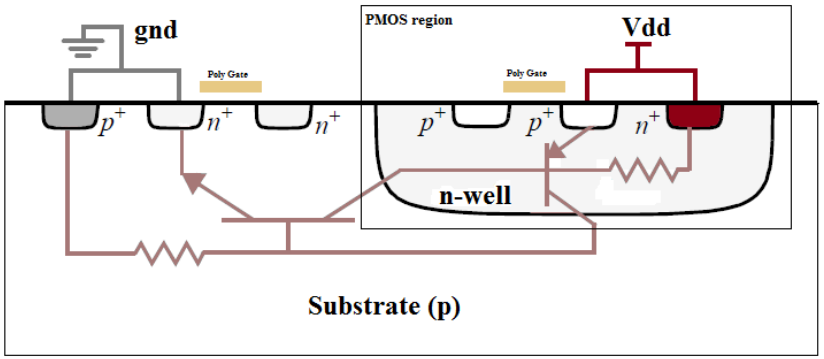
threshold shift w.r.t. 0 Mrad

Single Event Upset Testing

- determine rate of single event upsets (bit-flips)
- Shoot heavy ions of various type / angles
  - Using heavy ion facility in Louvain-la-Neuve



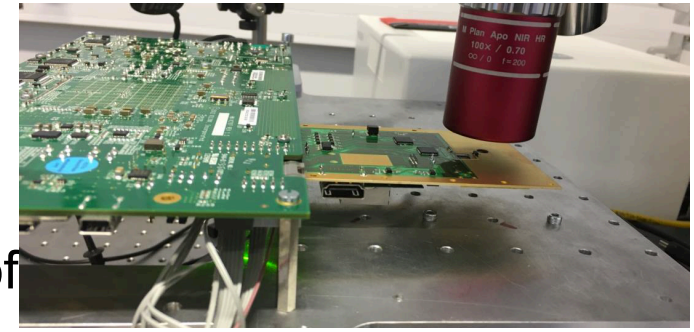
- Found some issues – VeloPix v1:
  - Single Event Latch-up (SEL): a (local) short circuit on the power lines
  - And large x-sec for the reset circuit

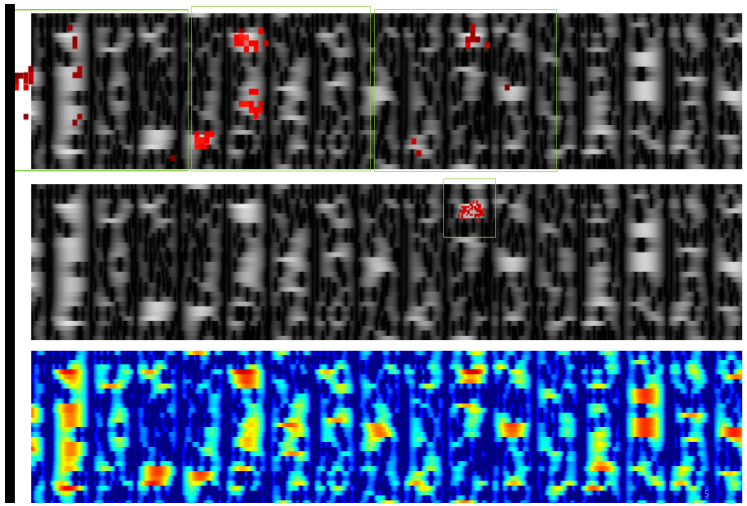


- SEL occurs in the matrix only
- strongly temperature dependent, not observed below -10 °C
  - though might still occur if tested for longer time
- SEL is due to higher substrate/well resistance in TSMC process.
- Solution: add extra substrate contacts to reduce distance to contact

Laser testing

- SEL confirmed by injection of laser light at Montpellier facility
  - very precise position of charge injection
  - but can not scan whole chip, too many steps (1 or 3 µm step size)
- NIR photons shot into chip from back side
- Local charge injection (also in depth) possible by two photon absorption
- VeloPix2 has these change already implemented.

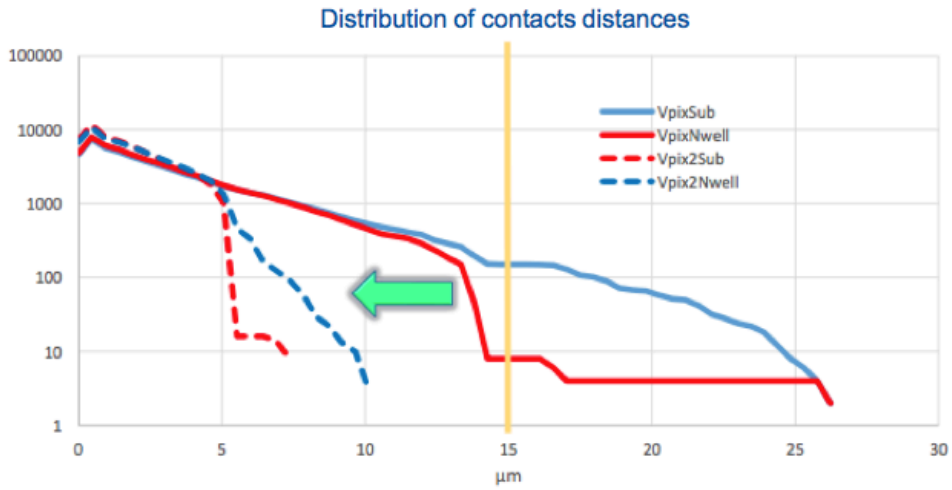




observed SEL 3 um steps

observed SEL 1 um steps

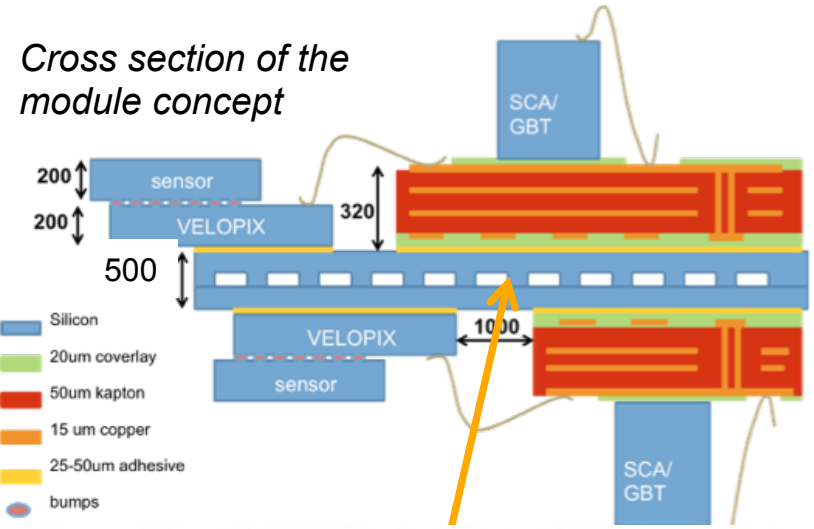
design: distance to contact

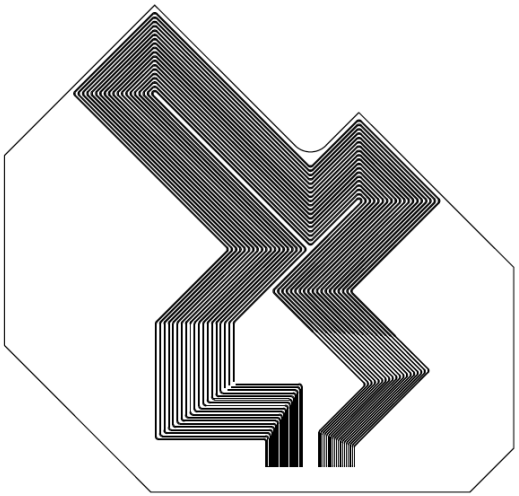


Cooling: micro channel substrate

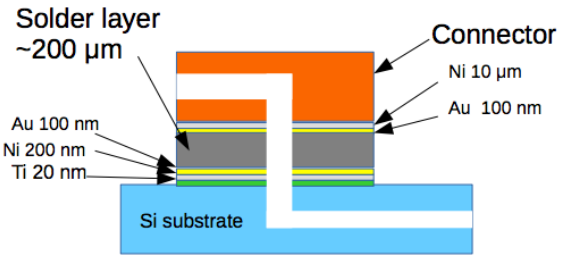
- Power consumption can go up to ~40W/module.
- Keep the sensors at < -20 °C to minimize the effects of radiation damage, and avoid thermal runaway
- Novel method: evaporate CO_2 via micro-channels etched in Si substrate ➔ Same Thermal Expansion Coefficient (CTE)

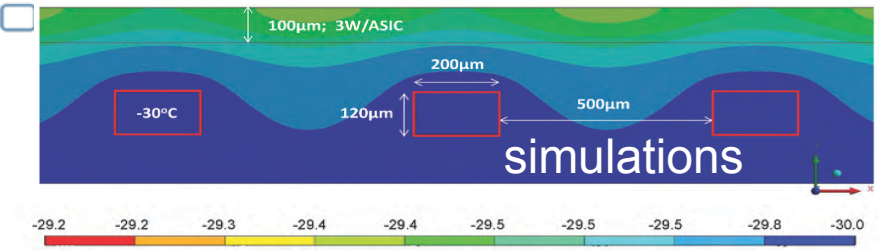
Cross section of the module concept

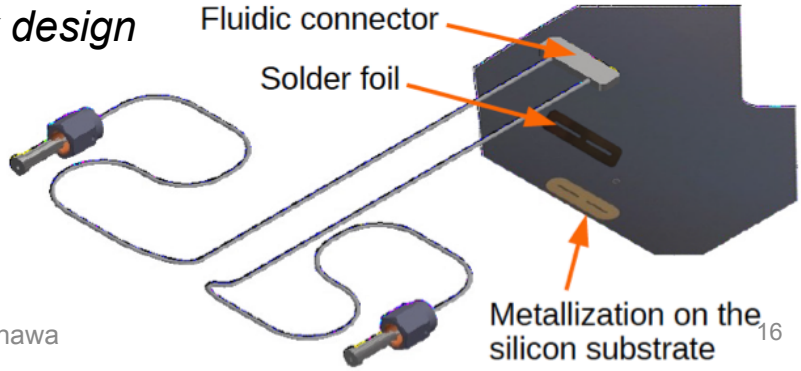




Race track design







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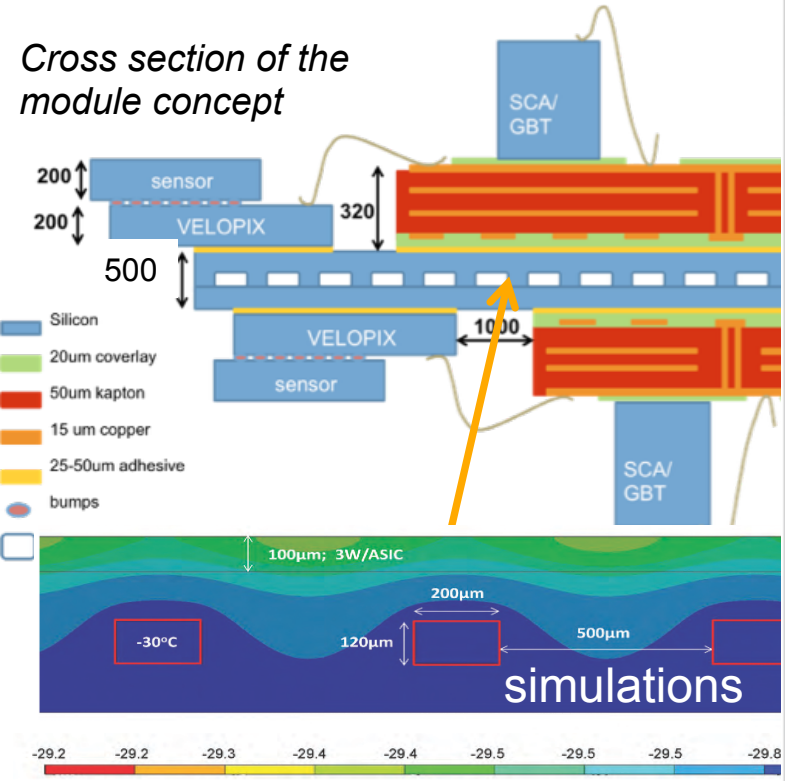
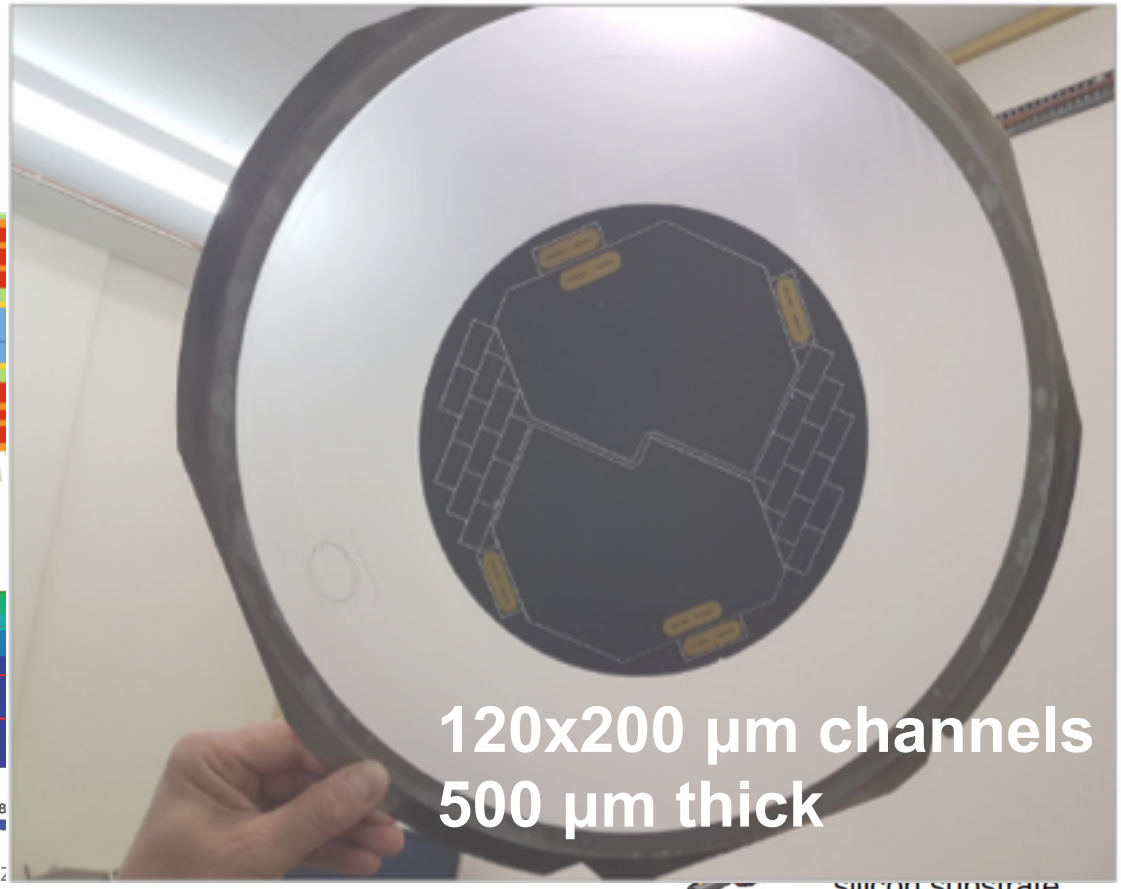
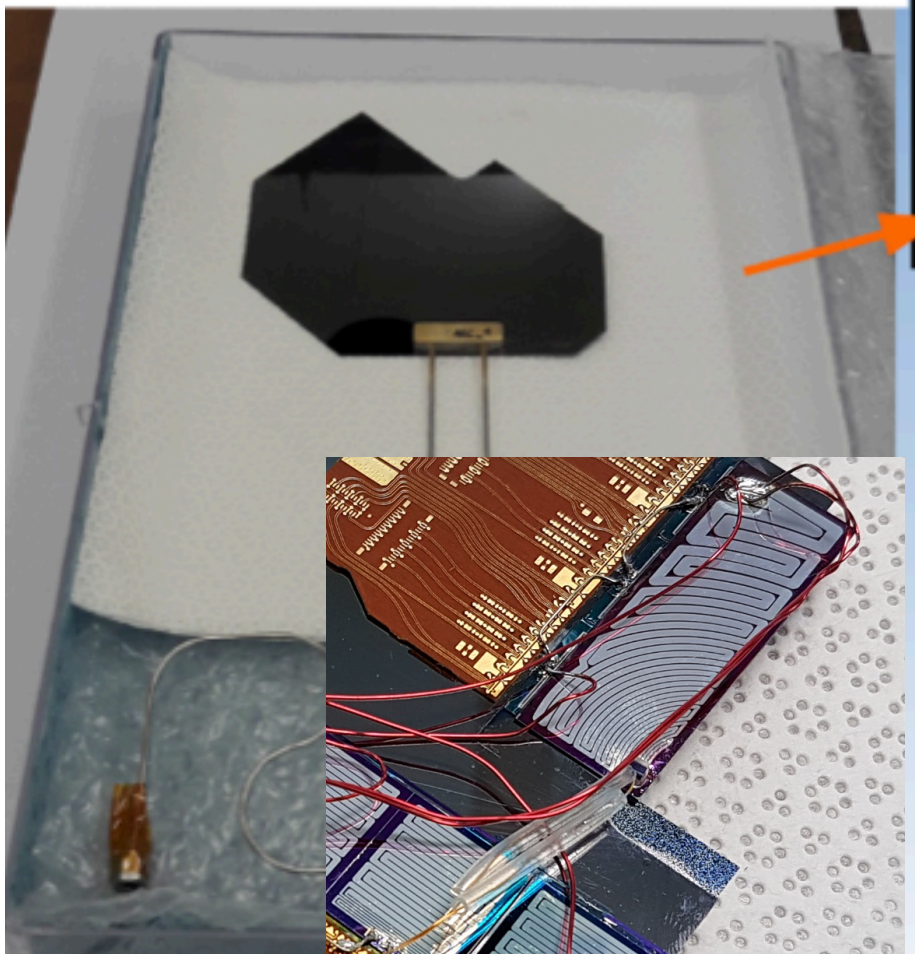
Cross section of the module concept





Microchannel Performance

First microchannels soldered on September 1st 2017

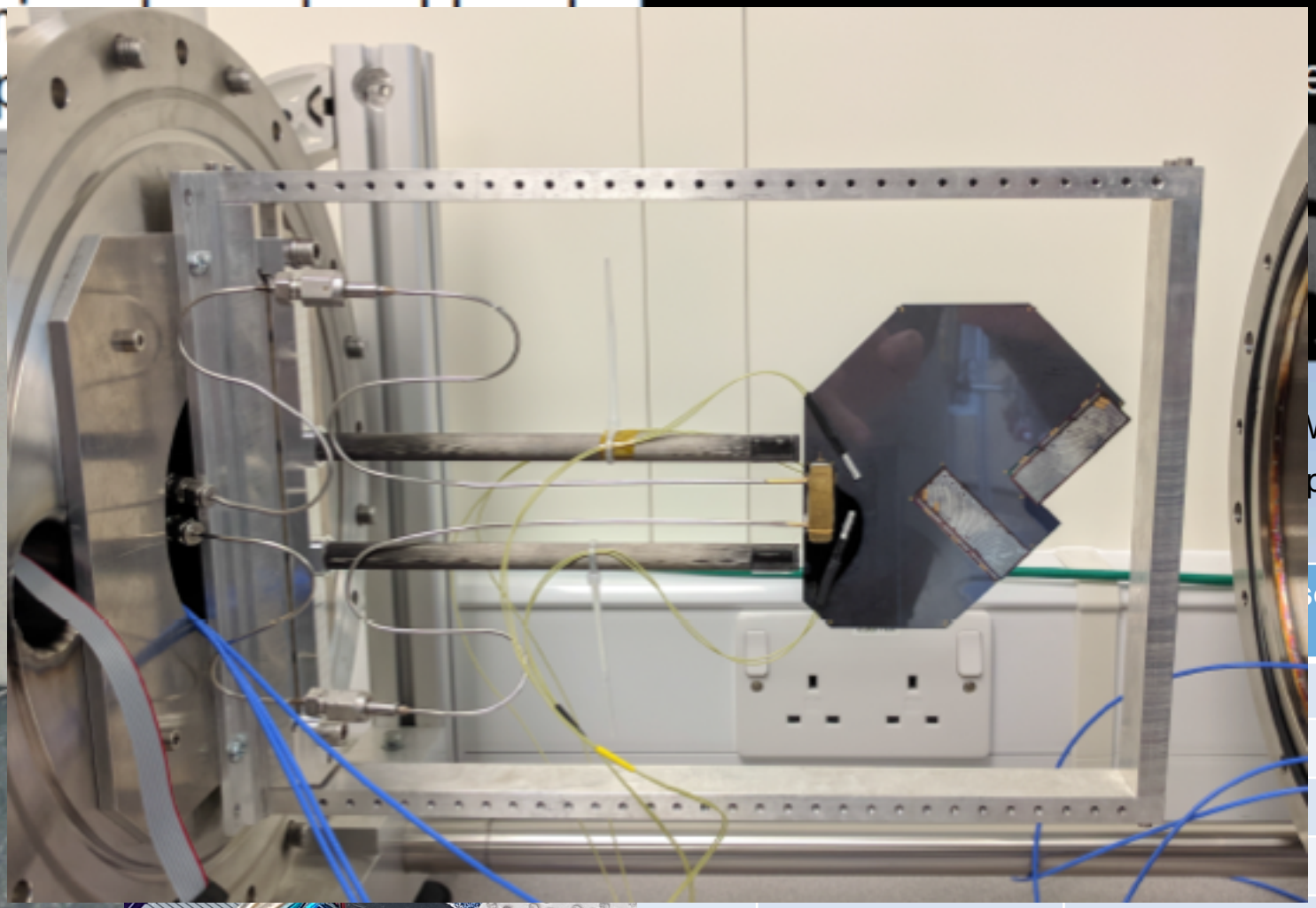


- Overhang sensor powered up to 1.3W
- Temperatures measured with PT100 probes
- In vacuum

Sensor Power (W)	dT (C) of Sensor tip
0	2.7
0.100	2.9
0.240	3.3
0.400	3.7
0.650	4.2
0.940	5.0
1.28	5.7

Realistic heaters glued with Araldite 2020, thin layer
All four tiles powered to 26W

Microchannel Performance



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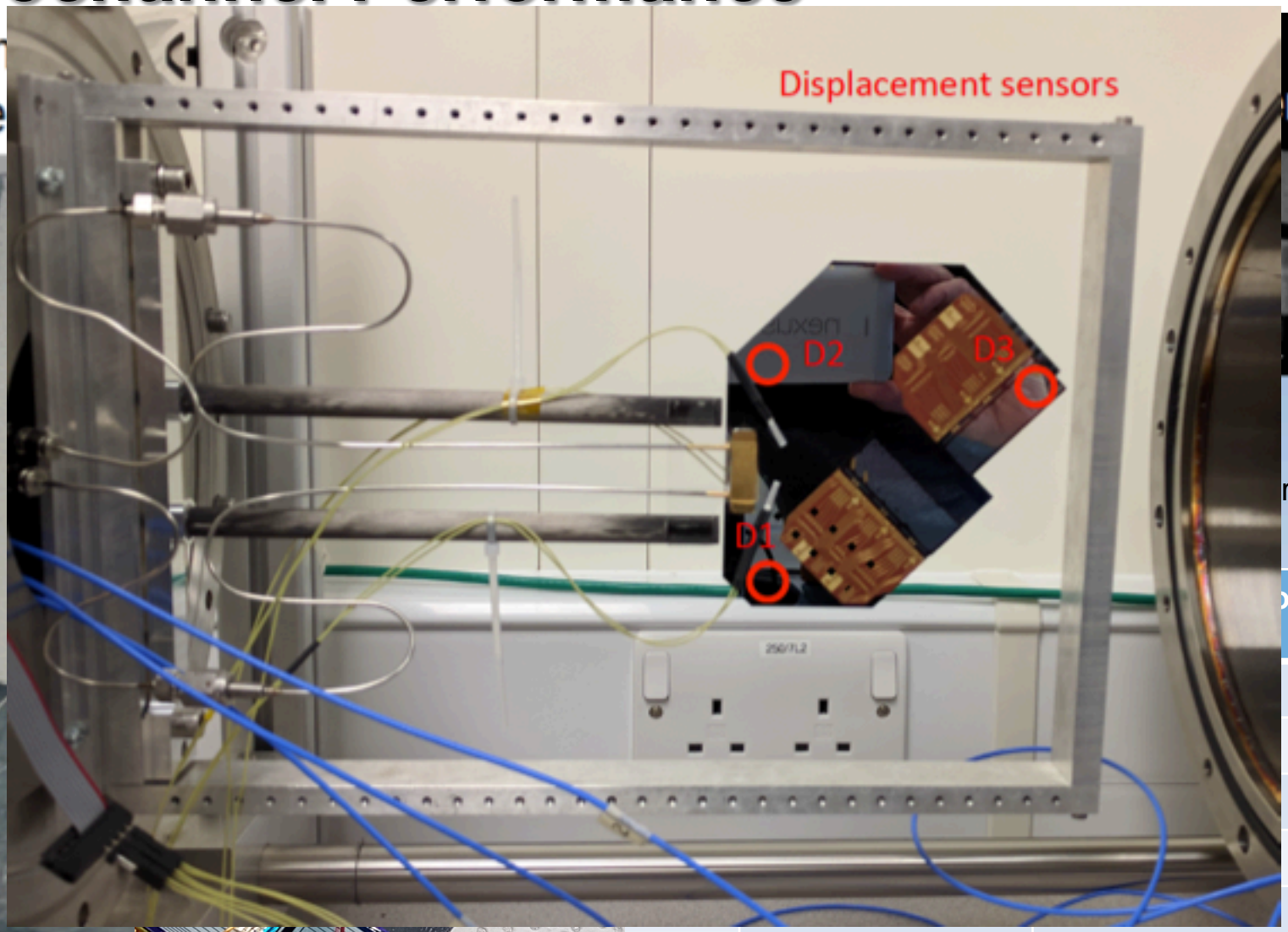

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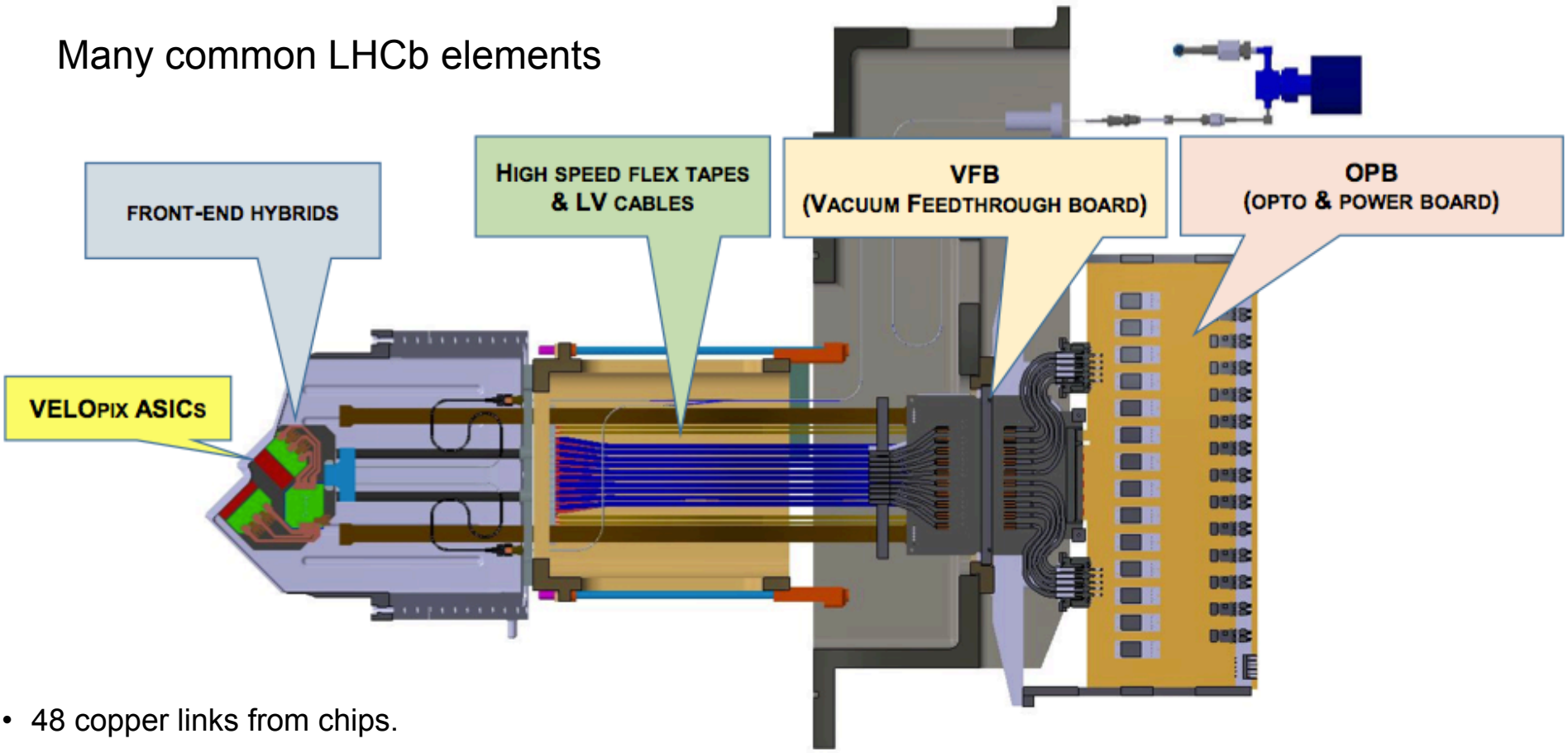
Electronics chain: overview

Many common LHCb elements



- 48 copper links from chips.
- Electrical to optical conversion outside of vacuum tank → 20 Optical links ~5 Gbit/s each
- 1 FPGA to reads out 1 module

VELO specific components involve:
data transmission,
backend data acquisition and
Time reordering of hits/clusters.

Electronics chain: overview

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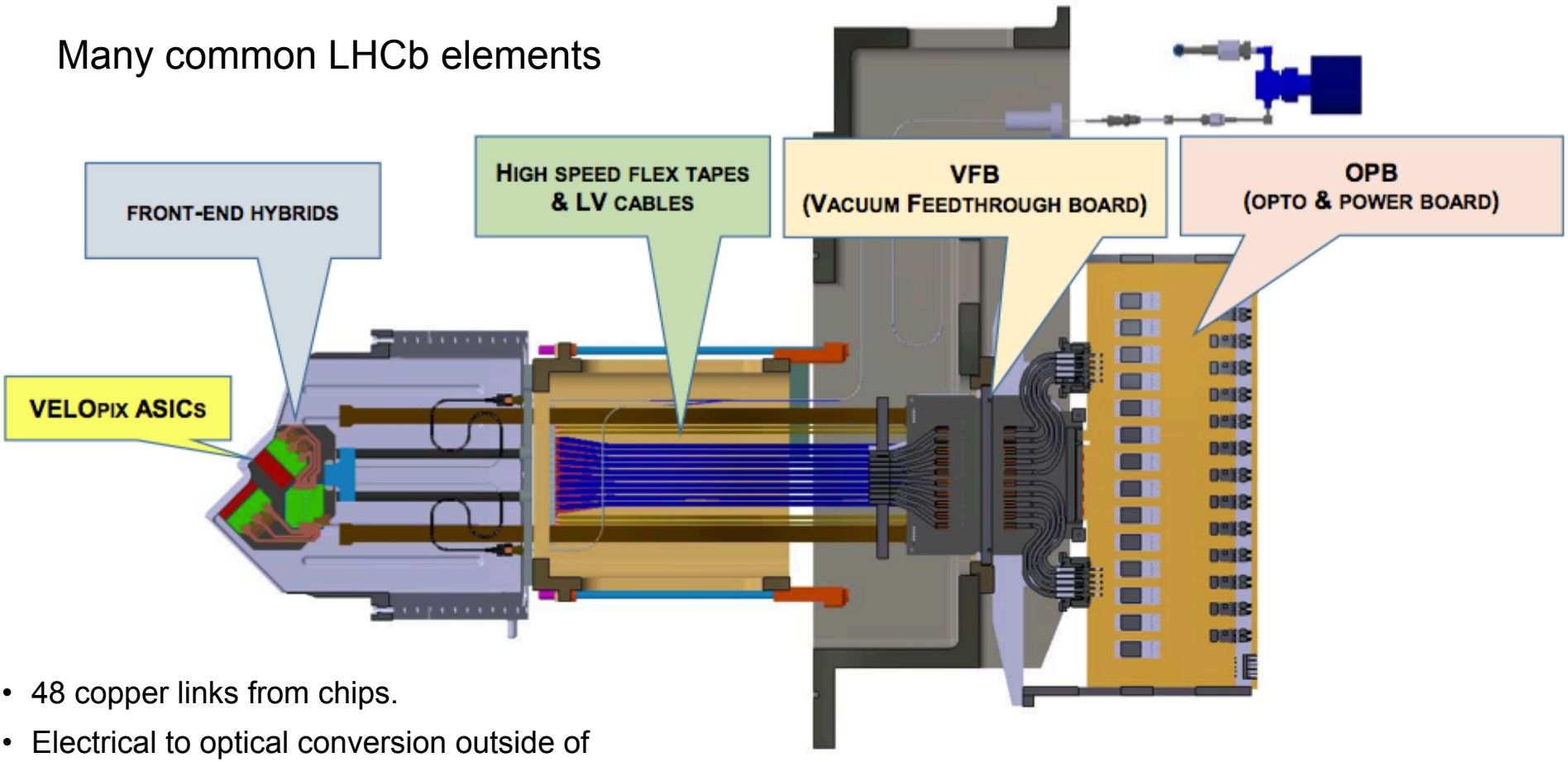

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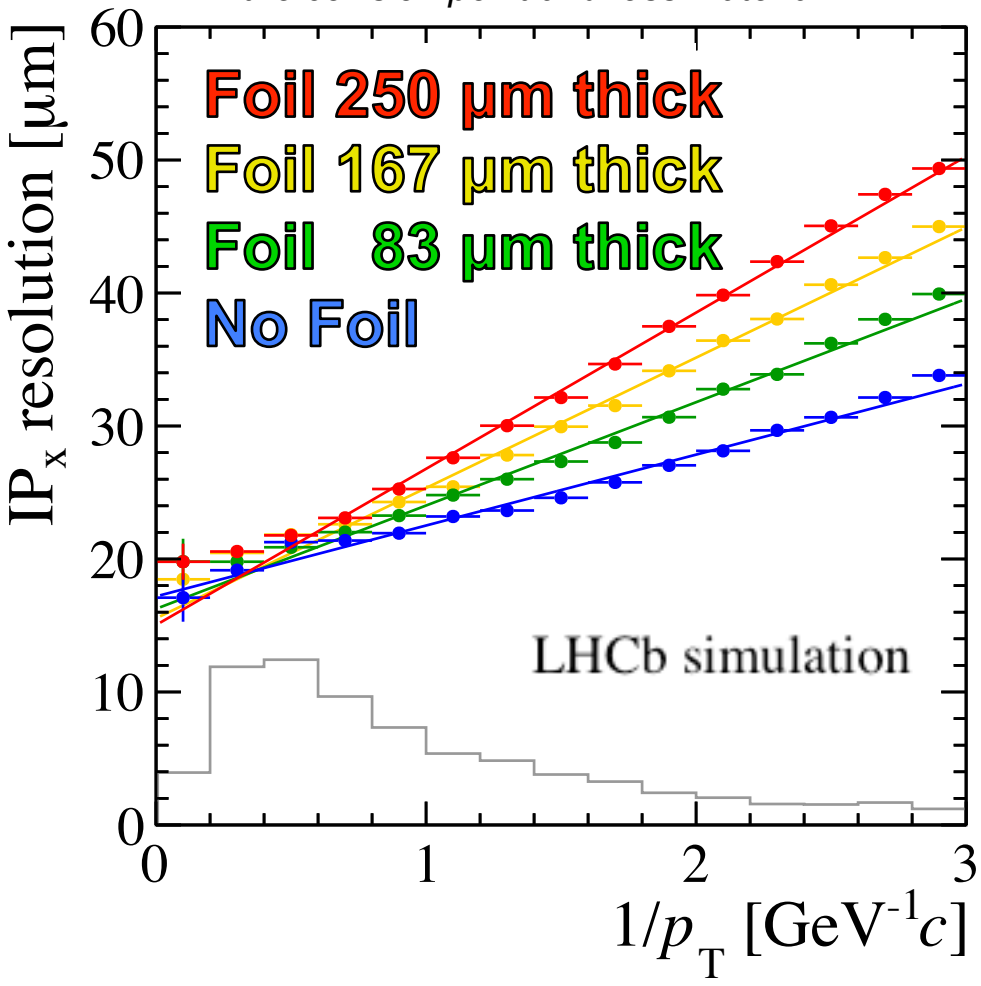
Prototypes of all components currently under test

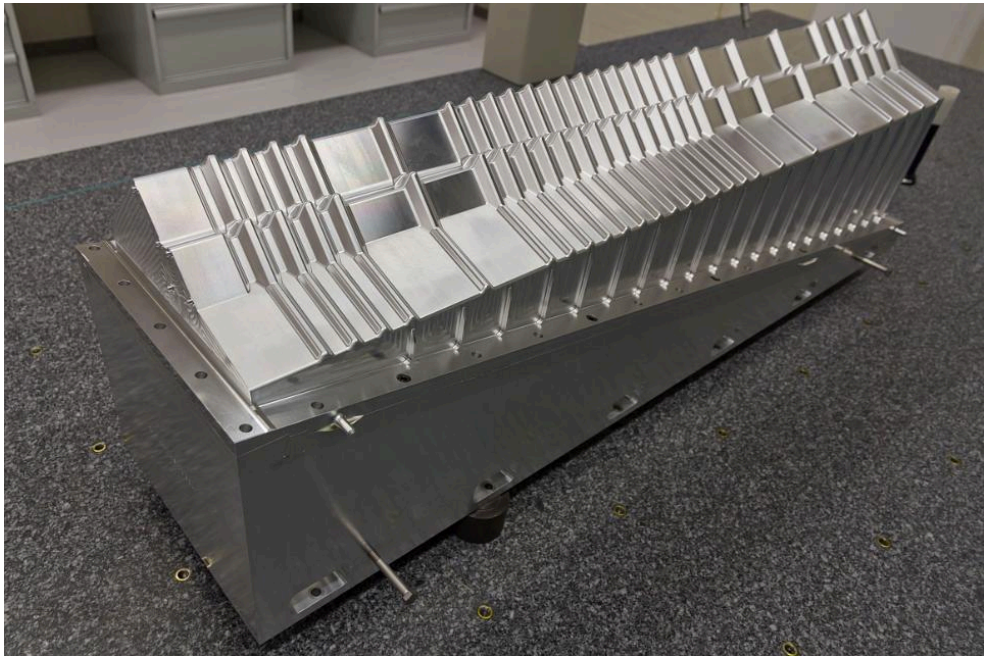
Upgrade RF Foil

- Requirements
  - Vacuum tight (< 10^{-9} mbar l/s)
  - Radiation hard
  - Low Mass
  - Good electrical conductivity
  - Thermally stable and conductive
- Material and fabrication:
  - Aluminium (AlMgMn).
  - ***500 μm thickness***:
  - By 5-axis milling of a single homogeneous block
- Chemical etching – 250μm

Impact parameter resolution is improved by going closer to the collision point and less material

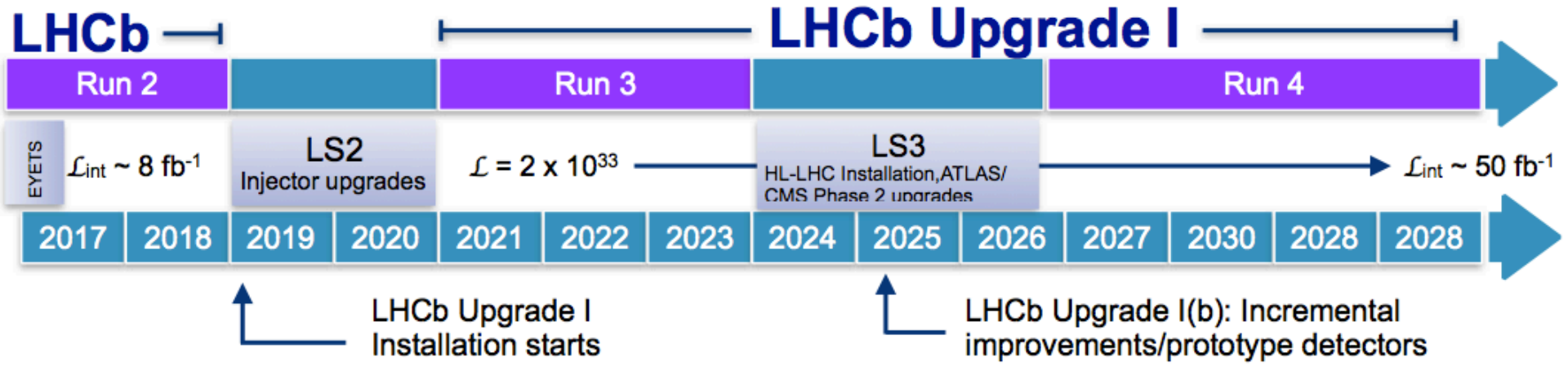


Upgrade RF Foil Prototypes



- *TL: start with an Al Block.*
- *BL: milling machine*
- *TR Full size foil with 500 μm*
- *BR: metrology of prototype*

Timeline



Many Engineering Design Reviews (EDR) done in 2017
Some parts already gone through Production Readiness Review (PRR)

Summary

- We plan to install a fully upgraded detector in the ***LS2/2019***
- With a 40 MHz "***triggerless***" readout
- Run @ L = 2 x 10^{33} cm^{-2} s^{-1} (5x now), but front-end ***40 times higher rate***.

- VELO subdetector will consist planar silicon pixel sensors with 55 x 55 μm^2 pitch
  - Get closer to the collision point
  - Bigger segmentation

- New ASIC VeloPix with 20 Gbit/s output bandwidth

- Evaporative CO_2 cooling in Silicon with a ***micro-channel*** substrate as interface

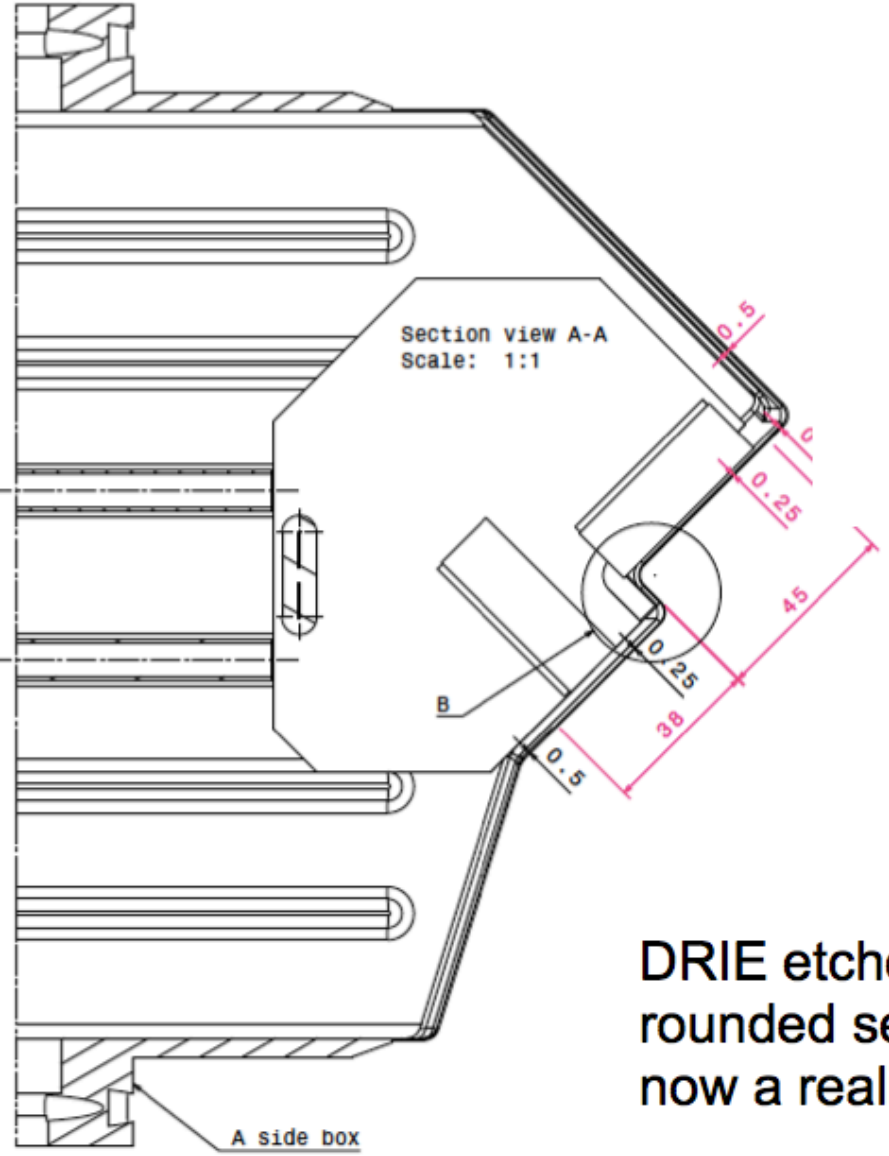
- 500/250 μm thick RF-box milled from solid block of Aluminum

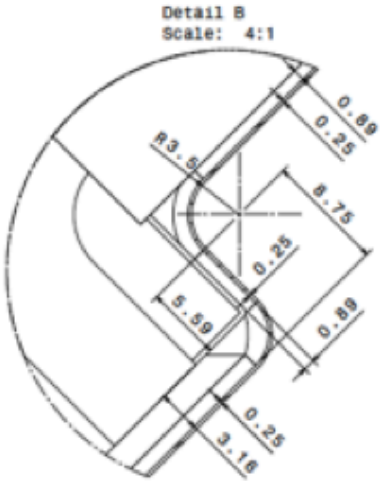
- Developments for the upgrade going well and on schedule

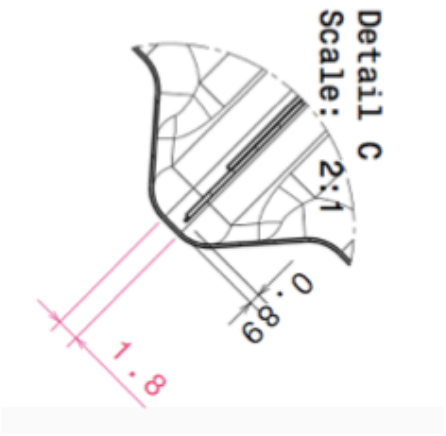
The LHCb VELO upgrade is a challenging project with many new techniques

Back up

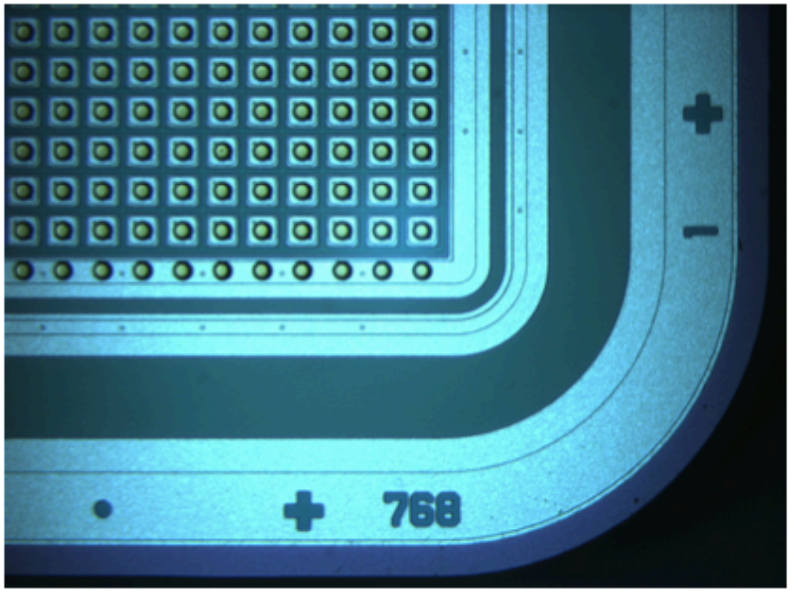
Foil clearances and dedicated sensors



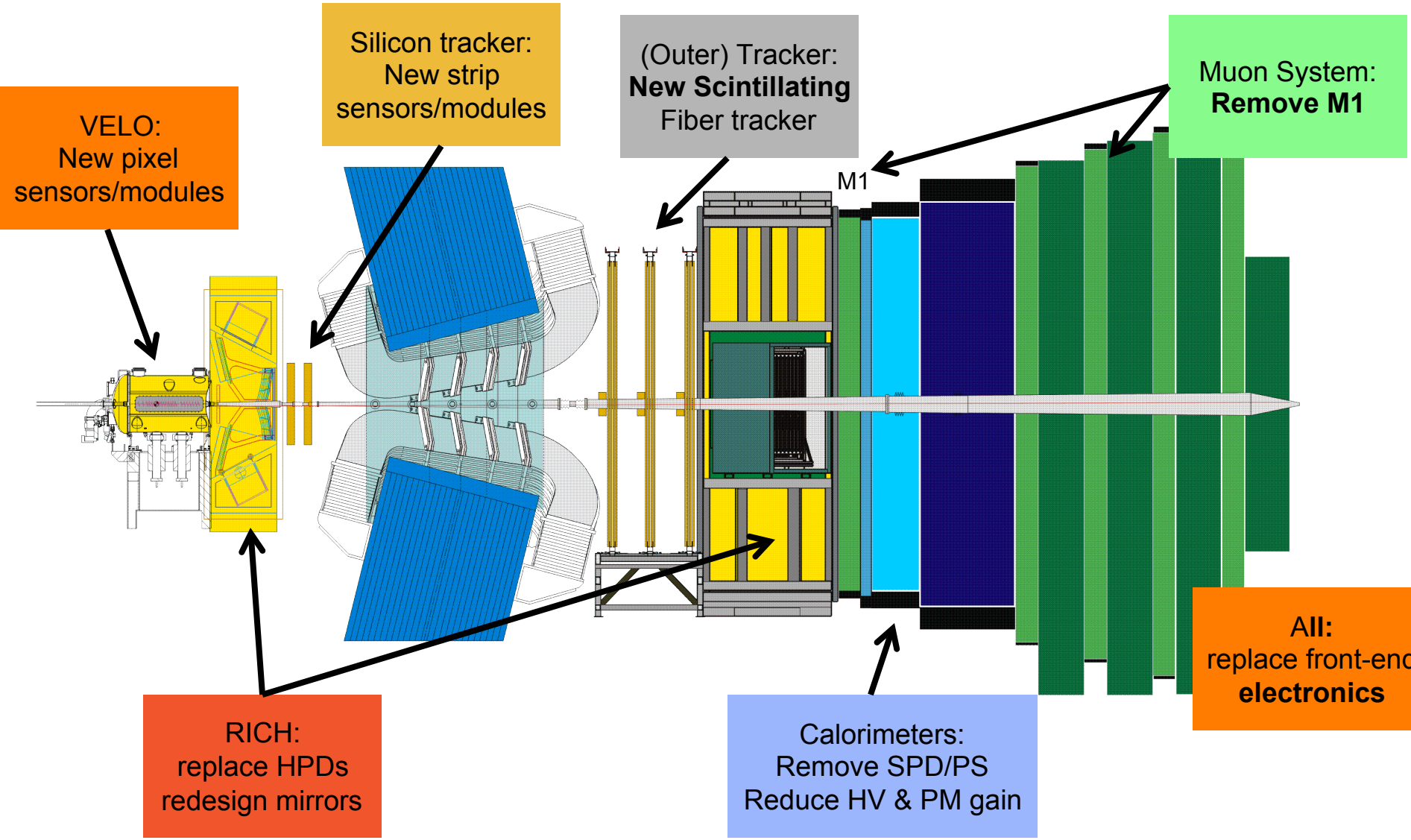




DRIE etched
rounded sensors
now a reality



LHCb Upgrade Overview



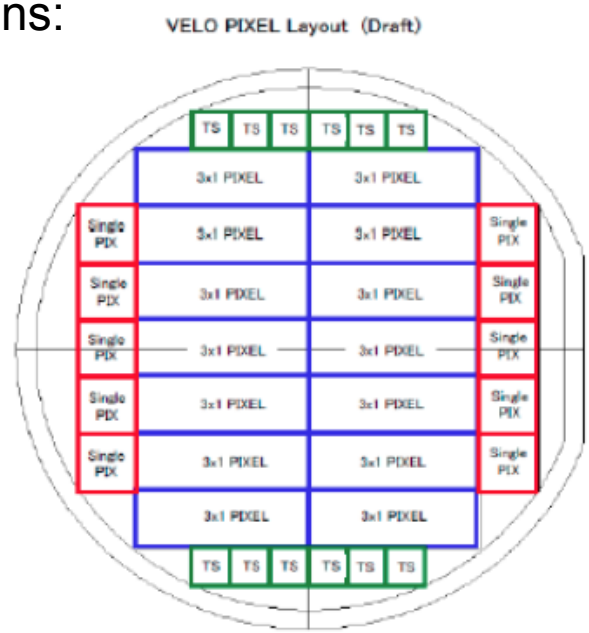
VeloPix ASIC

Specification	Timepix3	VeloPix
pixel dimension	55x55 μm^2	55x55 μm^2
matrix size	256x256	256x256
timewalk	< 25 ns	< 25 ns
Time over Threshold range	10 bit	4 bit
leakage current compensation (per pixel)	> 20 nA	> 20 nA
Time stamp resolution	1.6 ns	25 ns
Time stamp range	18 bit	12 bit
sustainable hit rate	40 MHits/s	> 600 MHits/s
output bandwidth	2.5 Gbit/s	> 13.6 Gbit/s
power consumption per chip	< 2 Watts	< 3 Watts
radiation hardness	no spec.	> 400 MRad
single event upset robust	no	yes

Silicon sensors

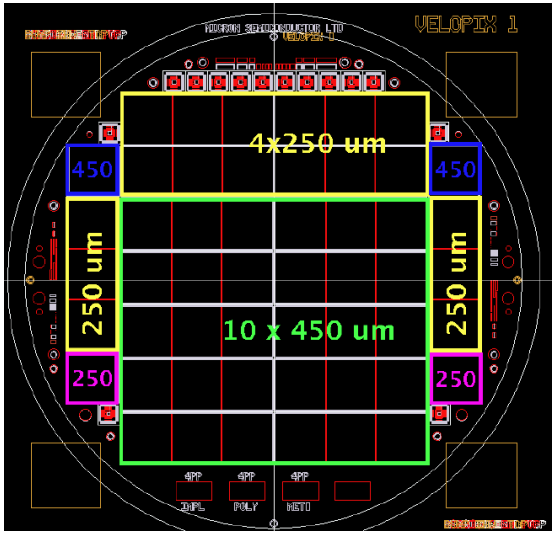
- Focus on two vendors with proven track record in radiation hard and HV tolerant sensor designs:

HPK



- n-in-p, 200 um thick
- 450 um guard ring
- 3x1 and single-ASIC sensors

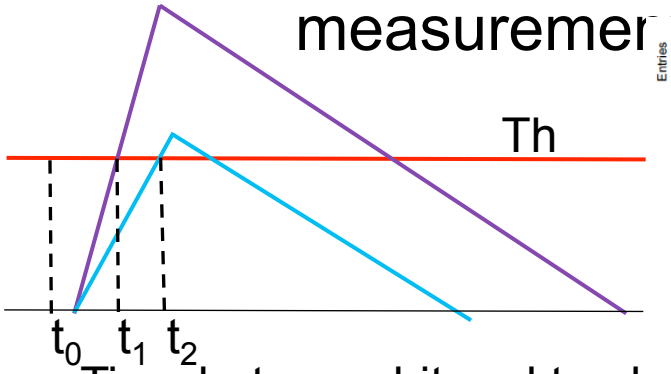
Micron



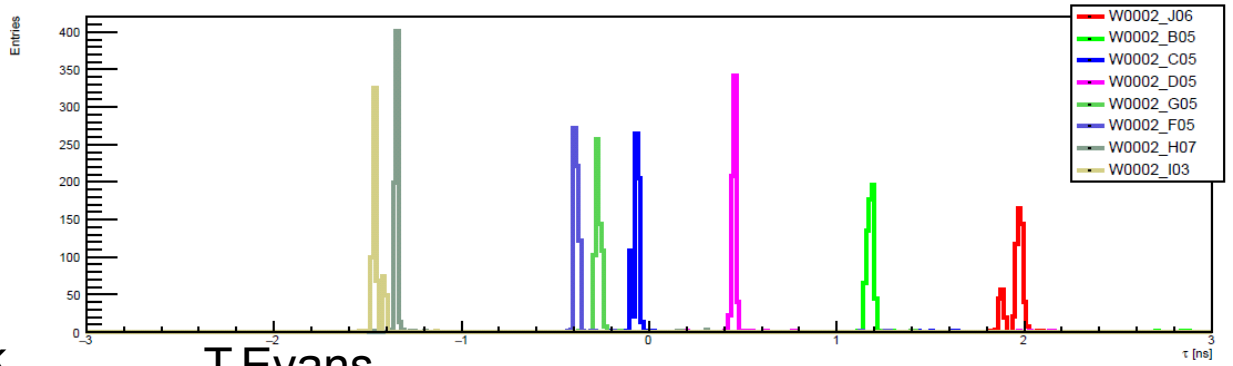
- n-in-n or n-in-p, 150/200 um
- Baseline of 450 um guard ring
- Reduced width guard rings (150um) and overlapping guard rings on backside in n-in-n case
  - Irradiation and test beam program to validate Sensor and ASIC tech at high rates.

Timing

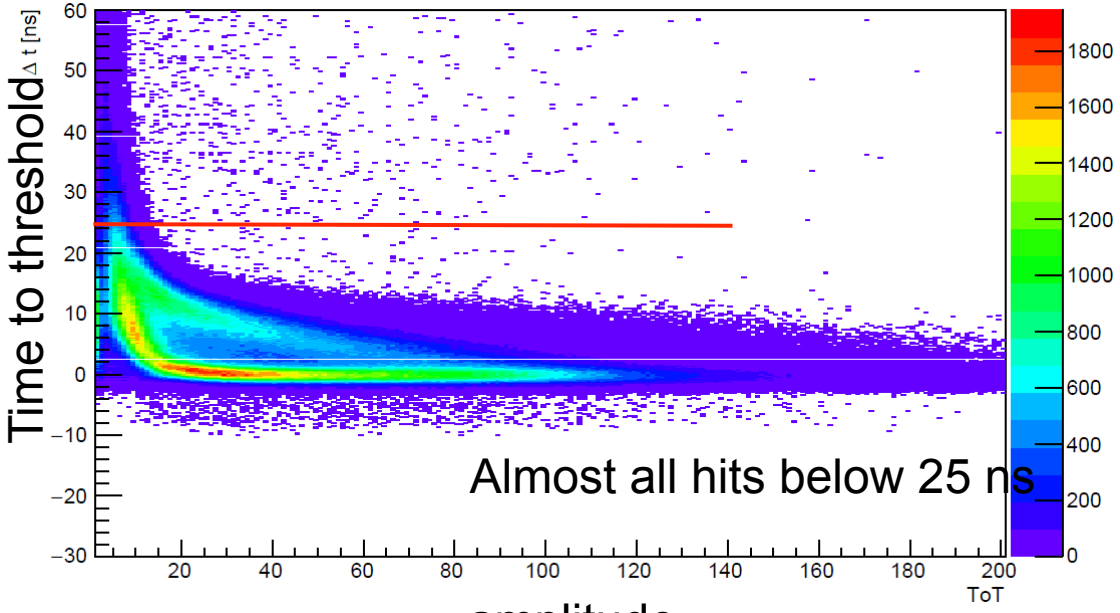
- Telescope has a very stable and precise time measuremen
- Single TPX3 measurement resolution measured to 1 ns and telescope down to 0.4 ns.



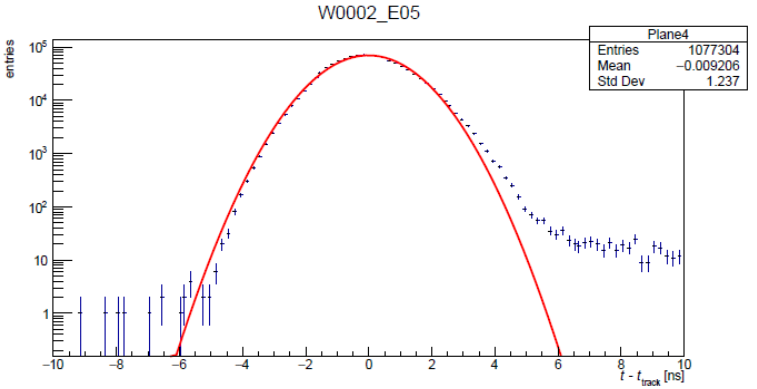
Time between hit and track



T.Evans



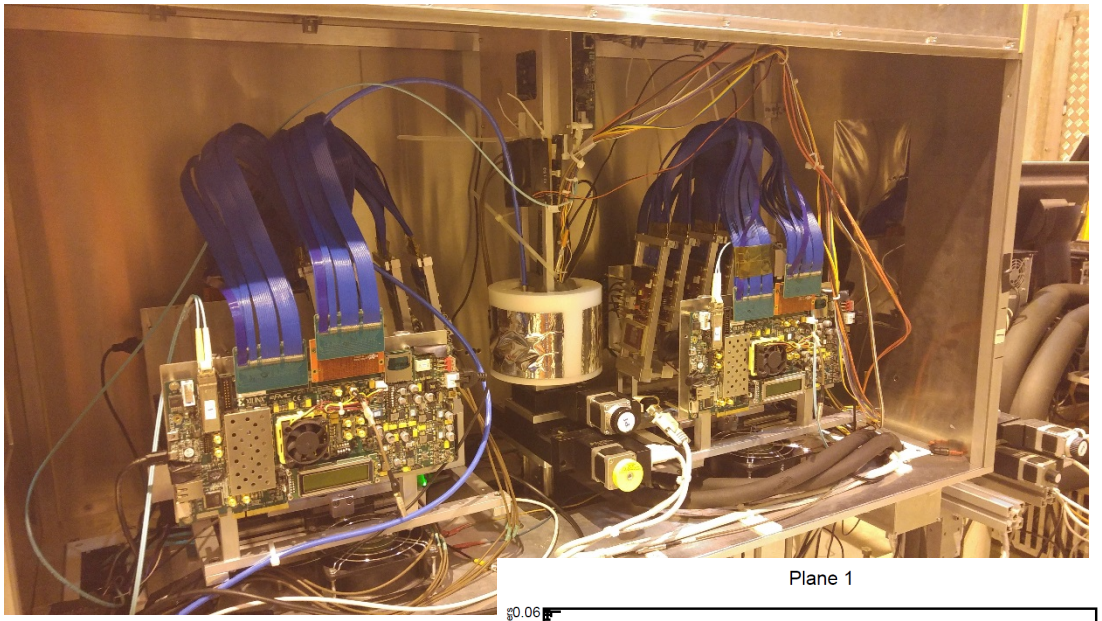
amplitude

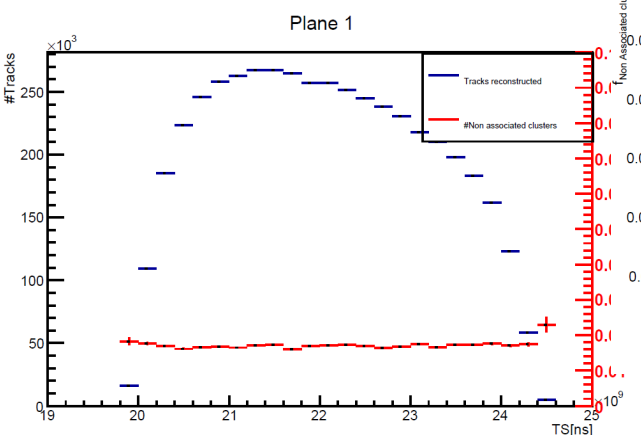


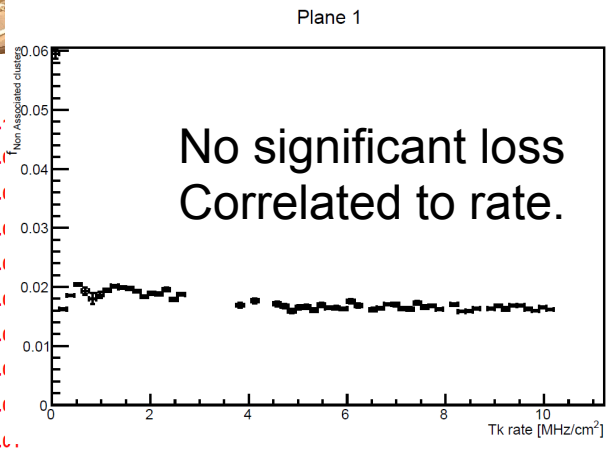
Hit time residual

The Telescope – our infrastructure.

- The **Timepix3** telescope is ***fast, precise***, and easy to combine with **Timepix3** DUTs.
- The software is written in Gaudi architecture: Kepler. ***~15k tracks/s***.
- ***Charge*** measurement and clustering give a great pointing resolution ➔down to ***2 μm***.
- Precise ***time stamps*** make it simple and clean for the PatRec.
- Tracks can be measured with ***0.4 ns timing precision***
- We have operated up to ***10 Mtracks/s/cm^2.***







A.DosilSuarez

Timeline

Upgrade TDR

module production

Sensor production

Assembly

installation

LS1

LS2

50 ns

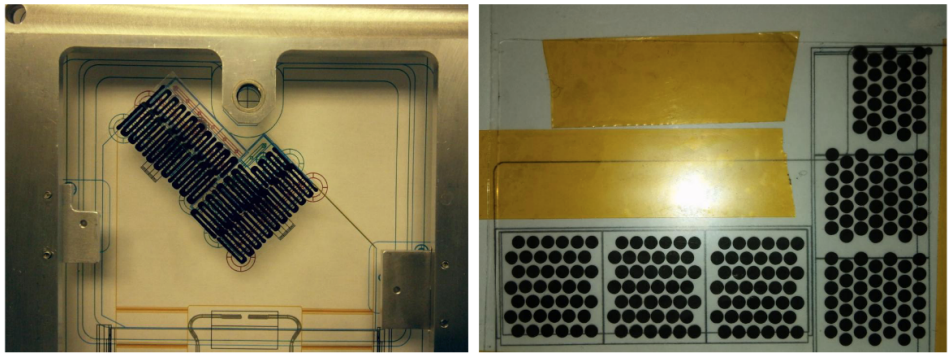
25 ns

Start-up 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 … 20xx

$\sqrt{s}$ (TeV):	0.9 - 7	-	8	-	13 -14	**LHCb Upgrade**
$\mathcal{L}$ ($cm^{-2}s^{-1}$):	10^{32}	3-4x10^{32}			4x10^{32}	20 – 30 x10^{32}
$\int \mathcal{L}dt$	3 fb^{-1}				8 fb^{-1}	> 50 fb^{-1}

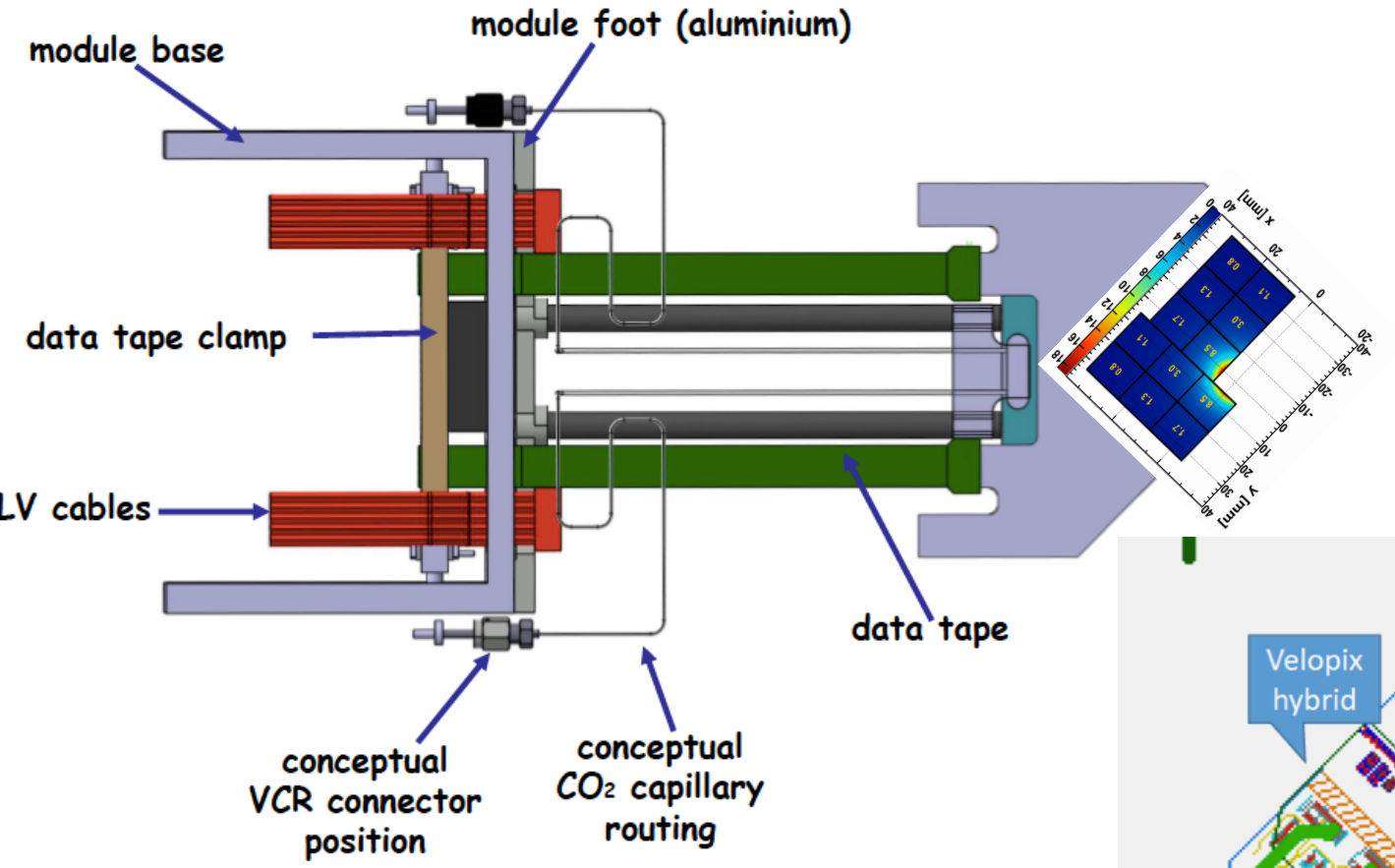
Current upgrade plan still compatible with post LS3 …

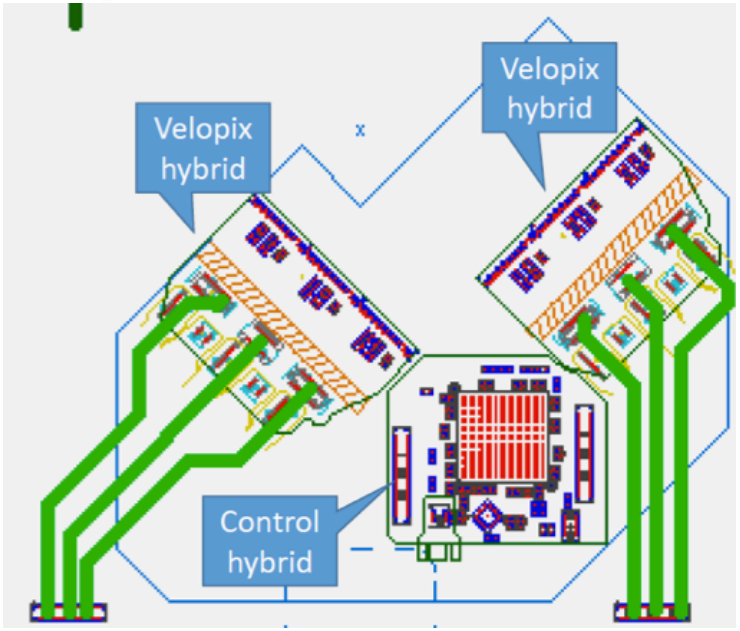
Module prototypes



The modules will be produced in both Nikhef and Mancheter University

Modules: 52 @ 25mm pitch (along beam)



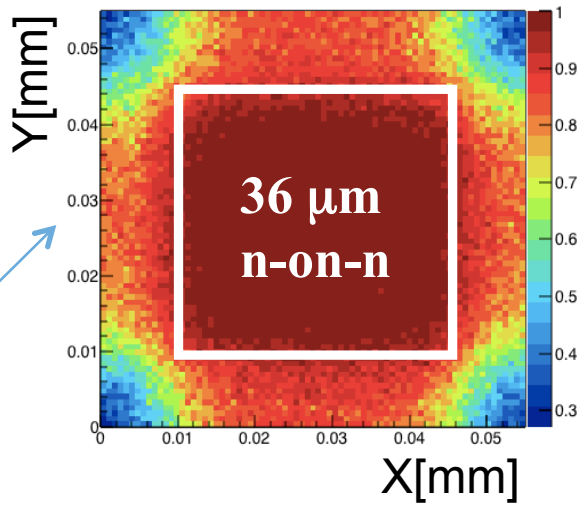


Sensor Production

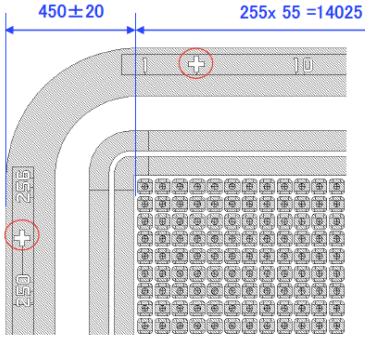
- Sensor corners to be rounded to optimise foil clearance
- Implant width: 39 µm chosen – better efficiency

Intrapixel Efficiencies

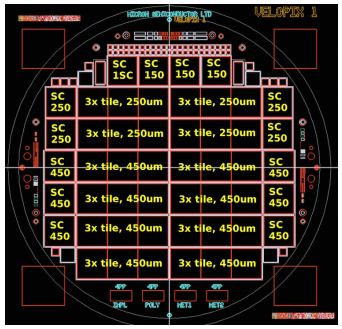
Micron



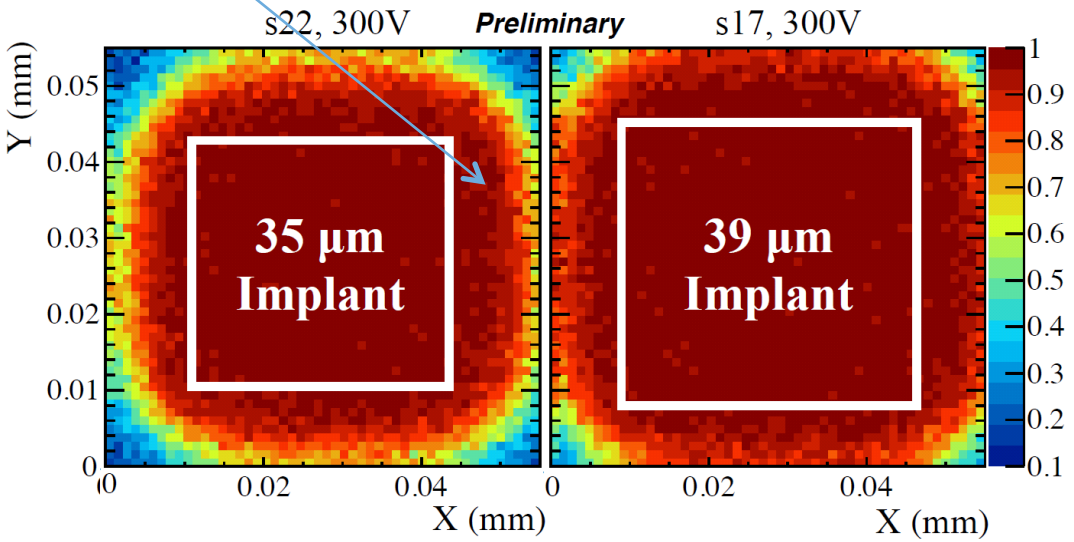
300V:
Underdepleted



Mask detail
Under Production
at HPK



Mask detail
Under Design
at Micron



HPK

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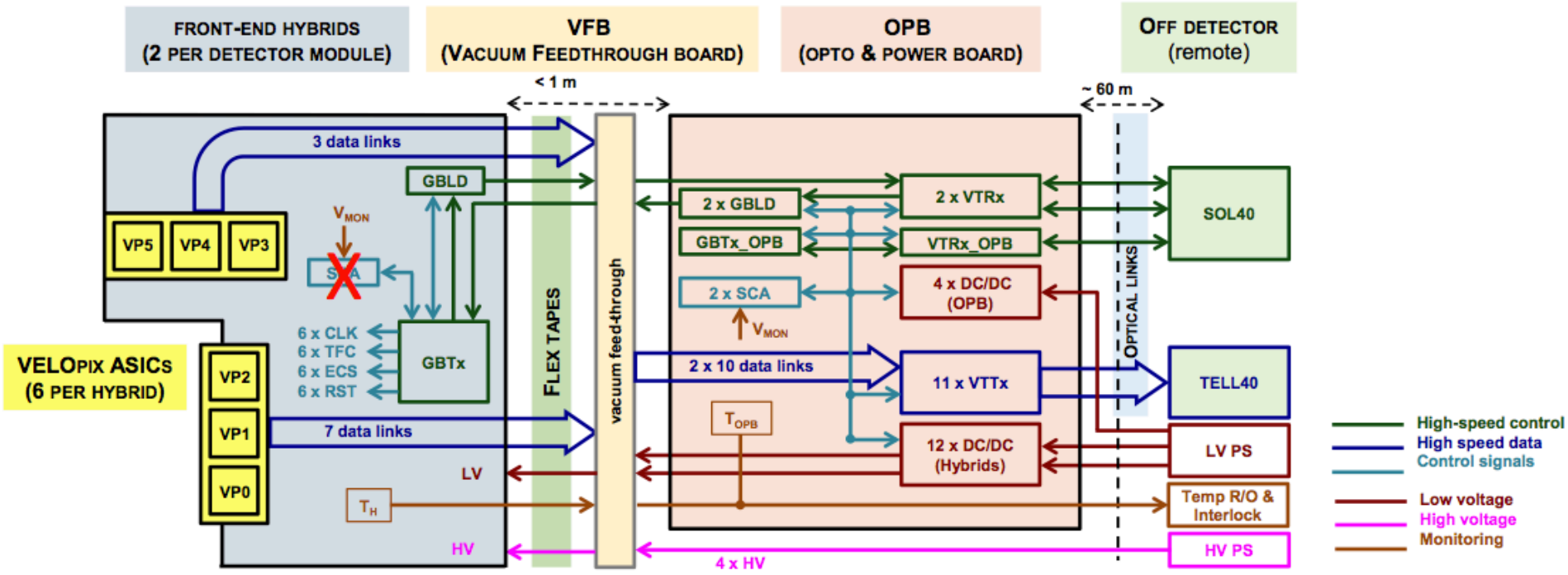

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