Istituto Nazionale di Fisica Nucleare
Sezione di Genova

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The Phase-2 ATLAS ITk Pixel Upgrade

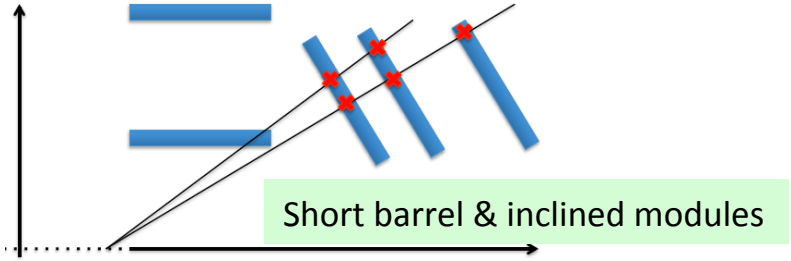
Leonardo Rossi

on behalf of the ATLAS Collaboration

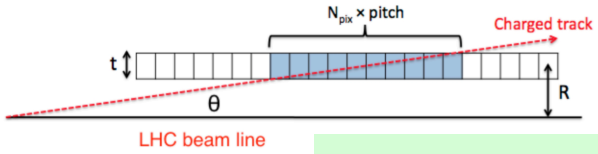
First time Pixel ITk is presented at Hiroshima Symposium

- In HSTD10 only one ITk-Pixel-related presentation (S. Veil – LBNL) proposing (and showing results for) an extended barrel layout configuration (and comparison with the alternative inclined configuration).

inclined? (optimized material on track) or **extended?** (precise high-p tracklets)



Short barrel & inclined modules



Very long barrel

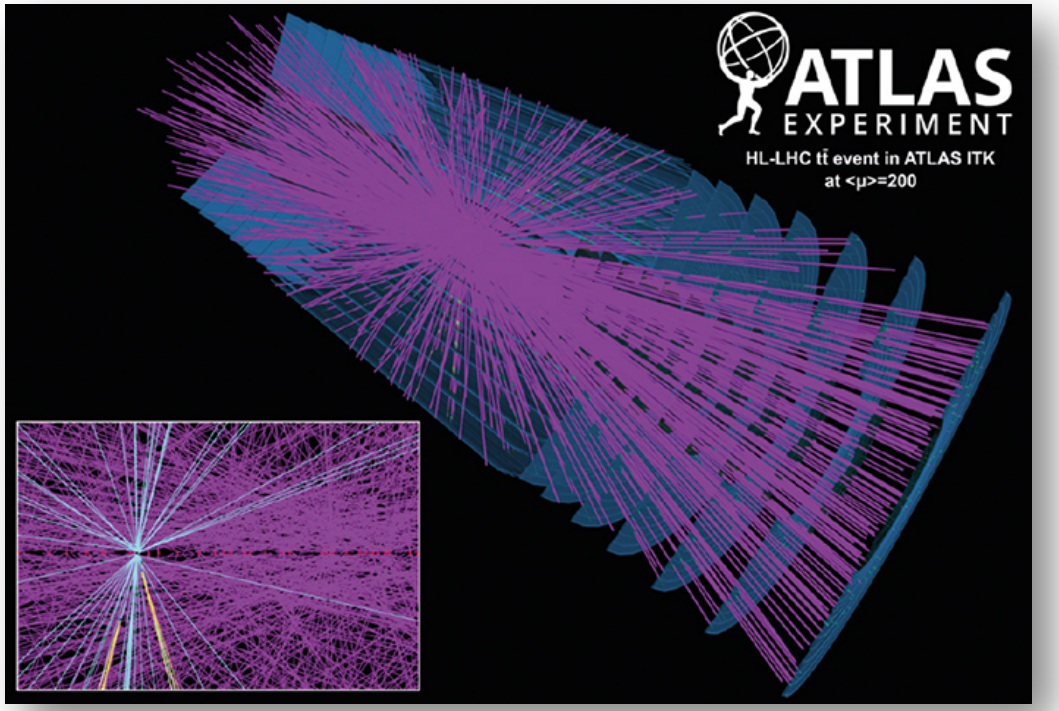
$$N_{pix} = \frac{t}{\tan\theta \times p}$$

- Lot of work done since then and not only this choice has been made, but many other parts of the ITk pixel program have been defined and new prototype results have been obtained.
- ATLAS Pixel ITk has grown to a >100 lab collaboration and is about to submit to the LHCC the TDR of the project.
- In the following I'll present the motivation behind the project (why?, when?), the most significant design choices (how?) and results obtained over the last two years.

Why ATLAS Pixel ITk?

μ= number of interactions per beam crossing

- Only technique*) allowing "cm-away" 10 μm precision measurements of track trajectories emerging from of μ=200 pp synchronous collisions at 14 TeV and able to do it up to $2*10^{16}$ MeV n_{eq} /cm^2 doses (HL-LHC specs).



~12000 tracks in the tracker acceptance (each 25 nsec)

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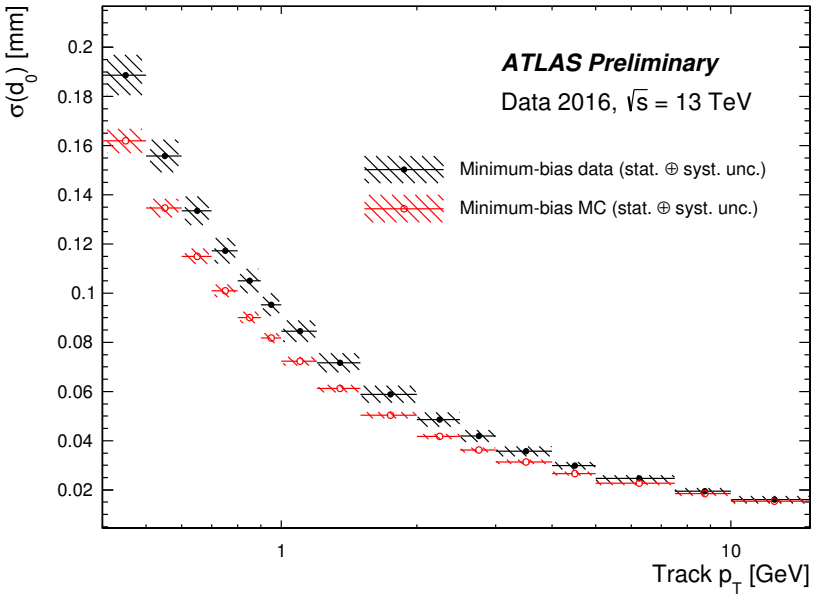
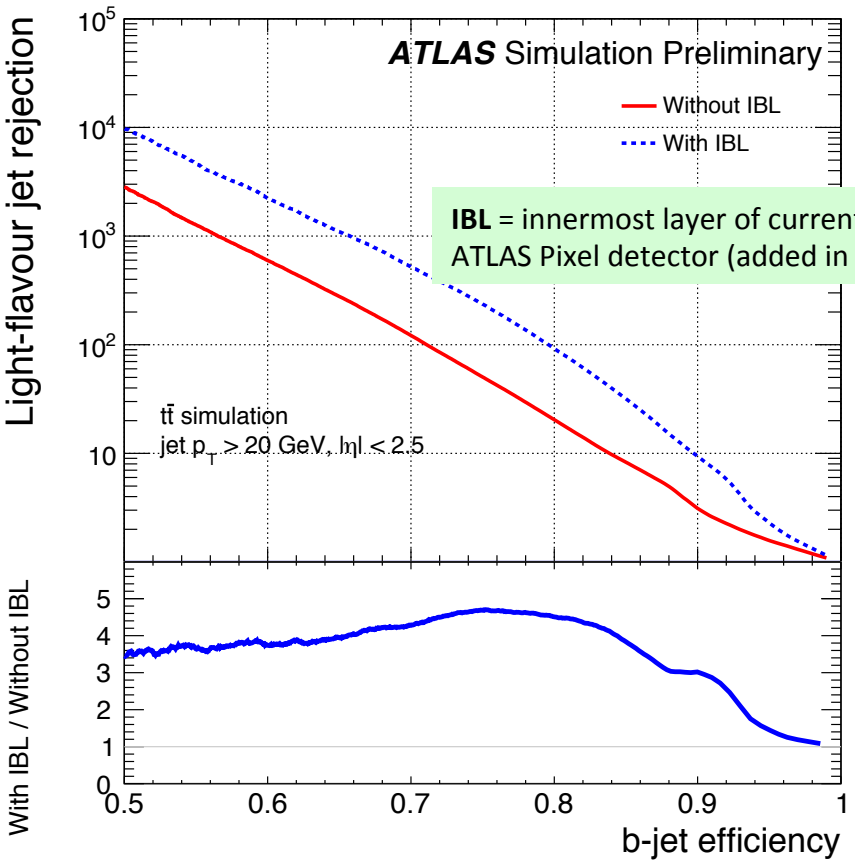
*) thanks to 4 10^4 adjacent and independent sensors per cm^2, all of them with 25ns time resolution.

- Current ATLAS Pixel has proven to work stably and beautifully up to μ=60 (even if designed for μ=25).

C. Martin presentation





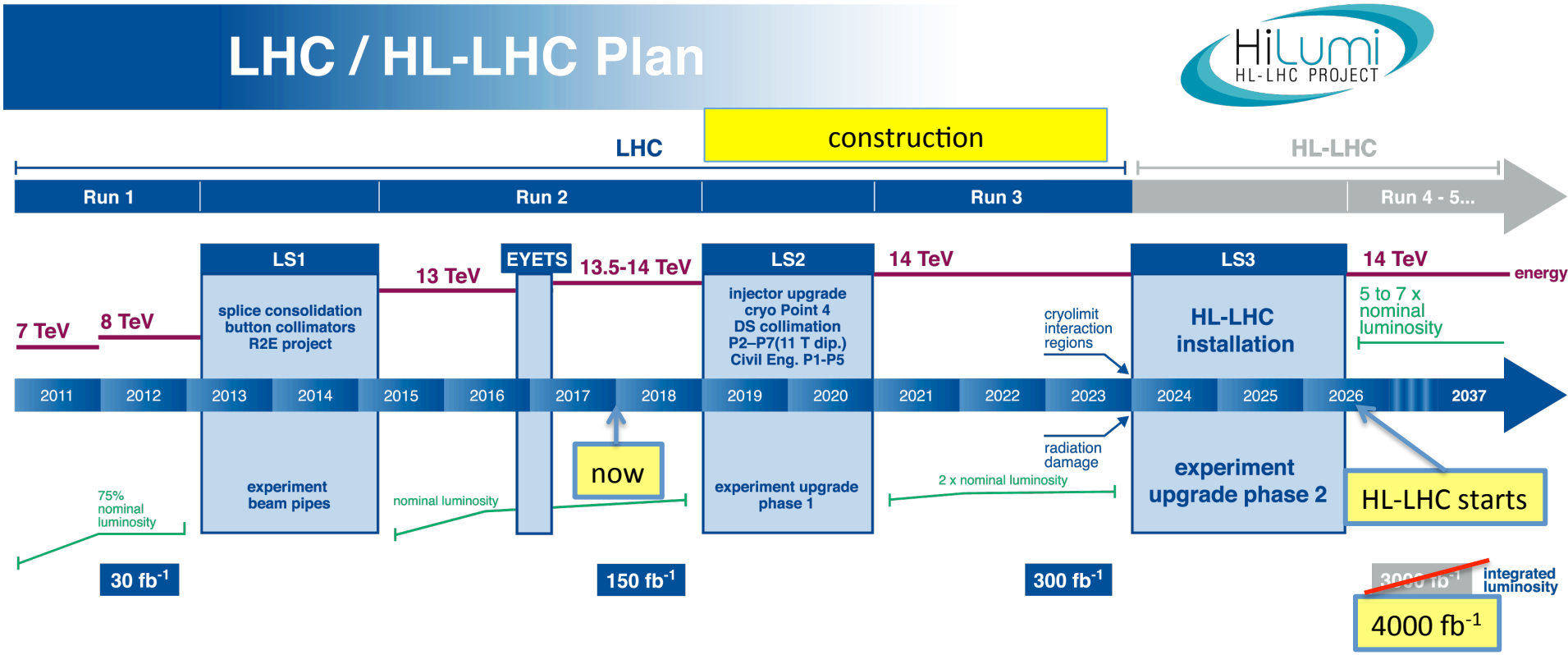
IBL = innermost layer of current ATLAS Pixel detector (added in 2015)

- The design spec extrapolation (LHC→HL-LHC) is not huge (~7). Similar factor in the ratio of areas (then in collaborators…) as a larger role is given to Pixel in HL-LHC tracker (no more large-R gaseous detectors). Project is doable, but requires to push further a technology already on the edge. Challenging (and possibly fun)!

When ATLAS Pixel ITk?

Thanks F. Hartmann!

LHC / HL-LHC Plan



- Driven by HL-LHC schedule (we are still 9 yrs from HL-LHC start, but this is less than the time needed from TDR (1998) to data (2010) for the current ATLAS Pixel→ the timeline of the ATLAS ITk Pixel project is quite critical)
- Must be ready for installation in 2024→ construction from 2019 to 2023, then integration at CERN and system tests.

How (do we plan to build the) ATLAS Pixel ITk?

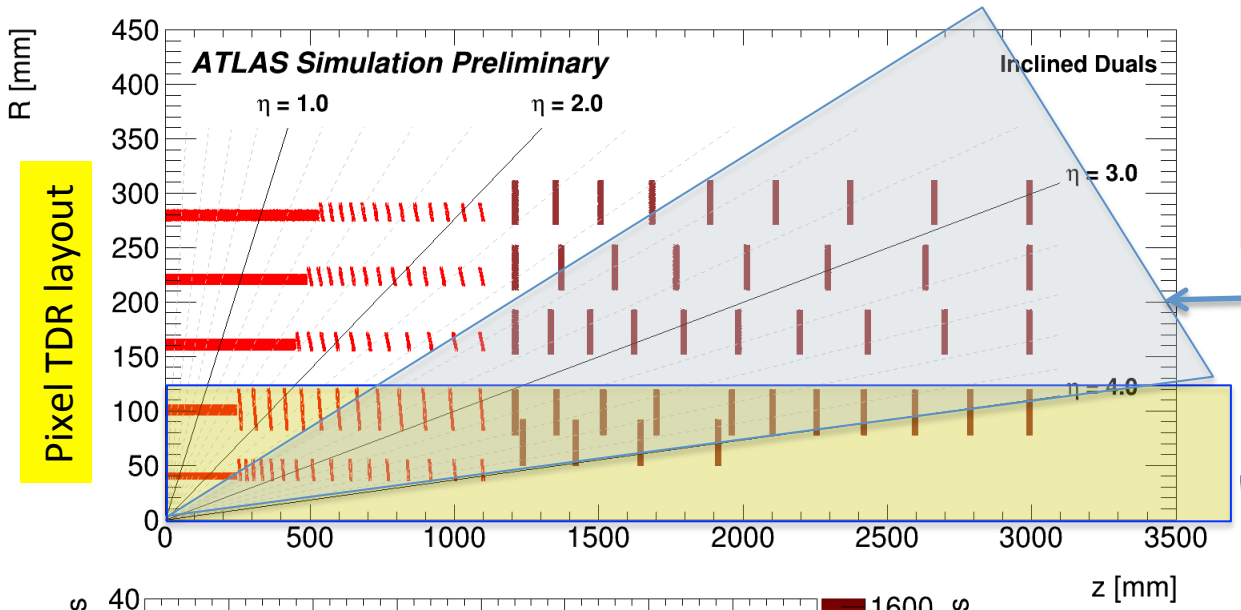
The layout

- This is the basic strategic choice and the skeleton around which the project should be refined.
- Related to viable solutions in all sectors (sensors, electronics, mechanics, cooling services, etc.) and driven by the mission of the ITk in the ATLAS experimental program (reconstruct, in the HL-LHC environment, tracks and vertices and tag short-lived particles at least as efficiently and precisely as currently done at LHC)
- As usual in this phase of the project many solutions were proposed and studied using full simulation (including a realistic evaluation of supports and services).
- The TDR baseline design was defined aiming at:
  - > 5 hits close to the interaction point with high granularity and accuracy ~10μm
  - > 9 precision hits over the full acceptance ($-4<\eta<4$) and up to R~1m
  - minimization of material over the full η-acceptance
  - best physics reach (good b-tagging, efficient reconstruction in dense jets and in high-pile-up environment, and precise track & vertex measurements)

P. Phillips poster

Short barrel followed by inclined modules and then by disks (of different radial coverage → a measurement "layer" is not necessarily coplanar)

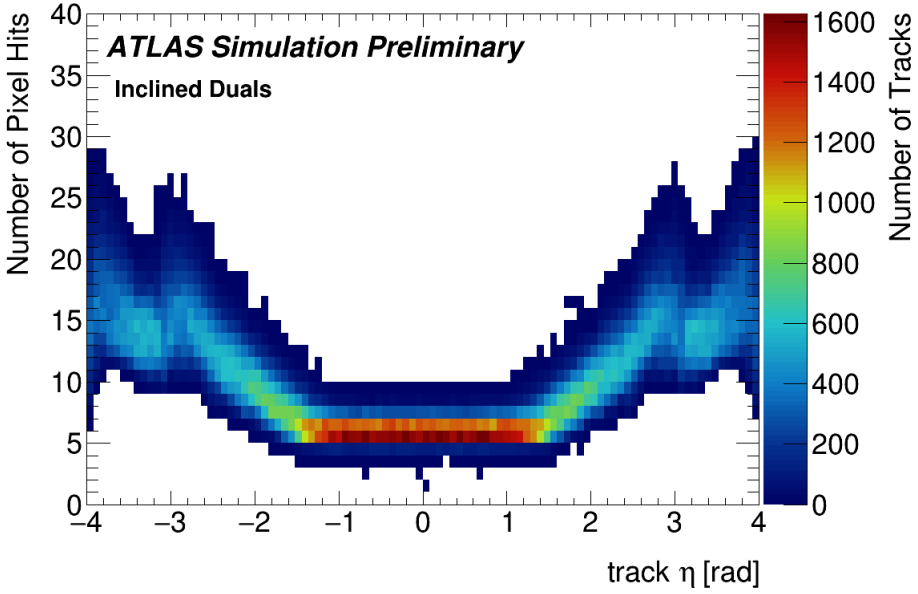
Pixel TDR layout

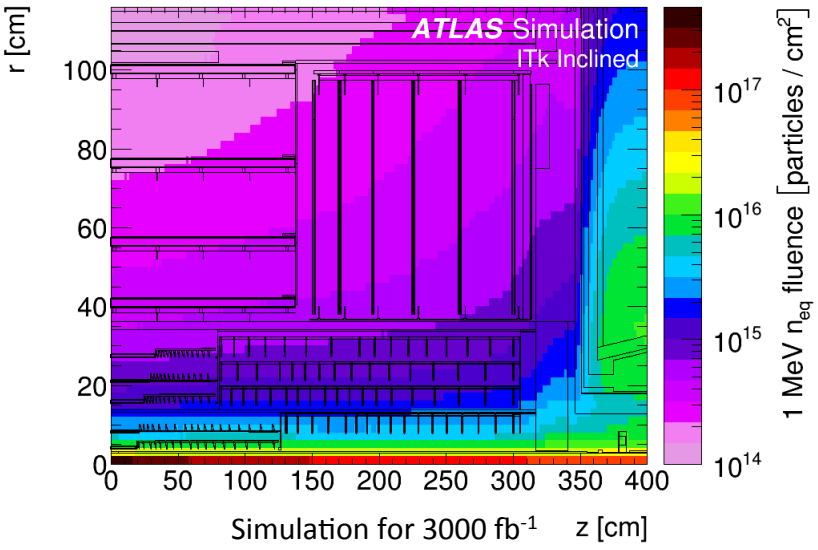


Active area: **12.7 m²**
Pixel size: 50x50 (or 25x100) μm²
# of modules: 10276
# of FE chips: 33184
# of channels: **~5 10⁹**

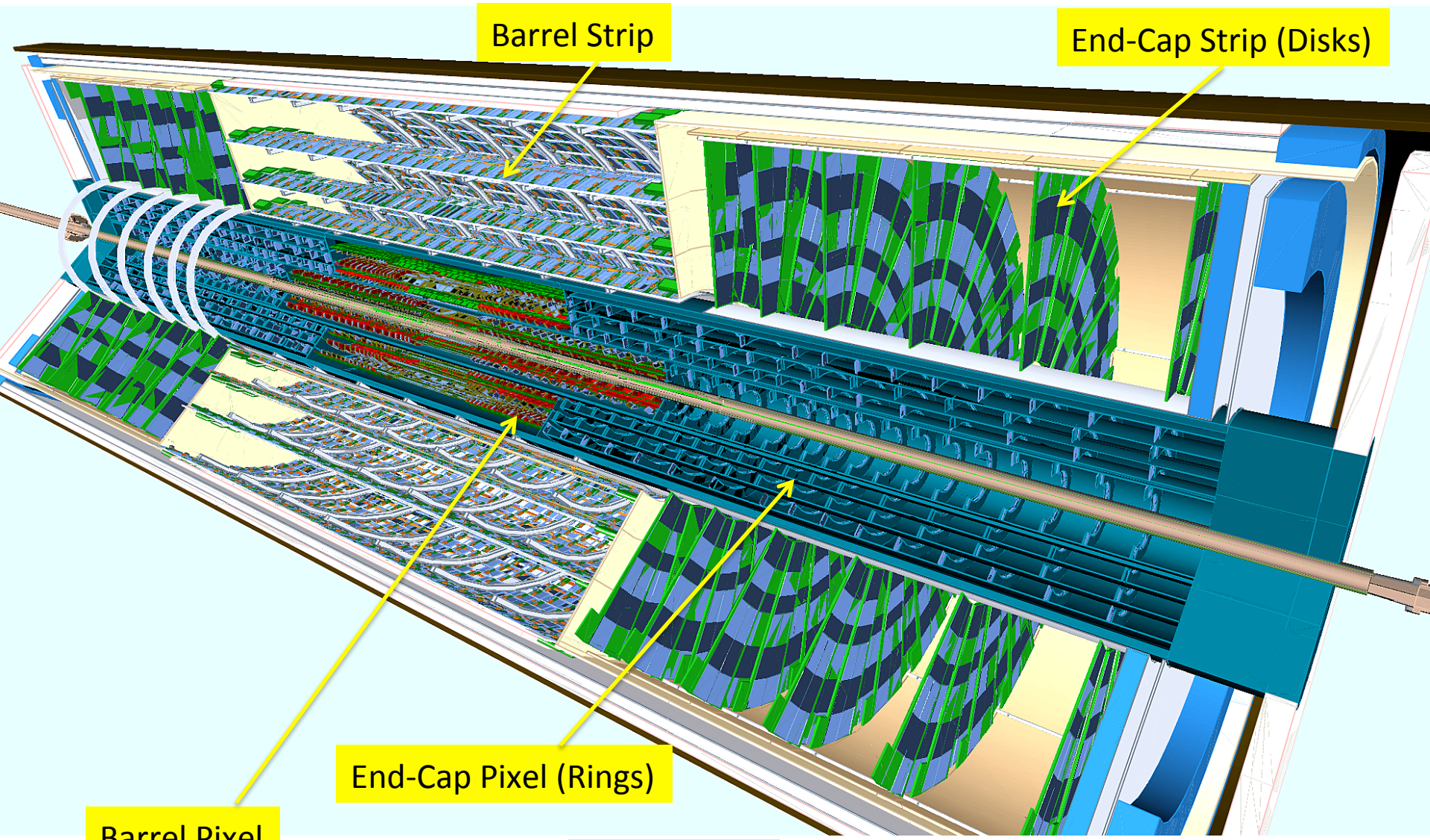
Additional η-acceptance

Insertable inner layers





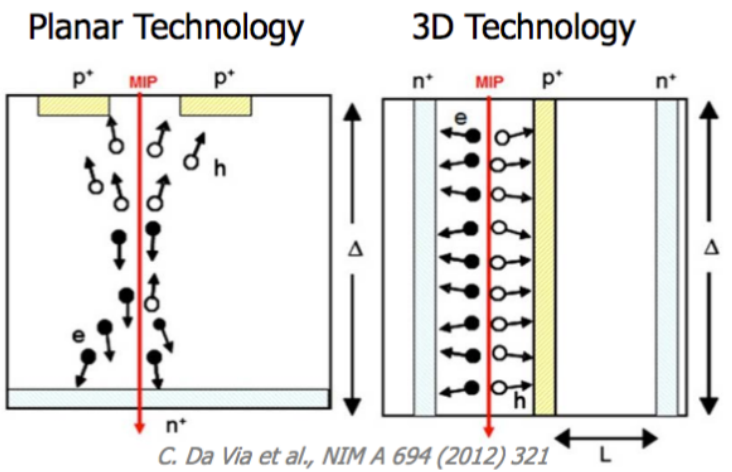
An artistic view to get a better feeling of the ITk layout



R~1m, L~7m

The Sensors

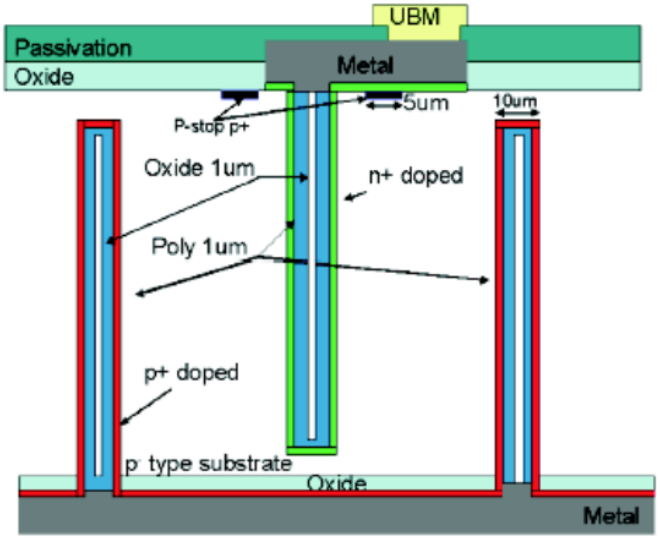
- Sensor technology must be tailored to the radiation environment (and financial constraints)
- Baseline is 3D for the innermost layer(s) and planar elsewhere. Outer barrel layer (~1/5 total area) may employ CMOS.



C. Da Via et al., NIM A 694 (2012) 321

3D sensors

- Used in IBL (and in operation since 2015)
- More rad-hard (and less power hungry), but also higher C_{IN} and more complex production process (yield and less available firms)
- ➔naturally confined to innermost layer(s)
- Challenges (vs IBL):
  - Smaller pixel needed (50x50 or 25x100 μm^2)→ yield?
  - Column themselves are not efficient→ tilt sensor
  - Thinner sensors (≤150μm)→ Lower signal & yield
  - Test before BB → sacrificial metal layer



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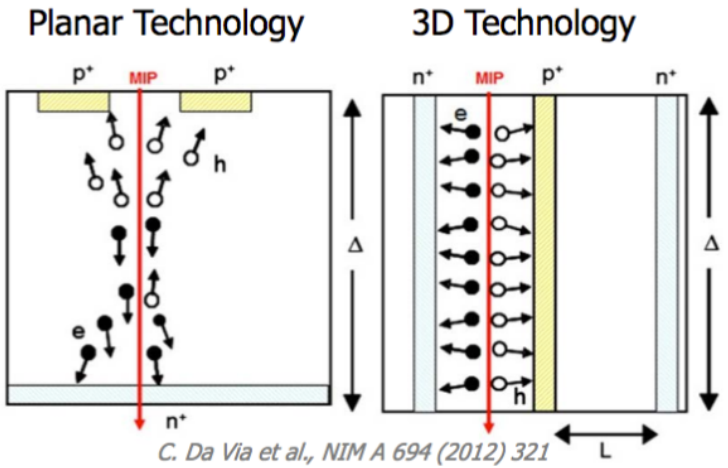
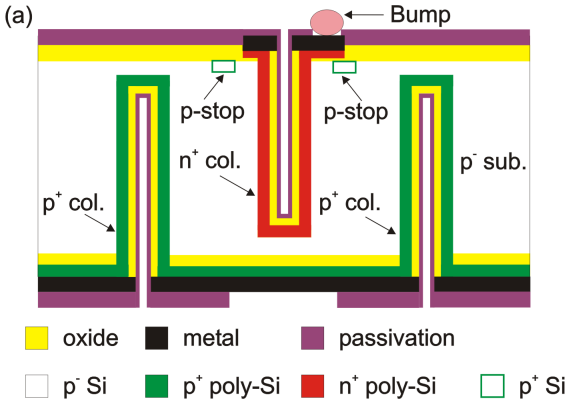
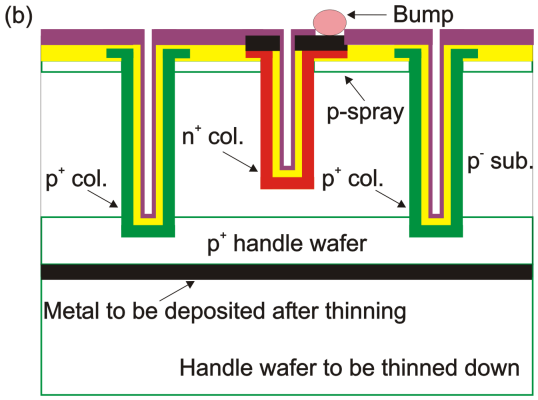


C. Da Via et al., NIM A 694 (2012) 321

3D sensors

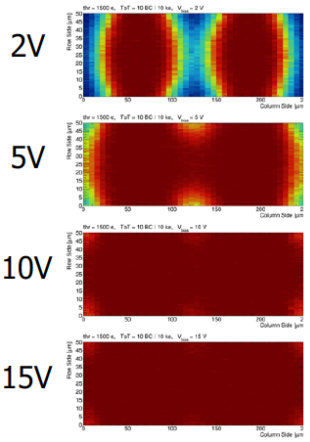
- Used in IBL (and in operation since 2015)
- More rad-hard (and less power hungry), but also higher C_{IN} and more complex production process (yield and less available firms)
- To increase yield a Single Side process has been studied and implemented, with very encouraging results

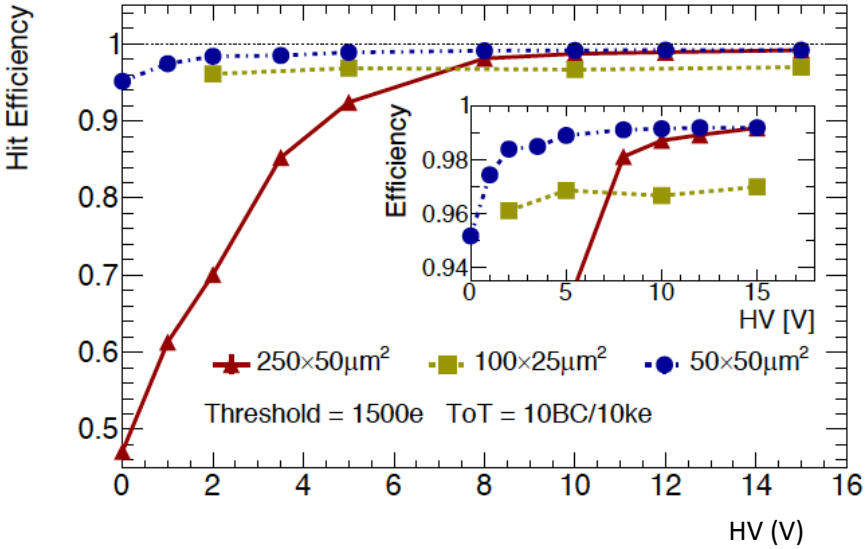




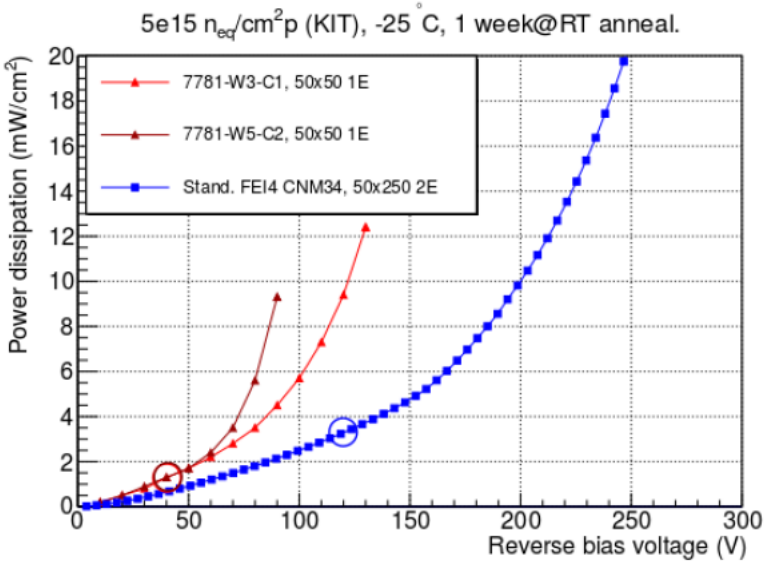
G.F. Dalla Betta et al. PoS (Vertex 2016) 028

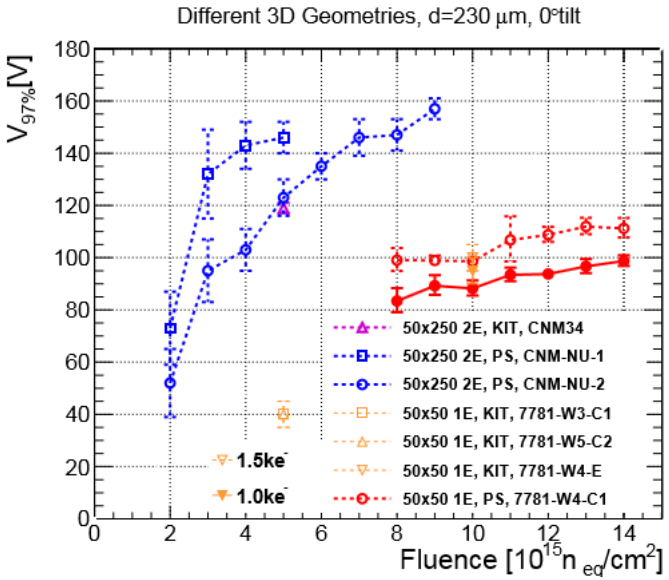
- Small (50x50μm²) pitch 3D ok before and after irrad. up to 1.4e16 n_{eq}/cm^2 (excellent detection efficiency and power dissipation)
- Better than 3D IBL generation (that used Double Side process)





Power dissipation 1.5mW/cm² @ 5 10^{15} n_{eq}/cm^2 (vs 3.5 mW/cm2 for IBL 3D)



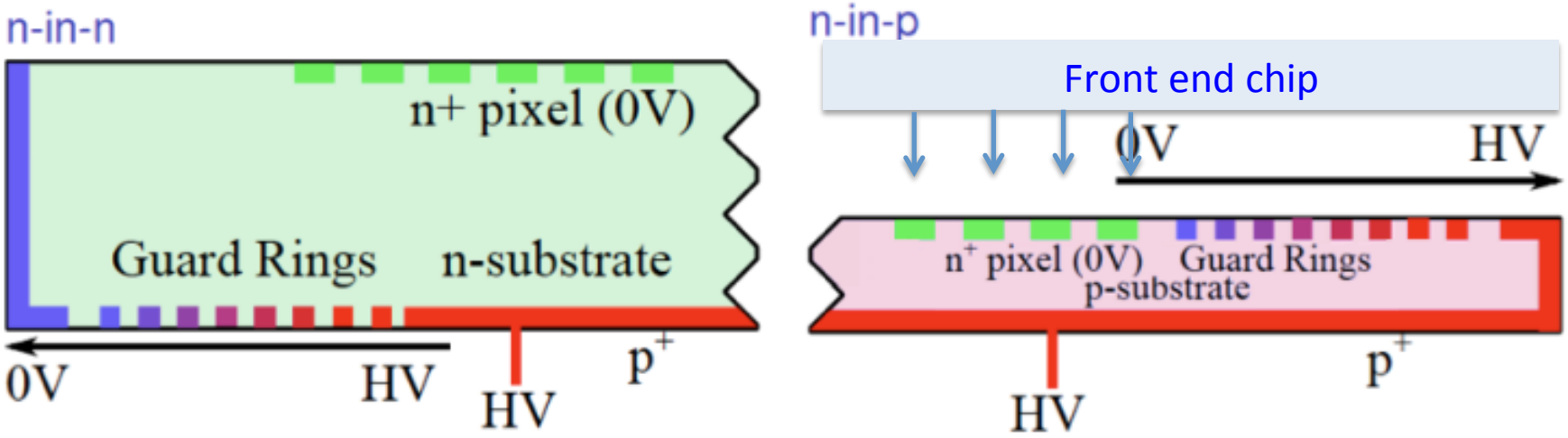


Beam test measurements of irradiated 3D pixel sensors with 50x50 μm² pixel size, D.Vasquez, Trento 2017

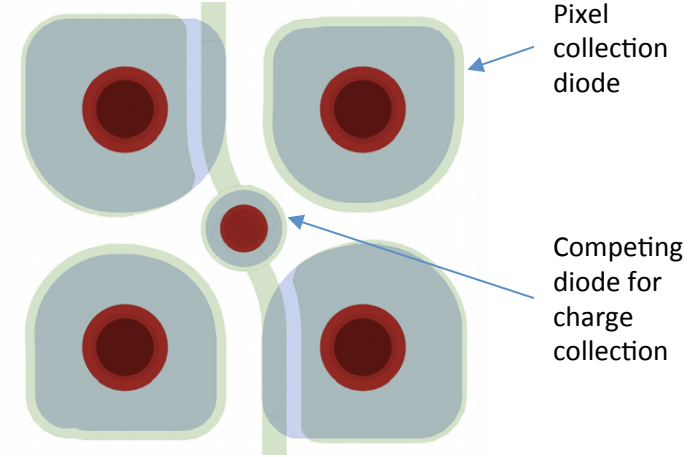
J. Lange, H. Oide presentations
G. Giugliarelli, G.Pellegrini posters

Planar sensors

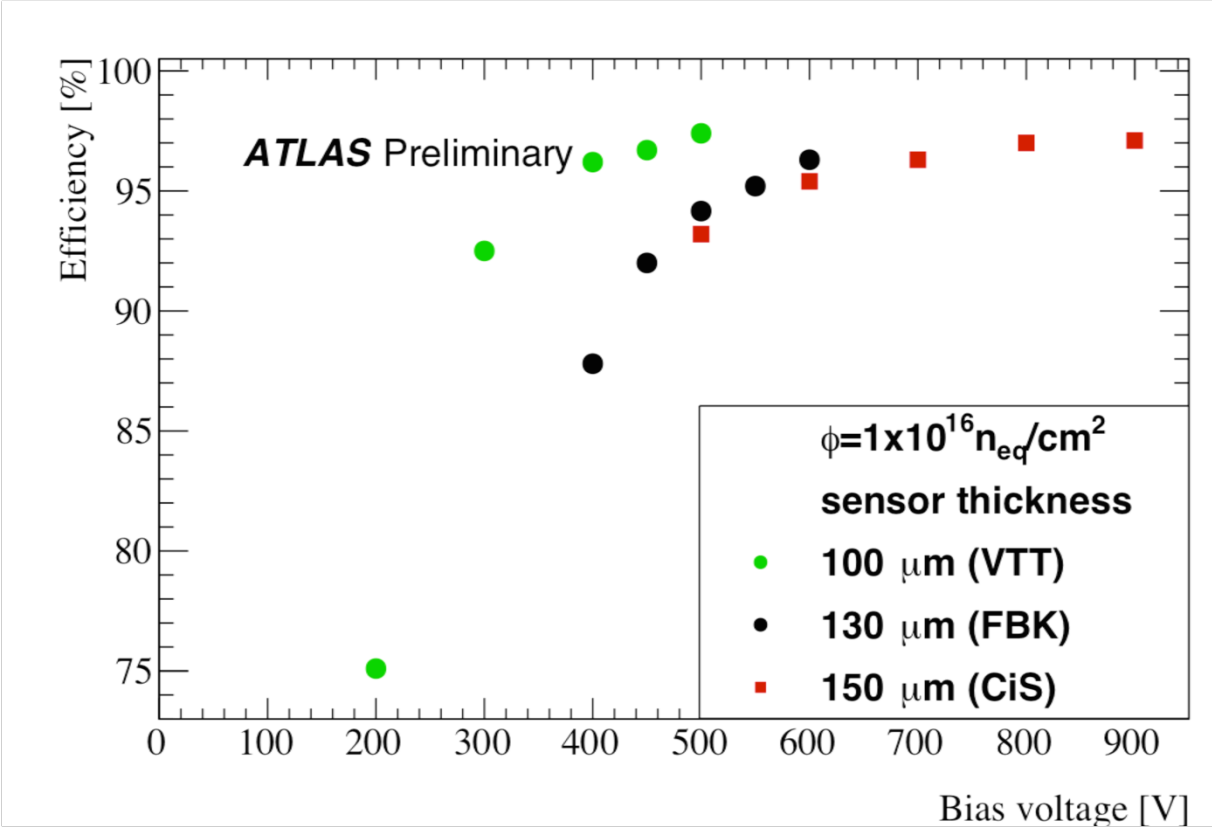
- Well proven and understood technique, but must simplify production to decrease cost (n-in-p = single sided process)



- Challenges:
  - HV insulator on sensor or chip needed (1000 V) → BCB coating
  - Thin detectors (≤150 μm) → low signal
  - A punch-through bias grid is necessary to select good sensors before hybridisation. This will result in a small and local inefficiency (especially after irradiation) → design optimisation (or sacrificial grid)



Pixel and Punch-Through structure design for 50x50 μm² pixels



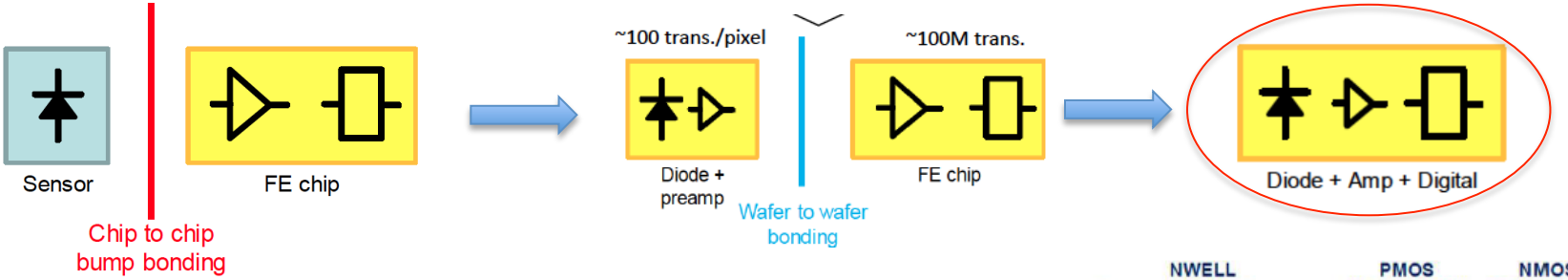
Test-beam activities and results for the ATLAS ITk pixel detector,
Tobias Bisanz at PSD11

- Hit efficiency for highly irradiated sensors (10^{16} MeV n_{eq}/cm^2) reaches 97%
- Thinner sensors require lower V_{bias}

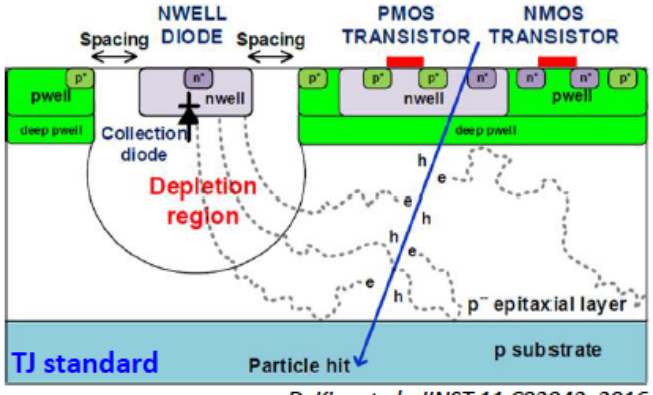
CMOS sensors

W. Snoeys, H. Pernegger, T. Hirono, I. Peric presentations M. Kiehn poster

- 3D and planar built on high-ρ Si and connected to FE electronics with high density BB. This technology is well known and optimisation of sensor and electronics can be done independently.
- But…need specialised foundries (high unit cost, low throughput 6" wafers) **and** BB
- CMOS foundries have much higher throughput (larger wafers) and became interested to medium-ρ Si (e.g. for automotive applications) & open to external designers → possible to implement sensors **and** circuits on the same substrate.

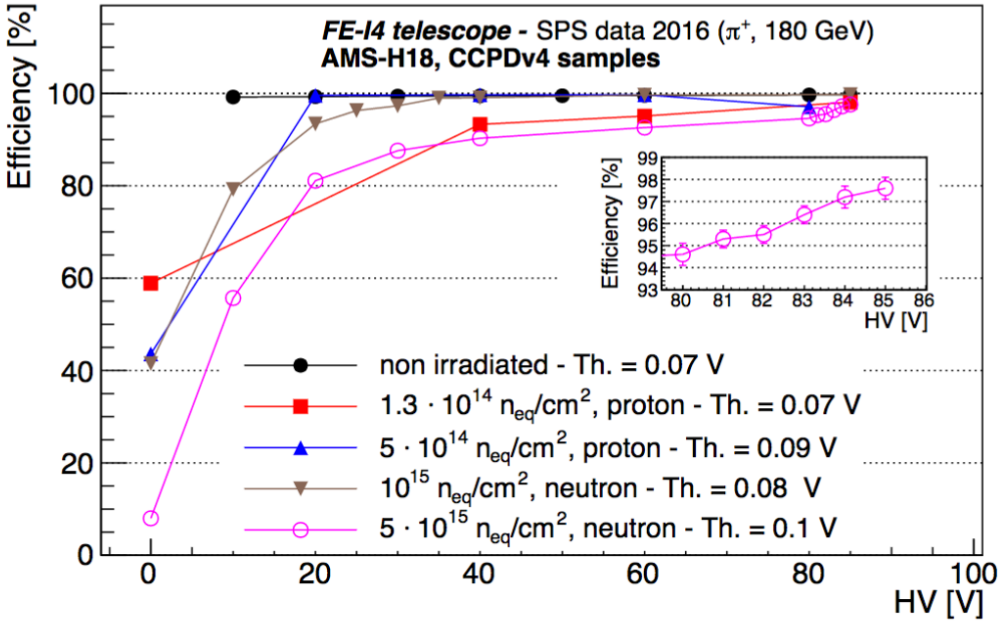


- E-field is weaker (charge collected by drift & diffusion) one may then worry about:
  - timing (can the detector be fast enough for LHC?)
  - Efficiency after irradiation (up to which dose can this device work?)

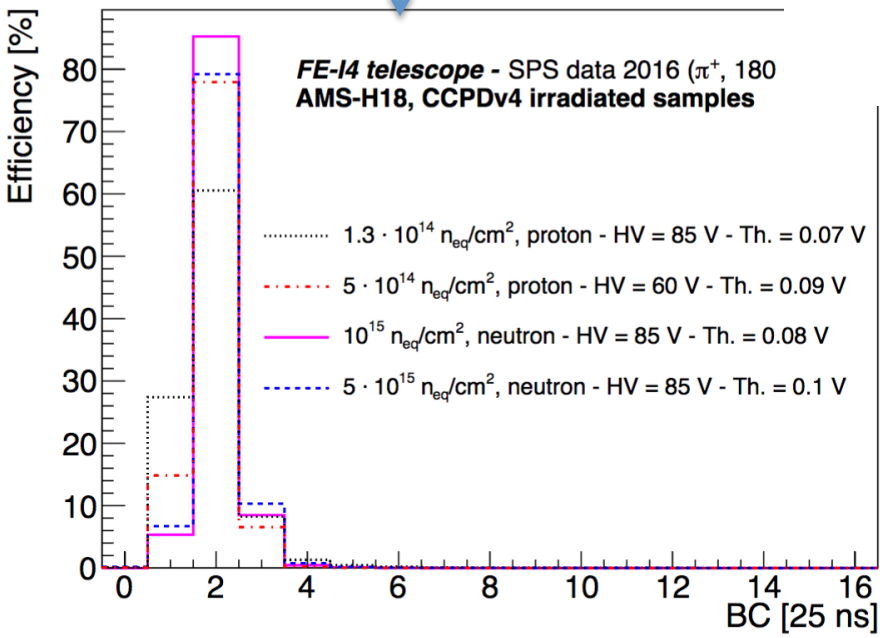


D. Kim et al., JINST 11 C02042, 2016

Efficiency after irradiation



Timing after irradiation



arXiv:1611.02669, M. Benoit et al.

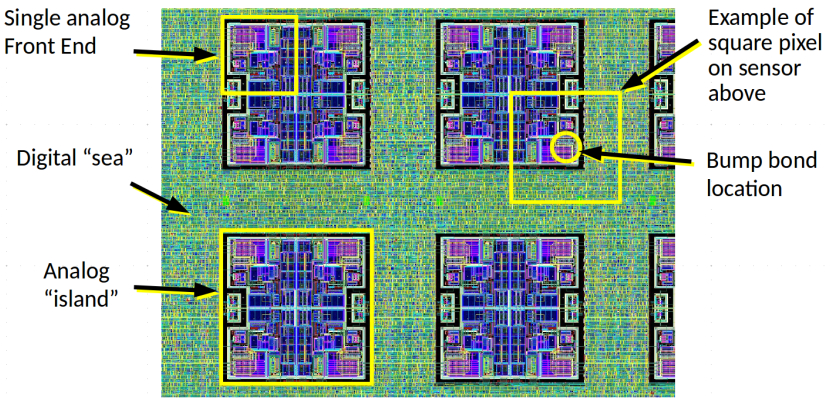
- The basics of CMOS for HL-LHC use (at large radius) is in hand
- Now see if a chip with full read-out architecture (and digital traffic) can be safely operated.
- If yes (and satisfactory) CMOS will be used for the external layer (with some gain of production time and some cost saving).

The FE electronics

- Synergic development with CMS (RD53) to design FE Pixel ASIC for HL-LHC. The first prototype chip has just been delivered (under test now!).

- Main characteristics:
  - Increased radiation hardness using 65nm technology in TSMC
  - First time using a fully synthetized digital part in a ”sea of digital”
  - Smallest pitch for hybrid LHC application so far , 50x50um^2 (possibility for 25x100μm^2)
  - Shunt LDO implemented for compatibility with Serial Powering
  - Highest data rate achievable per ASIC : 5Gbps
- Now tests on wafer and (if ok) with sensors
- Next iteration: each experiment will tailor to its own specs and extend to full size (now ~50%).

Technology	65nm CMOS
Pixel size	**50x50 um^2**
Pixels	192x400 = 76800 (50% of production chip)
Detector capacitance	< 100fF (200fF for edge pixels)
Detector leakage	< 10nA (20nA for edge pixels)
Detection threshold	<600e-
In -time threshold	<1200e-
Noise hits	< 10^{-6}
Hit rate	**< 3GHz/cm^2 (75 kHz avg. pixel hit rate)**
Trigger rate	Max 1MHz
Digital buffer	12.5 us
Hit loss at max hit rate (in-pixel pile-up)	≤1%
Charge resolution	≥ 4 bits ToT (Time over Threshold)
Readout data rate	**1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s**
Radiation tolerance	**500Mrad at -15°C**
SEU affecting whole chip	< 0.05 /hr/chip at 1.5GHz/cm^2 particle flux
Power consumption at max hit/trigger rate	**< 1W/cm^2 including SLDO losses**
Pixel analog/digital current	4uA/4uA
Temperature range	-40°C ÷ 40°C

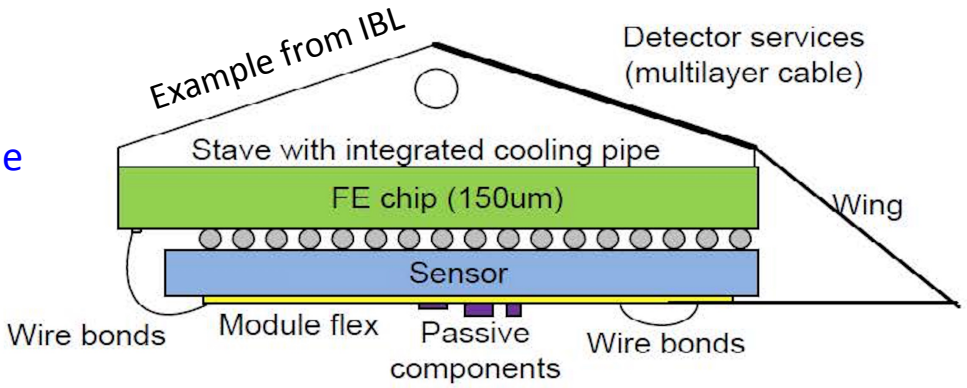


more in M. Garcia-Sciveres talk

The Module

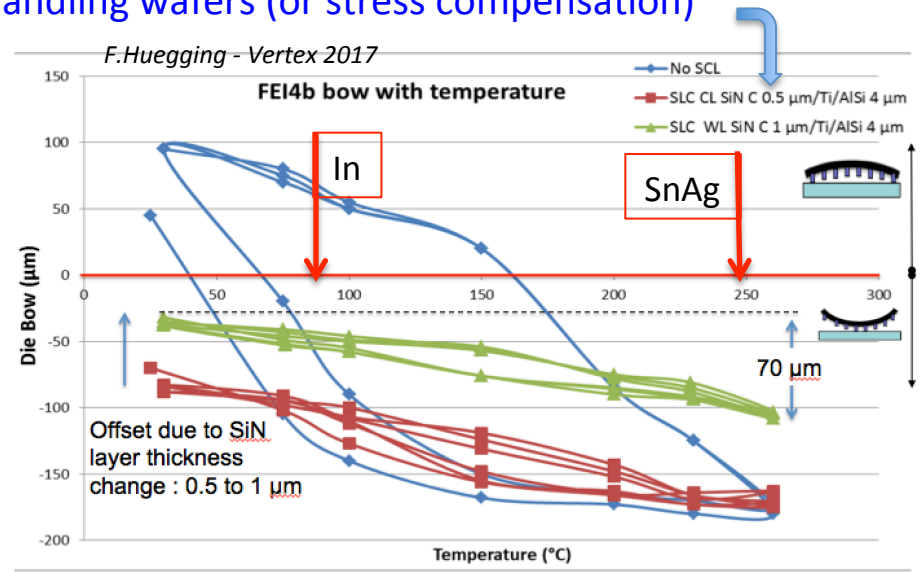
C. Buttar poster

- Sensors and mating FE electronics are joined through high density vertical connectivity (bump-bonding)→ bare module
- Module (basic building block, replicated many times to cover the detector surface) requires dressing with flex circuits for I/O



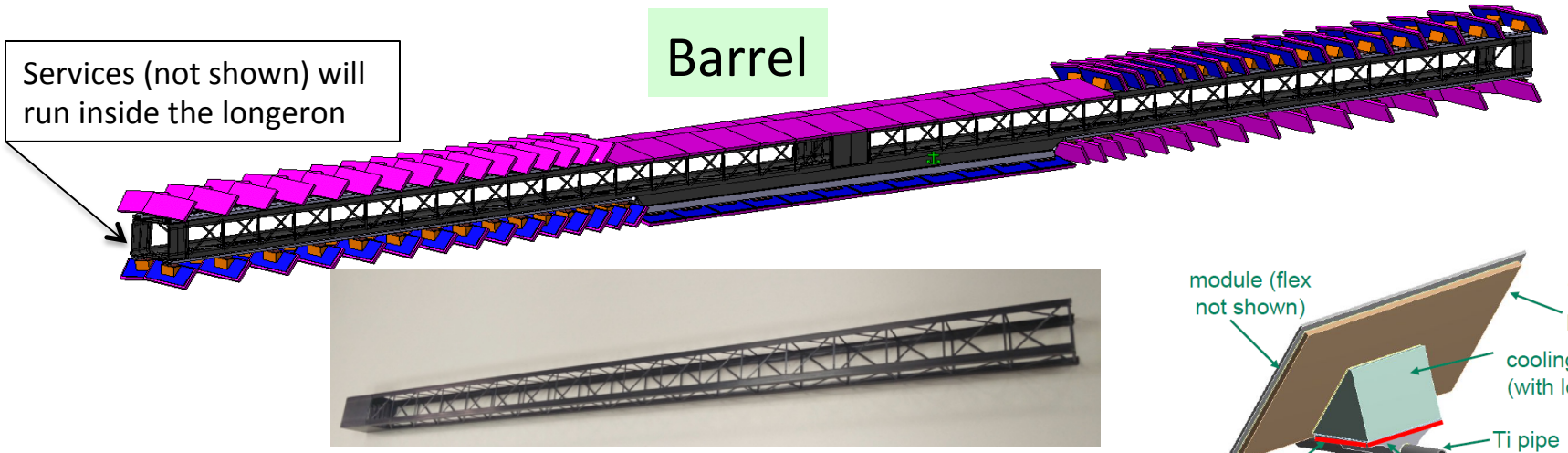
- For yield reasons 3D modules will be with 1 FE only, while planar with 4 FE (or 2).
- High-density bump-bonding (50x250μm²) routinely done (in few firms), but now:
  - 50x50 μm² pixels, same pitch as before but 5xdensity → just try…
  - Larger ASIC wafer size (12") → start with daisy chain dummy wafers to qualify firms
  - Thinner ASIC and Sensors (<150 um) →handling wafers (or stress compensation)

- Effort ongoing (now to 2019) to qualify 4 to 5 firms for BB production (needed for the large area of ITk Pixel; 12k modules in 2 years = 50 modules/week)
- Also considering to complement flip-chip "power" with in-house capability



The Mechanical Supports and Services

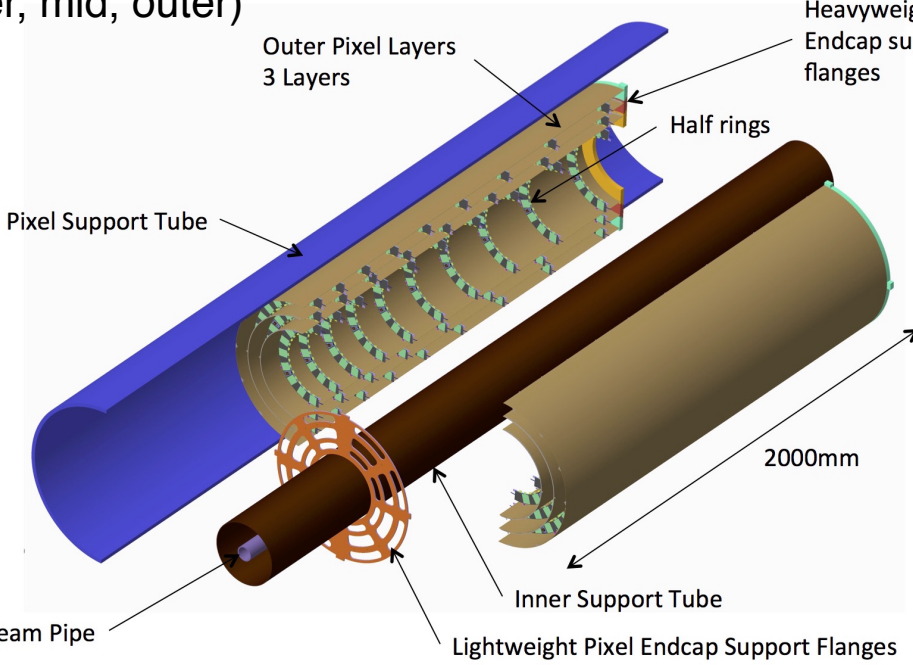
- Mechanics and services have been optimized for better coverage and lower material budget.
- Inclined layout preferred vs extended (better track reco for mid&low p)

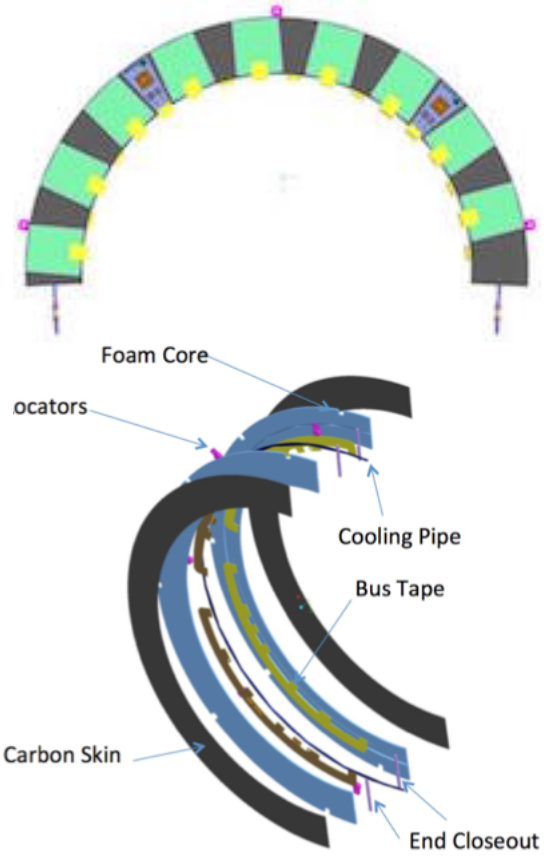


- Flat section in the middle part of the very long barrel
- Inclined modules mounted on pyrolitic graphite plate (PGP)
- connected to cooling pipe via high thermal conductivity cooling block (e.g. graphite)
- Inner layers could have slightly different support design (see later)

End-cap

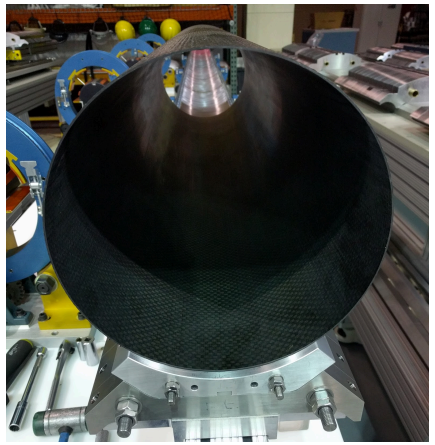
- Coverage (up to η=4) obtained with many disks with (partially overlapping) modules on both sides. Rings supported by CRF half shells.
- 1 measurement "plane" made of 3 z-displaced rings (inner, mid, outer)



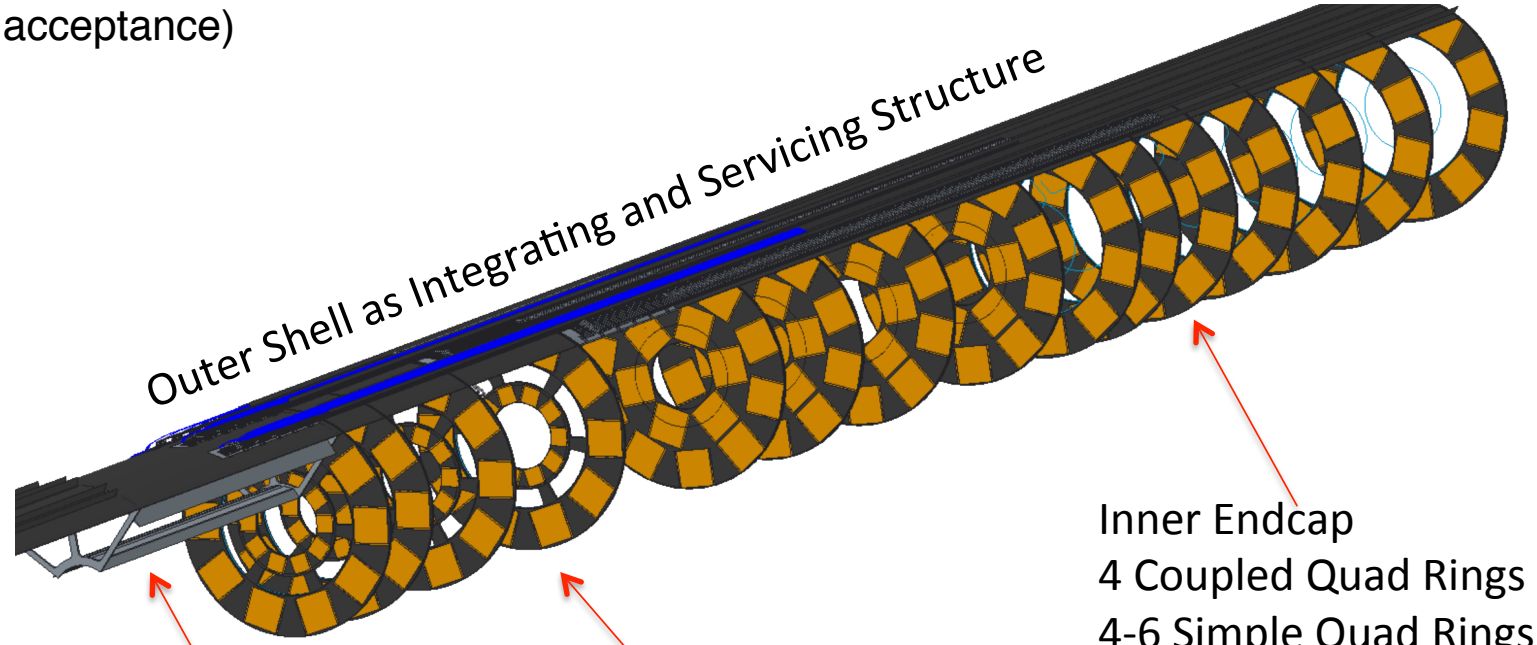


- Cooling pipe (and power lines) running inside a thermally conductive carbon foam sandwiched between two carbon fibre rings

The innermost insertable layers



- Must slide-in inside a carbon fibre shell (prototype here→)
- Inner layout contains a (short) barrel part and many small rings (some covering the barrel acceptance and some the EC acceptance)



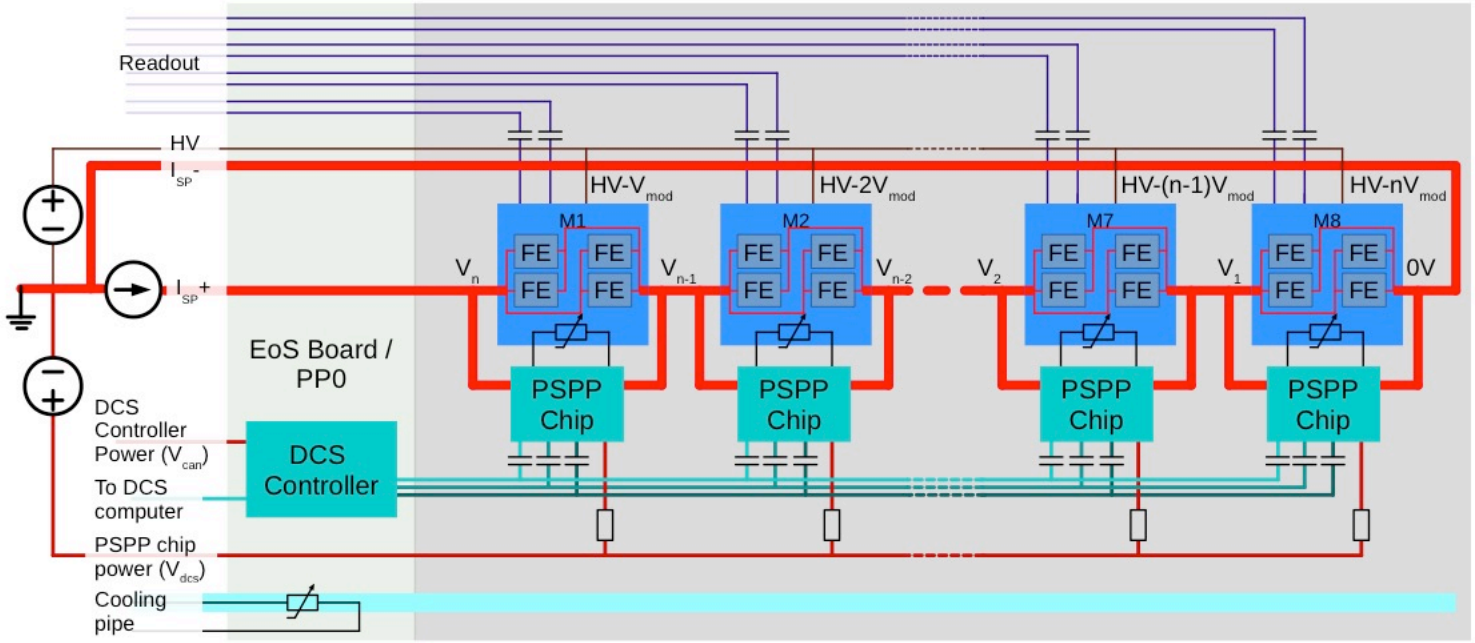
Inner Endcap
4 Coupled Quad Rings
4-6 Simple Quad Rings

Barrel Rings
16 Layer0/Layer1 Coupled Rings
(1/4 shown here for clarity)

Barrel
16 Layer0 Staves
20 Layer1 Staves

Serial Powering

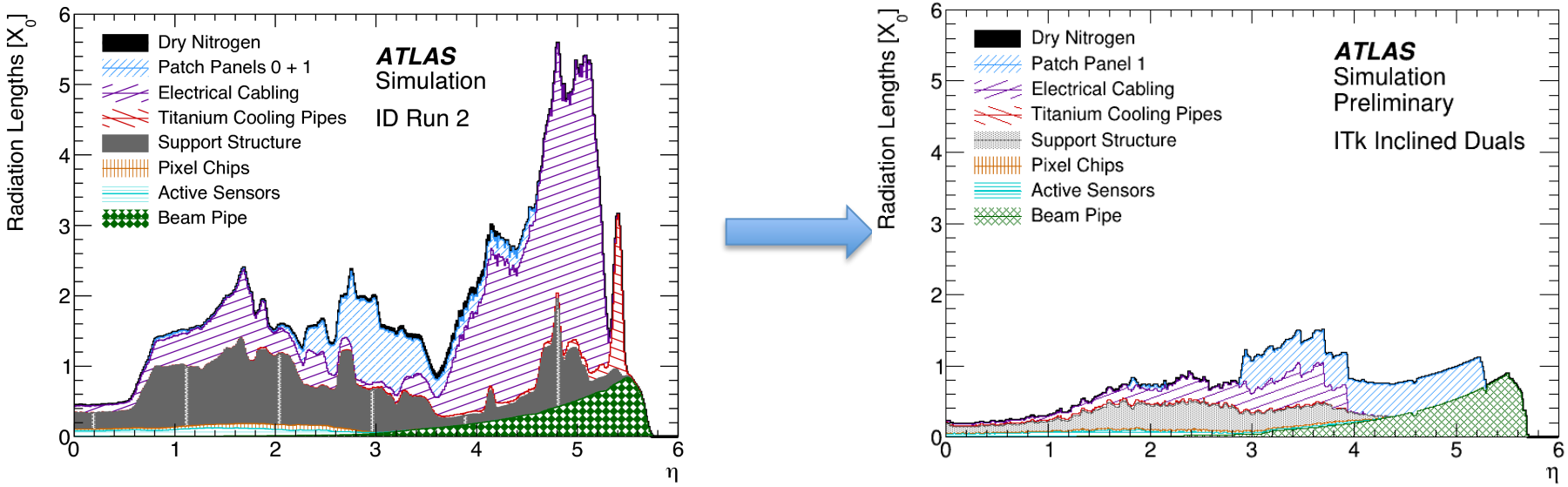
- Crucial to minimize the amount of material (one cable instead of 12 or 16)



- DCS functionality integrated in the system
  - PSPP chip: monitor and control of module (bypassing)
  - Independent DCS power and communication lines
  - Test results on a prototype made of 6 FEI4 quad modules (3 with bypass chip) show no degradation of threshold or noise (vs parallel powering of the same setup) → good, but more tests needed to reach the desired modularity (and fail safe operation).

Material budget

- All the design choices (thin sensors & electronics, use of CO2 evaporative cooling, use of serial powering, etc.) greatly reduced the material budget in the acceptance region (compared to the current Pixel detector that has one layer less).
- …and even more in the forward region up to $\eta<5.5$
- most of the gain comes from cables (i.e. serial powering)

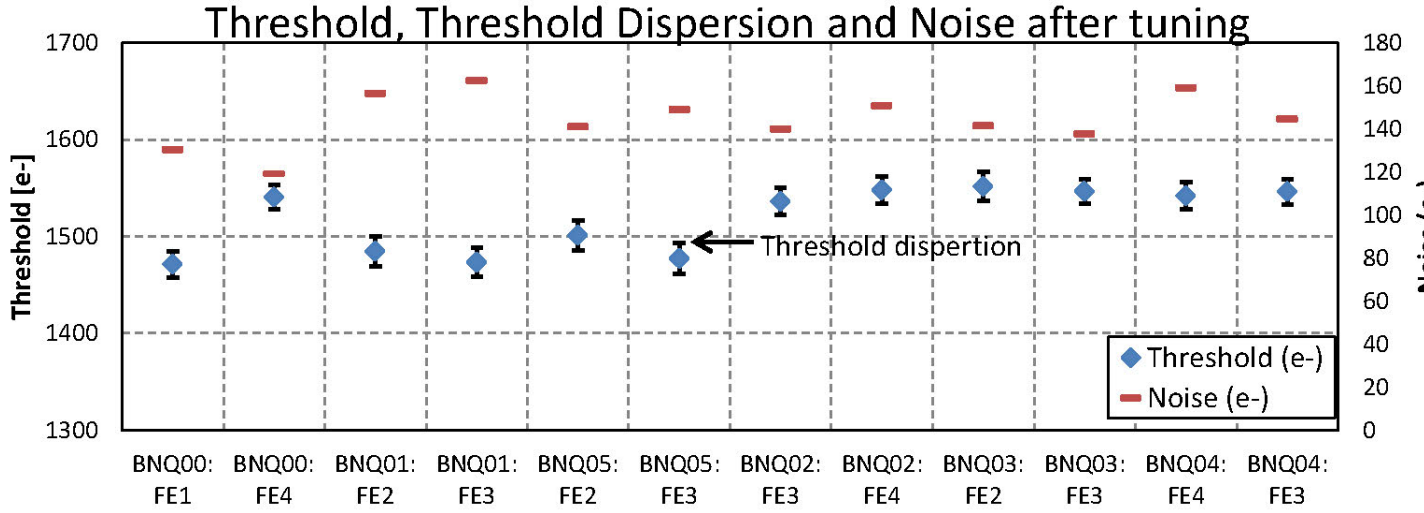


- …now we just have to maintain the promises (it is well known that trackers tend to put on some weight during construction)

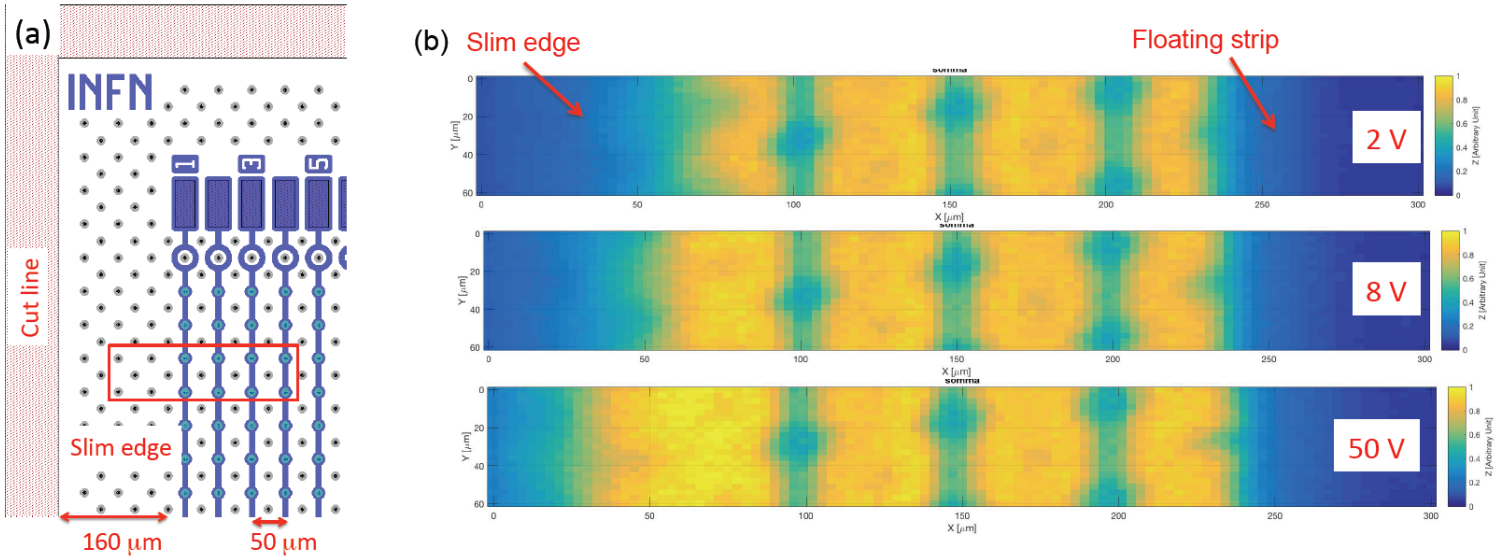
Concluding remarks

- All the basic techniques for the project are understood and available in the collaboration and in the industrial environment.
- Many refinements are needed, some of which are critical for the timely success of the project (e.g. serial powering, bump-bonding, FE chip, etc.)
- The production plan is quite constrained and will require careful optimization (& standardization over 100 labs) and flexibility to react to problems.
- The ATLAS ITk Pixel collaboration is going to submit its TDR to the LHCC next week.
- Ready to jump…

Additional information



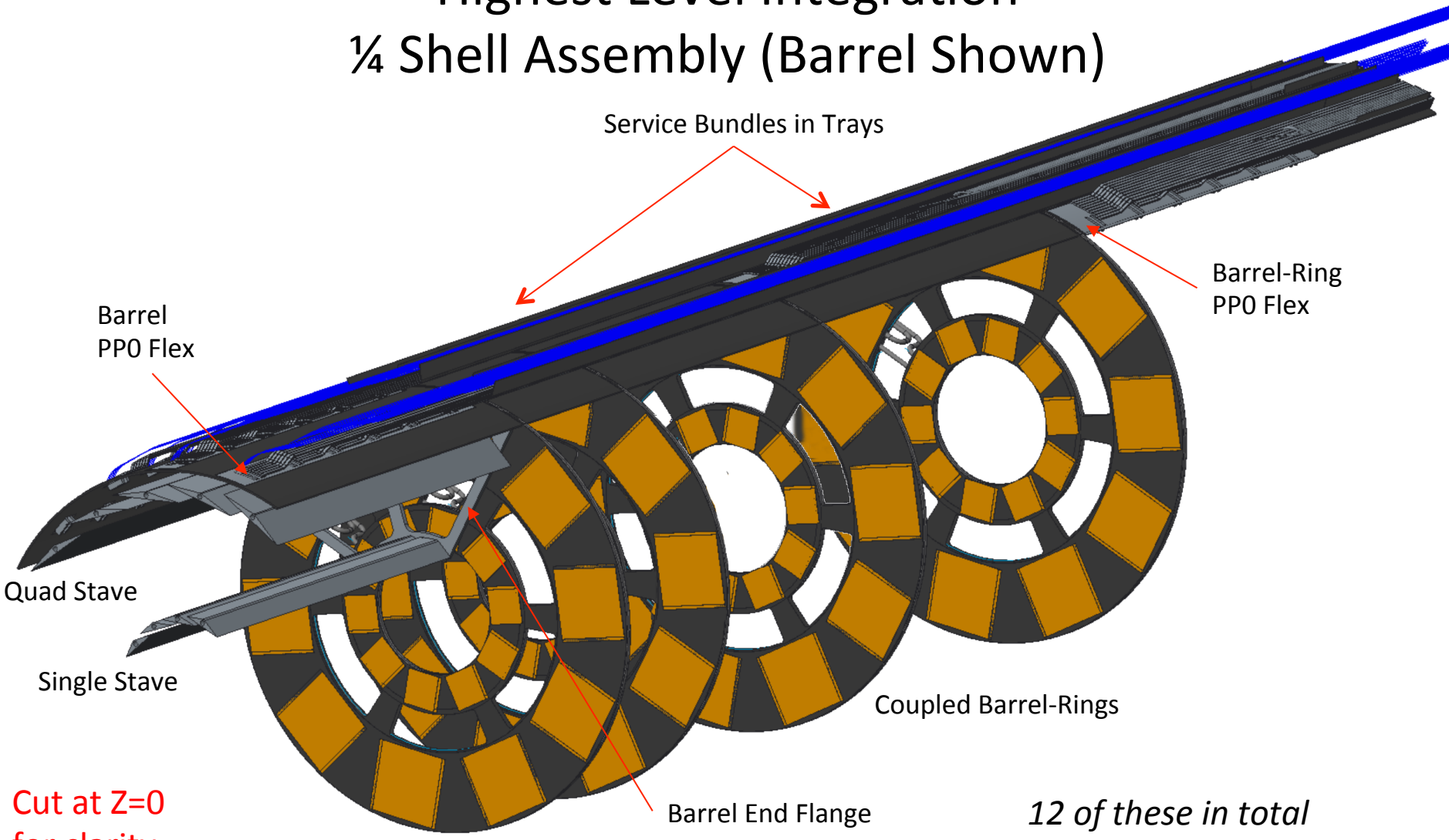
Serial Power



SS 3D

Figure 5 (a) Layout detail of 3D strip sensor of 50×50 μm² elementary cell layout (the red rectangle indicates the region of interest for the laser scan), and (b) maps of measured signals at three different bias voltage (2, 8, and 50 V).

Highest Level Integration
¼ Shell Assembly (Barrel Shown)

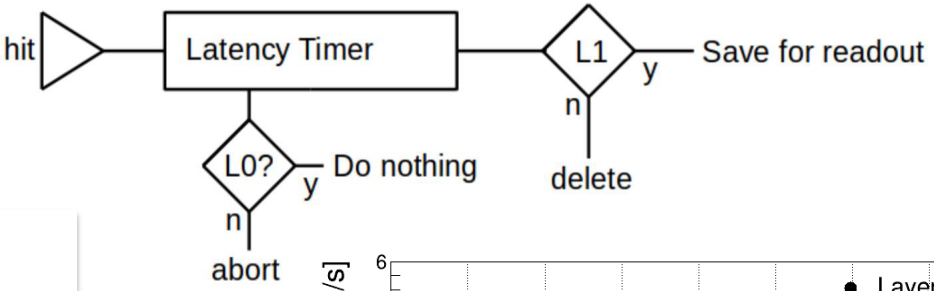


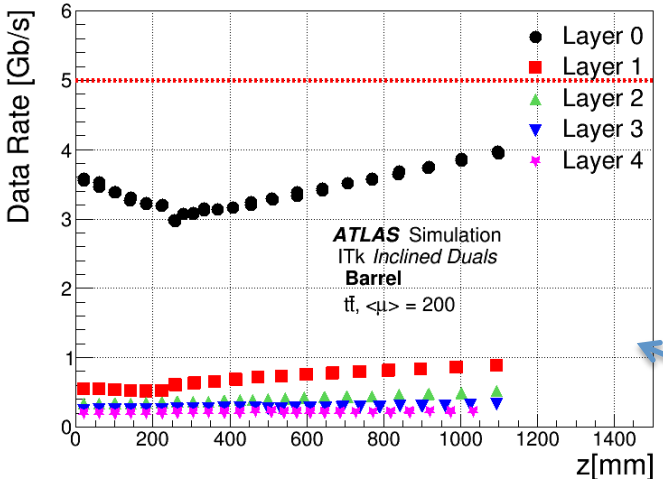
Cut at Z=0
for clarity

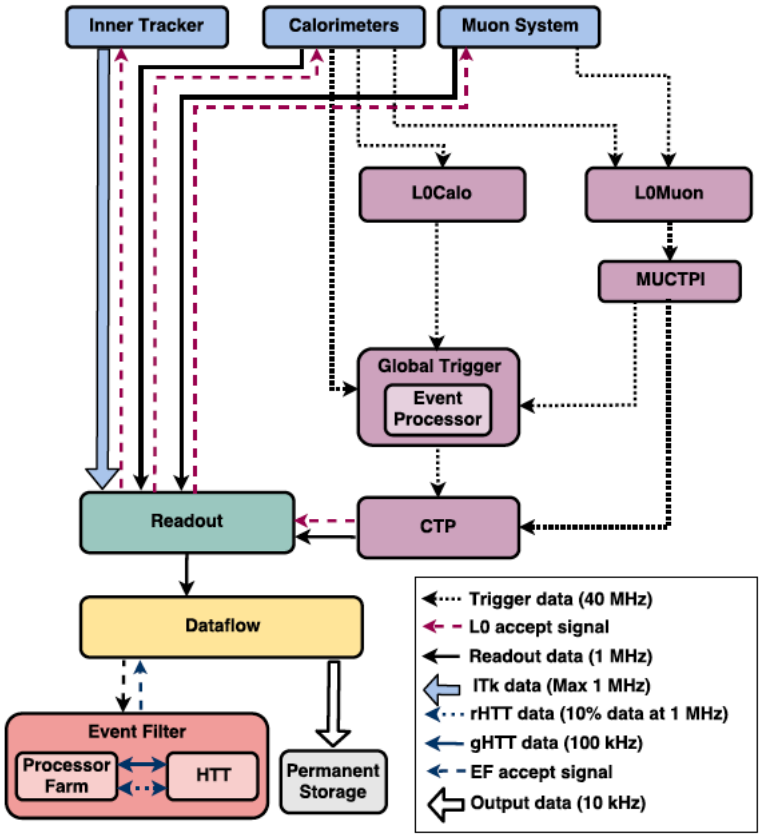
12 of these in total

Read-out &Trigger

- 1 MHz read-out and up to 35μs data latency (alternative is partial 4 MHz read-out @L0 trigger and 800 kHz full read-out @L1)
- 4 MHz L0 sustainable only from outer ITk pixel layers.







L0 [L1] trigger latency 10 [35] μs

Average data rate in barrel layers
Layer 0 is critical