Development of a far-infrared image sensor with Si-supported Ge BIB detector and FD-SOI cryo-CMOS ROIC hybridized by nano-particle deposition Au-bump

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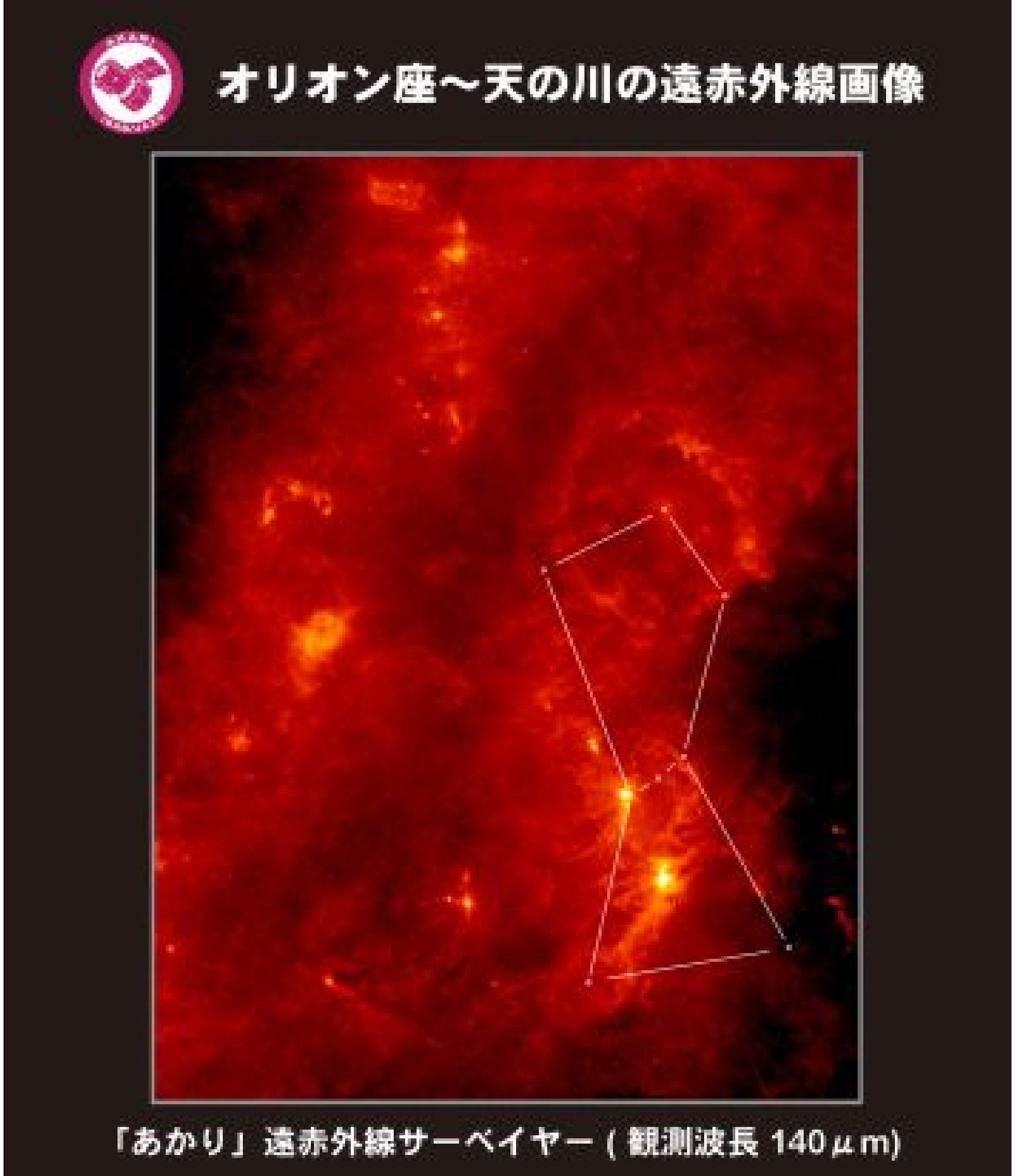
- Far-infrared (FIR) astronomy
- Detector and readout integrated circuit (ROIC) technology used for FIR astronomy
- Germanium Blocked impurity band (BIB) detector
- Fully depleted silicon on insulator (FD-SOI) CMOS cryo-ROIC
- Si-supported detector structure and NpD Au bump

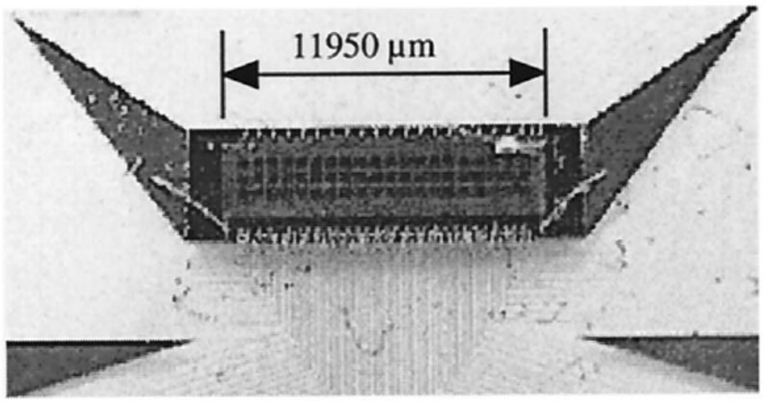


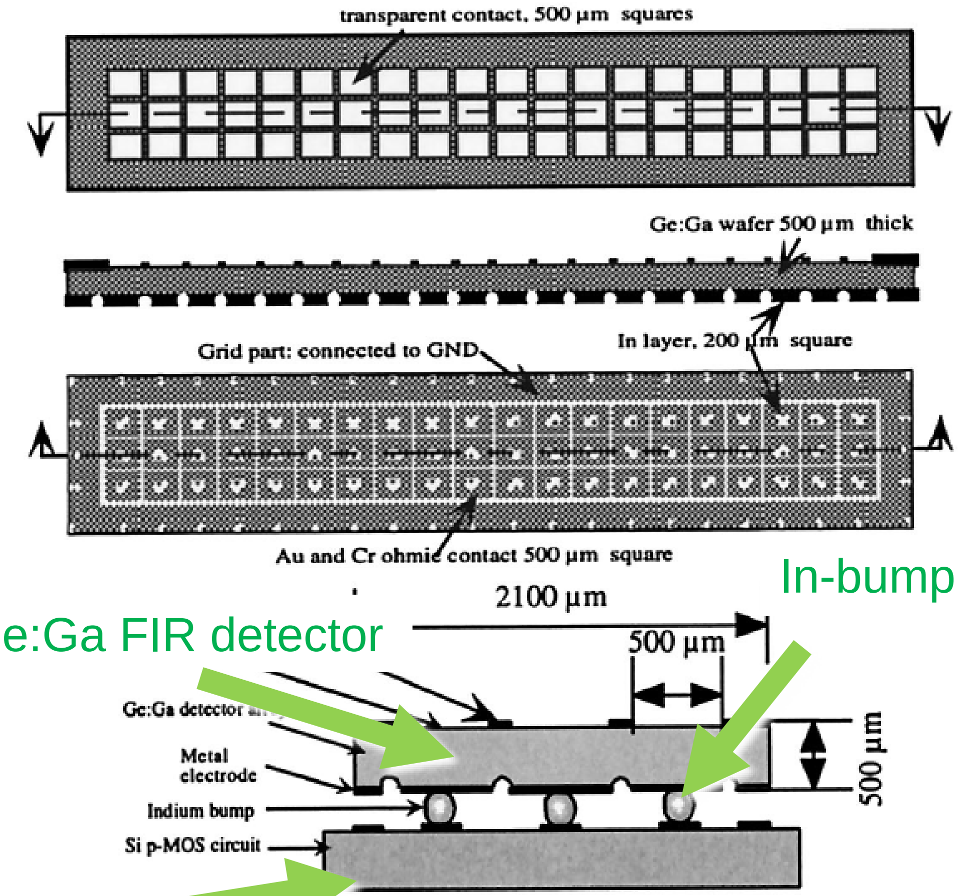
- FIR (140um) image of Orion star-forming region.
- Taken by the Japanese first infrared astronomical satellite AKARI (2006)

Far-infrared astronomy

- Strong tool for investigation of birth and evolution of planets, stars and galaxies
- Strong UV-to-OPTICAL light from young bright stars and active galactic nuclei (AGNs) is absorbed by inter-stellar dust.
- The energy is re-emitted in the FIR (30-200 μm)
- Approximately 50% energy is emitted in the FIR.

FIR image sensor in AKARI era





Fujiwara et al. 2003, Appl. Opt. 42, 2166

In AKARI , the world first FIR image sensor chip 3x20 Ge:Ga photo-conductor (PC) array hybridized with PMOS cryo-ROIC by In-bump is used

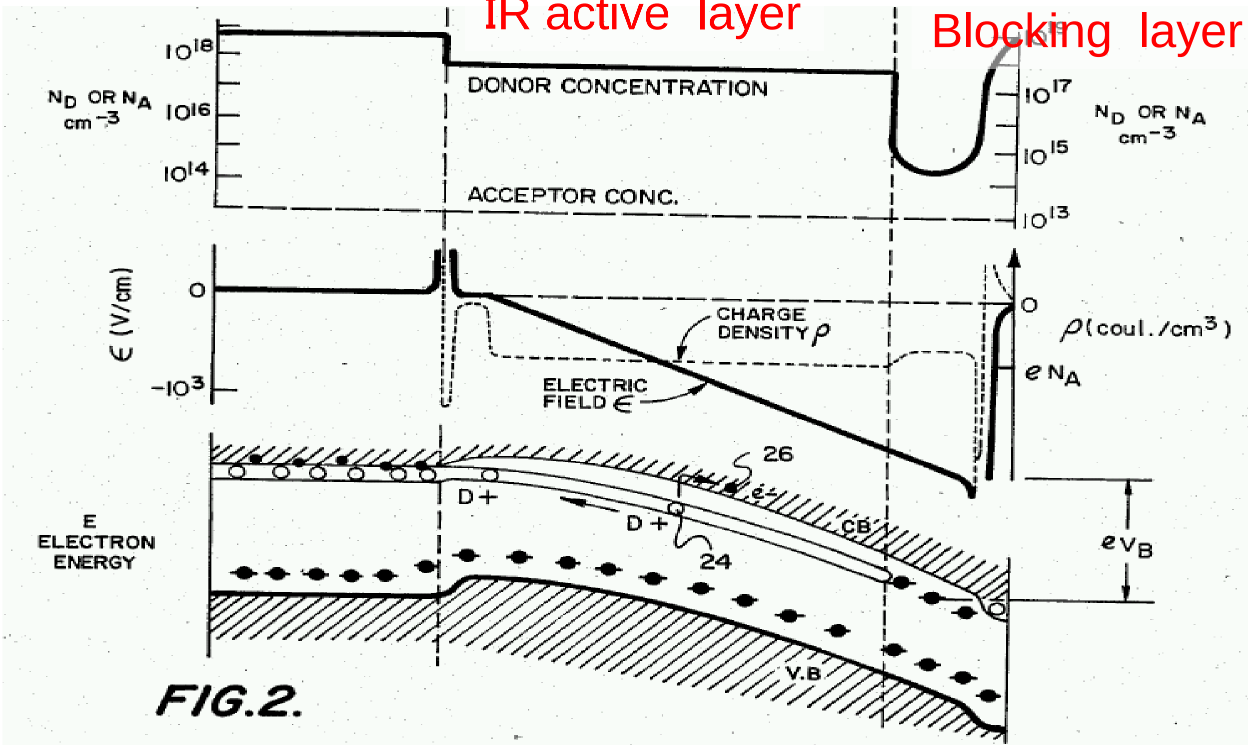
Problems on the previous IR image sensors

- Ge:Ga PC is not sensitive beyond 120 μm.
  - we have overcome it by detector with BIB structure which is sensitive up to 240 μm.
- PMOS ROIC consumes too much power (10 μW/pix)
  - We have overcome it by FD-SOI CMOS ROIC (1 μW/pix), which enables 1K pix array with 1mW at 2 K.
- Large coefficient of thermal expansion (CTE) mismatch between Ge detector and Si ROIC destroys the In-bump inter-connection.
  - We have overcome it by Si-supported structure and Nano-particle deposition (NpD) Au bump

Blocked impurity band (BIB) detector

highly-doped
IR active layer

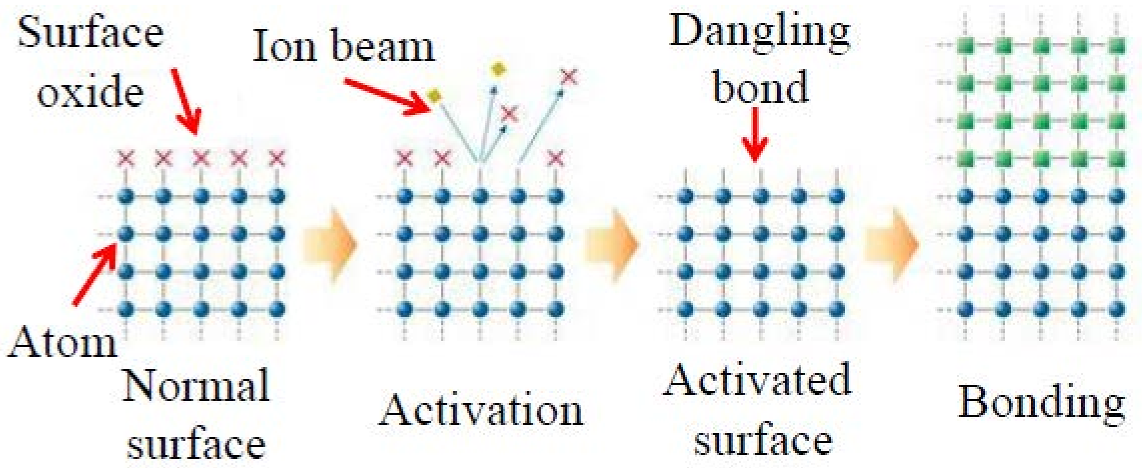
Non-doped
Blocking layer



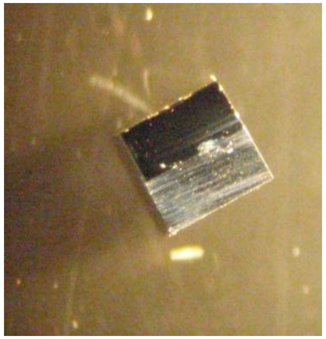
Petroff and Stapelbroek 1986, US patent 4568960

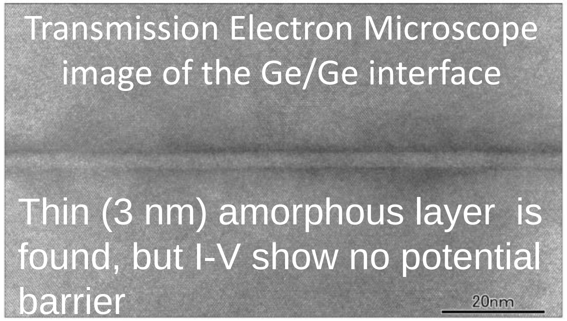
- Higher doping (~10^{16}/cc)
  - Higher QE
- Formation of impurity band
  - Reduce the band gap
  - Longer wavelength cut-off
- Non-doped layer (<10^{14}/cc)
  - Block dark current by IBC

Surface activate bonding (SAB)



https://www.mhiglobal.com/products/detail/wafer_bonding_machine.html





Watanabe et al. 2011, JJAP 50, 015701

The Ge/Ge bonding was done by Mitsubishi heavy industry.

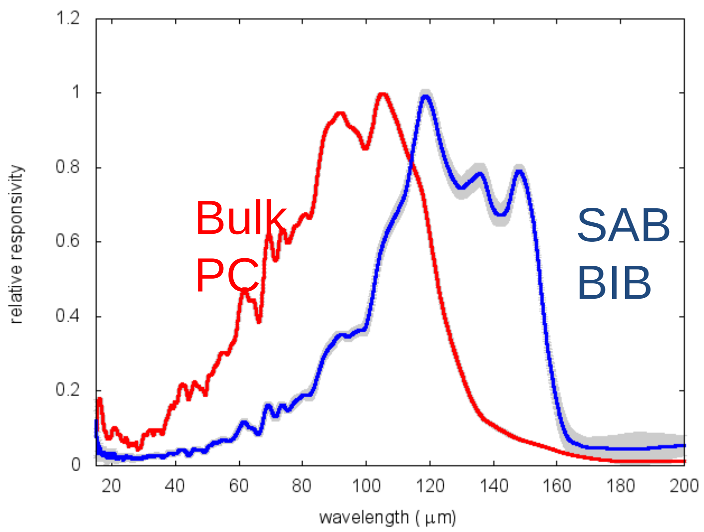
The problem is how to realize the BIB detectors with high quality crystal and large contrast in impurity concentration.

This is done by Surface activate bonding (SAB). SAB is a room temperature bonding technique in ultra-high vacuum condition.

The SAB process has a large advantage:
We can choose the best wafers both for the IR-active layer and the blocking layer.

Performance of our BIB device by SAB

Spectral response of a device with Ga concentration of 1×10^{16}/cc



Cut-off wavelength extension to 240 µm is observed for a device with Ga concentration of 8×10^{16}/cc

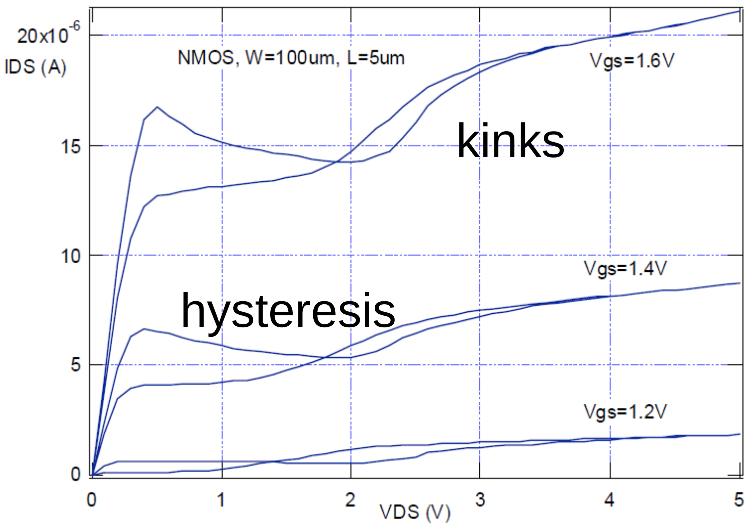
Hanaoka, Wada et al. 2016

- Responsivity: 1.5 A/W
  - QE 1%
  - A factor of 10 improvement can be achieved if we remove non-sensitive area.
- Dark current: non-detection (<5fA/mm^2)
  - Huge reduction compared with that of without blocking layer (10 nA/mm^2).
  - The blocking layer actually reduce the hopping dark current.
- NEP of $<2 \times 10^{-17}$ W/sqrt(Hz)
  - 2×10^{-19}W/sqrt(Hz) can be achieved if we remove non-sensitive area and reduce the detector area down to 0.1 mm x 0.1 mm.

FD-SOI CMOS ROIC for cryogenic operation

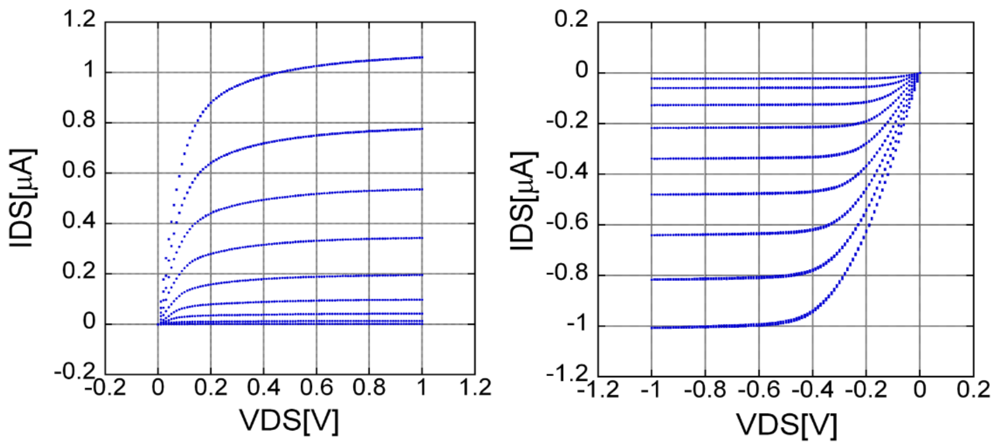
Nagase et al. P-34

I-V curve of n-ch MOSFET used for Herschel.



Merken et al. 2004, SPIE 5498, 622

I-V curve of FD-SOI MOSFET used for This work

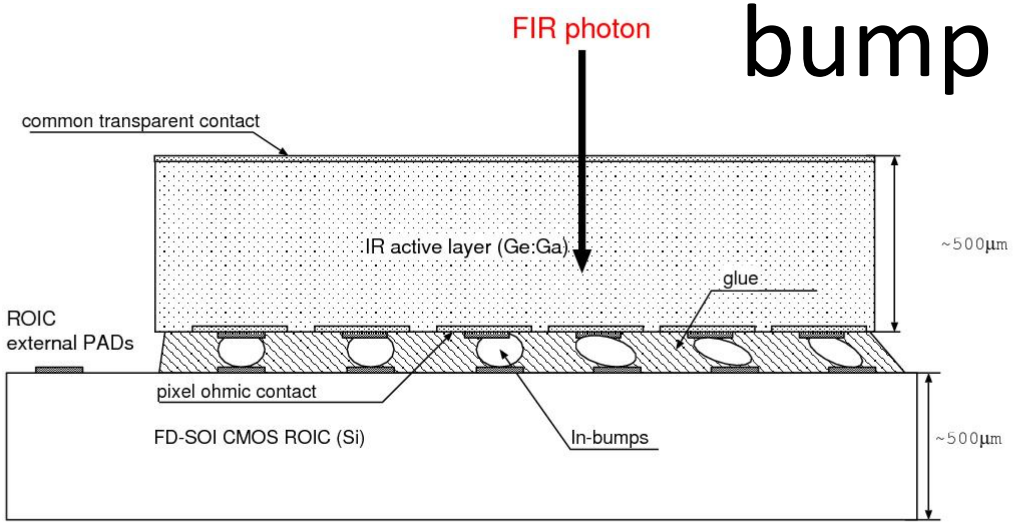


(Nagata, Wada et al. 2009

The previous ROIC does not have a good performance because the conventional MOSFETs, especially NMOS, suffer from kinks and hysteresis at cryogenic temperature.

We found FD-SOI MOSFETs show no kink and hysteresis both for NMOS and PMOS, and succeed to fabricate CMOS CTIA ROIC with 1μW/pix power consumption.

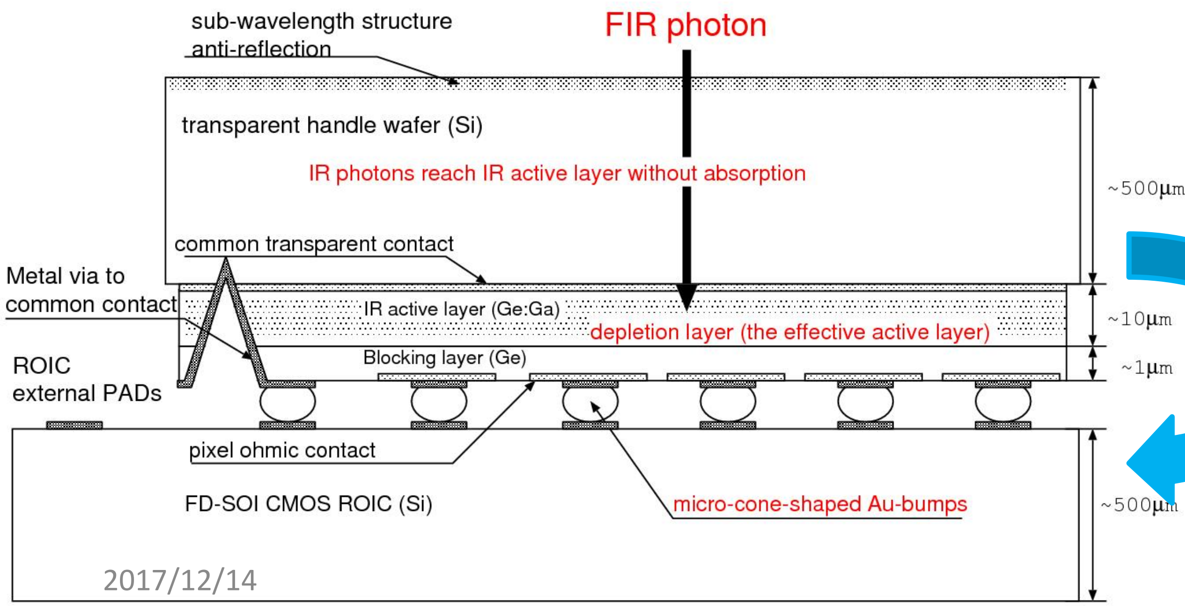
Si supported Ge detector and Au-bump



Large thermal expansion mismatch between Ge detector and Si ROIC.

CTE for Si : $2.6 \times 10^{-6}\ K^{-1}$

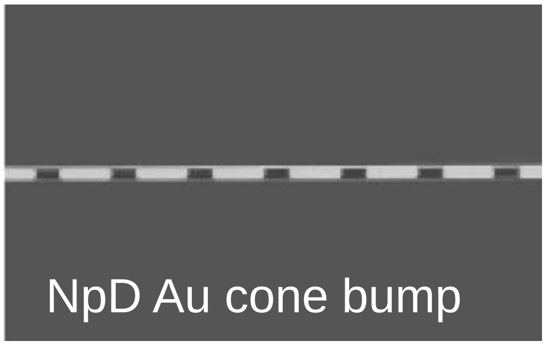
CTE for Ge : $5.8 \times 10^{-6}\ K^{-1}$

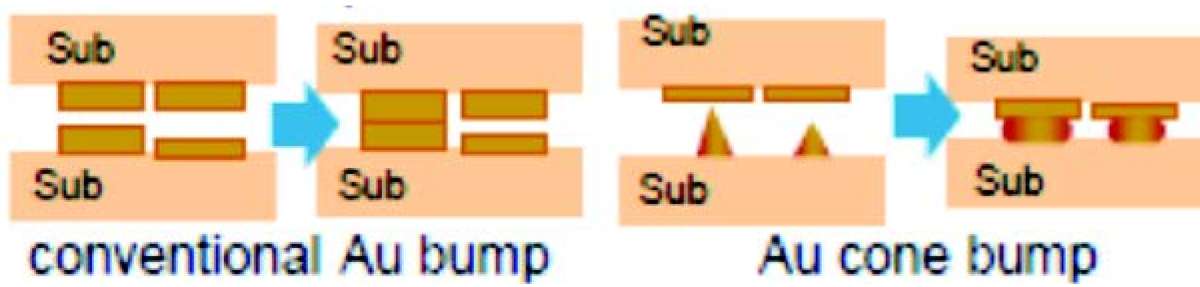


In order to reduce thermal expansion mismatch between Ge detector and Si ROIC, we employ Si wafer to support the Ge detector. The Ge detector and the Si wafer are bonded by SAB.

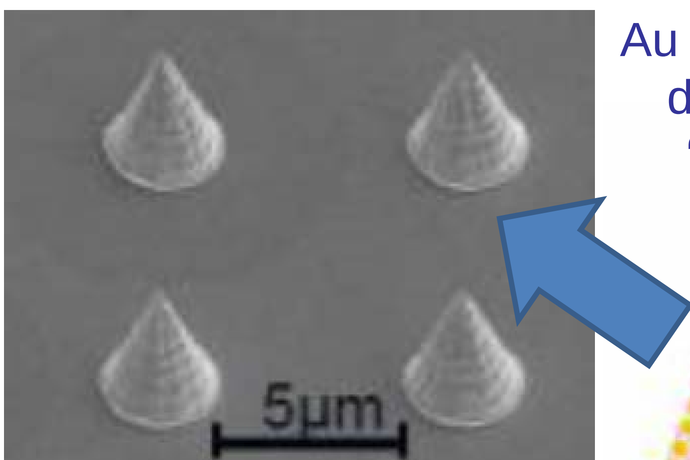
The mismatch between the detector and ROIC is reduced by a factor of 100, considering Young's constant (103 and 185 GPa) and thickness (10 μm and 500 μm) of Ge detector and Si support.

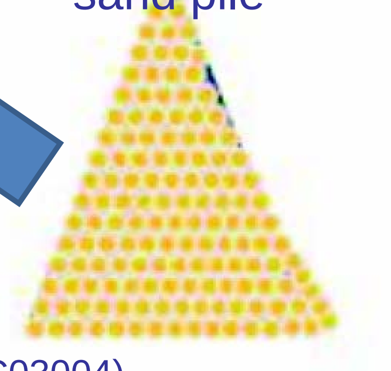
Hybridization Au cone bump fabricated by nano-particle deposition (NpD)





Cone bump fabricated by Au Nano-particle deposition -- “sand pile”





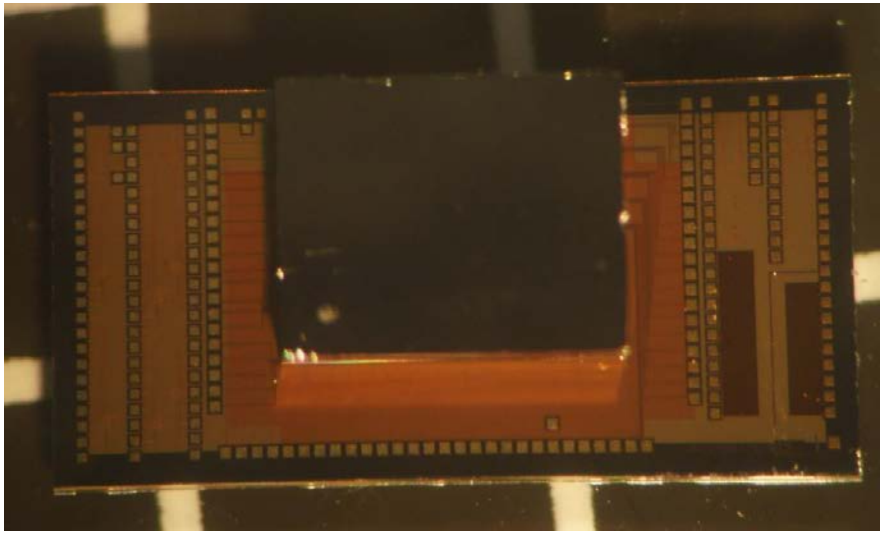
Hybridization has been done by Au cone bump fabricated by nano-particle deposition (NpD).

NpD bump is easy to deform and have large margin in height. During the hybridization, the NpD Au bump becomes bulk Au bump and recover the stiffness.

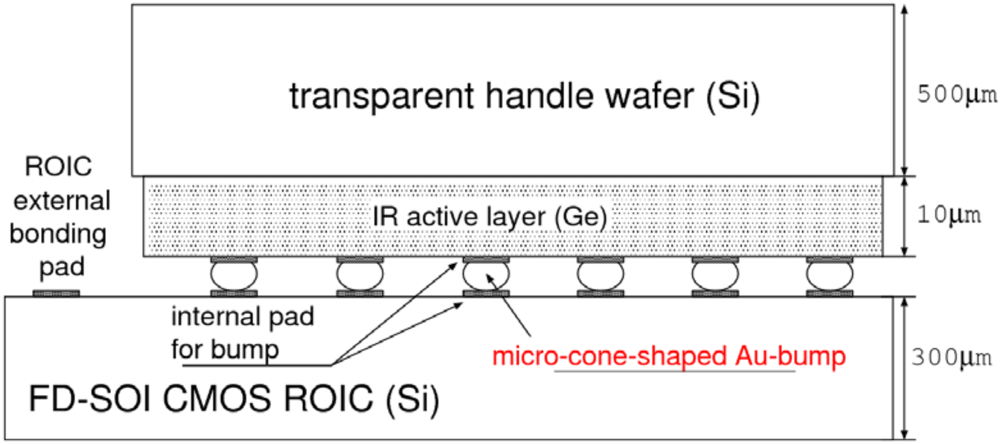
Au is oxidation resistant material and harder than Indium, so no under-fill is necessary. This is a large merit for cryogenic image sensor.

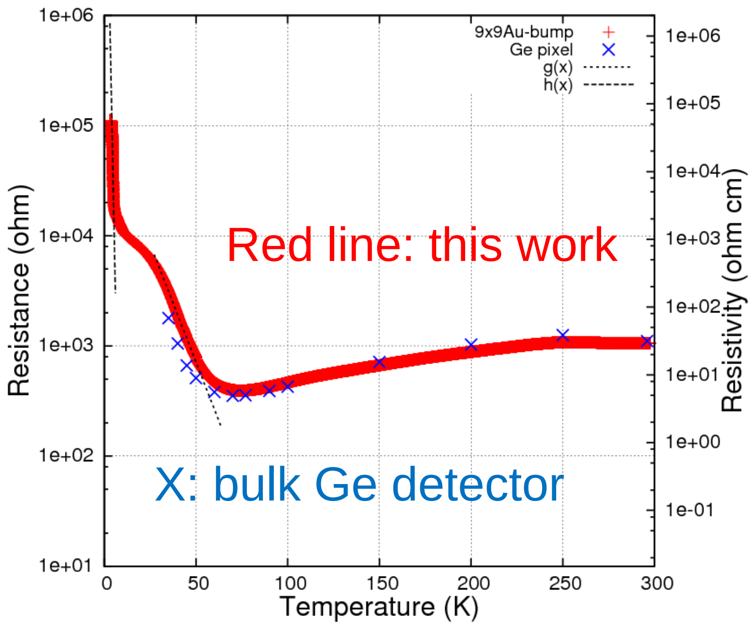
(Motoyoshi et al. 2015, JINST 10, C03004)

9 x 9 pixel Image sensor



We fabricated a demonstration 9 x 9 Image sensor (200 μm/pixel).
We measure resistance of the Ge detector through the NpD Au bump during the thermal cooling cycle down to 3 K. The resistance-temperature relation is similar to that of bulk Ge detector. This means the device operates properly.
All the pixels survive the cycle, and the change of resistance before and after the cycle is less than 5%.





Wada et al. 2016, JLTP 184, 217

Toward 32 x 32 FIR image sensor

- We have already fabricated 32 x 32 FD-SOI-CMOS CTIA ROIC.

  Nagase et al. P-34

- We have already fabricated 32 x 32 Ge-BIB detector on Si wafer.

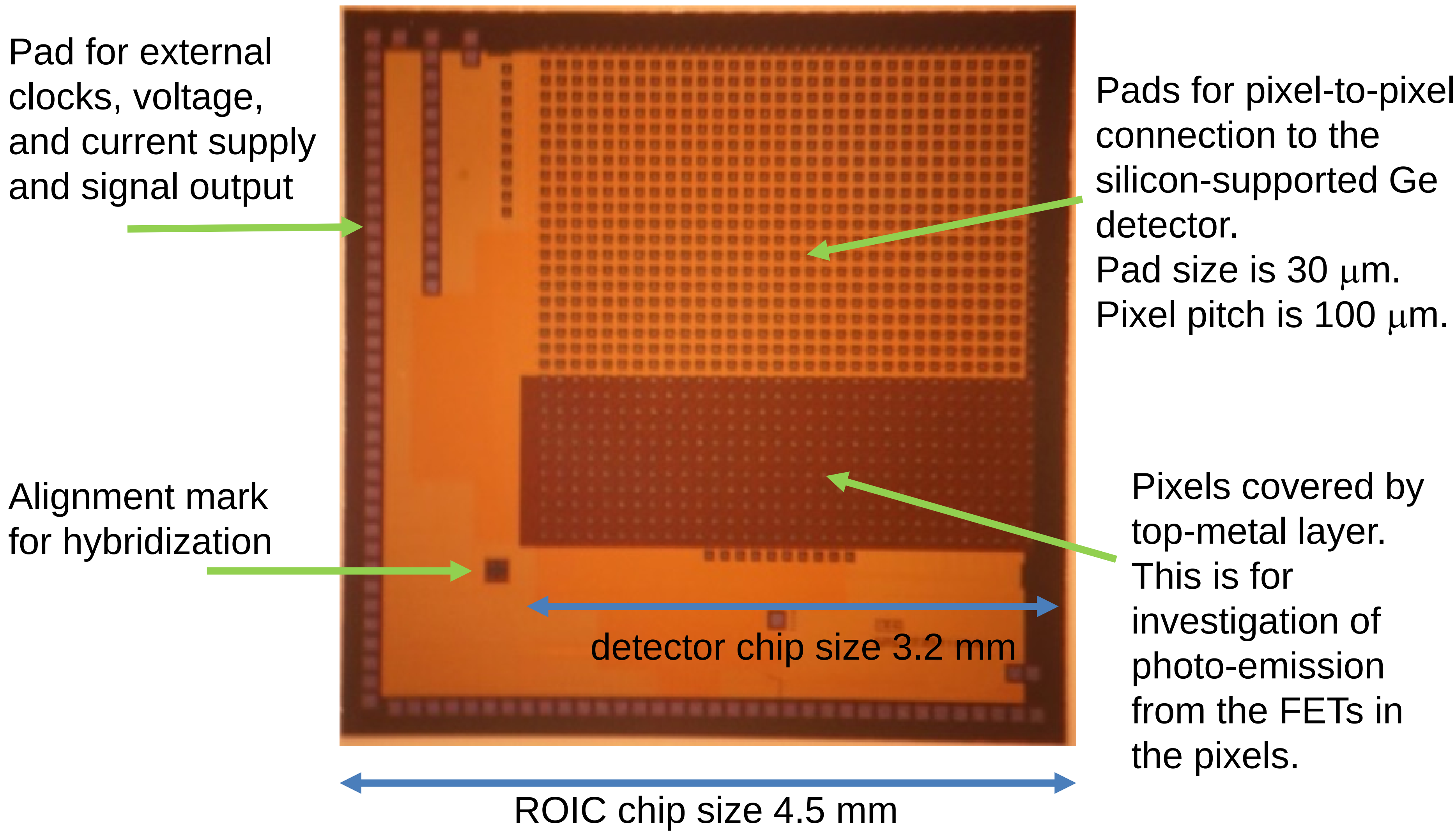
  Ishimaru et al. P-02

- Hybridization between the Si-supported Ge-BIB detector and FD-SOI CMOS ROIC will be done this fiscal year.
- We plan to make Balloon-borne telescope observations with Si-supported Ge-BIB detector

  Maeda et al. P-61

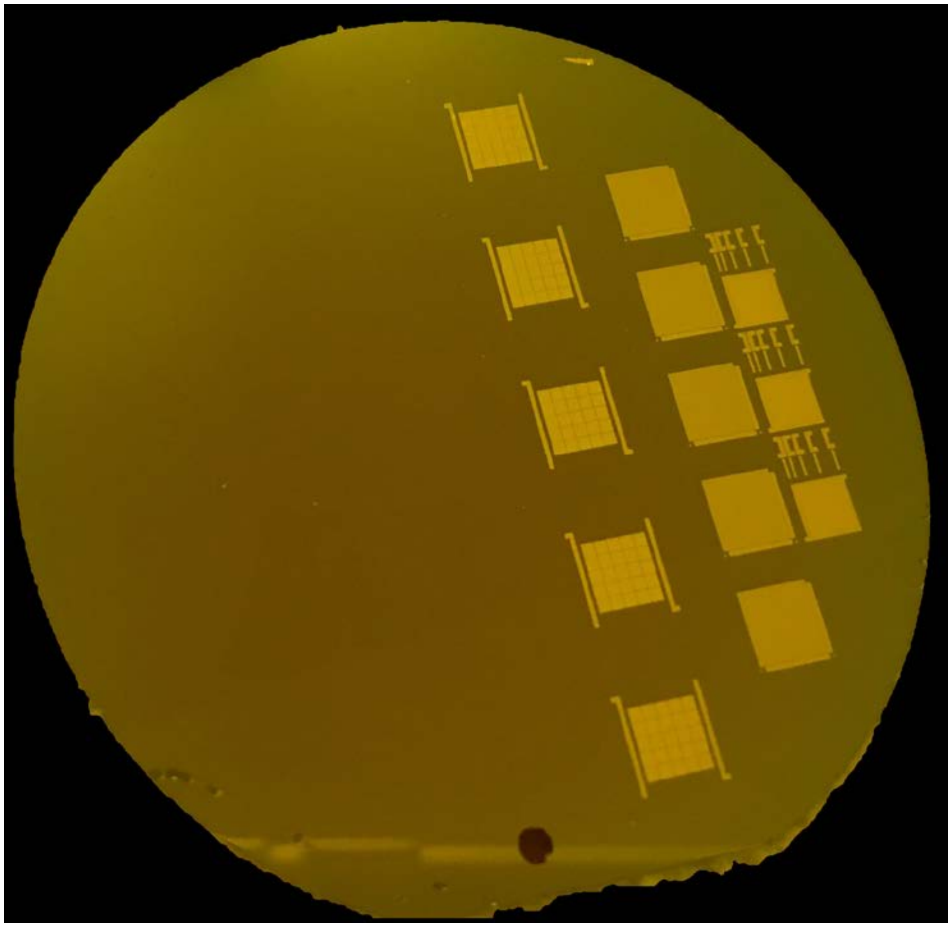
Nagase et al. P-34

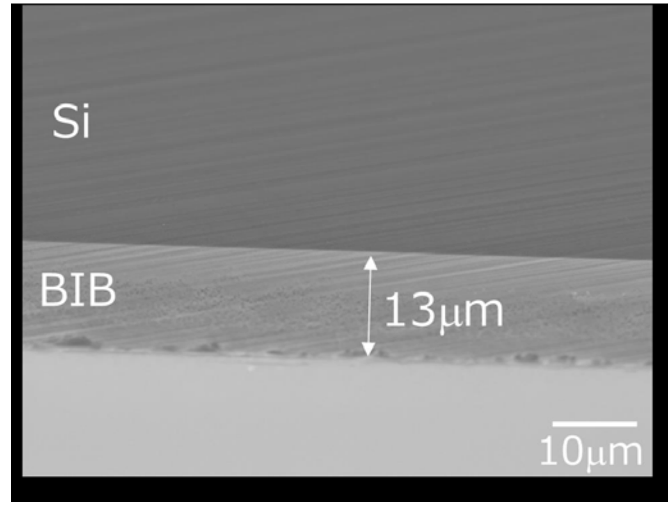
Photograph of 32x32 CTIA ROIC chip

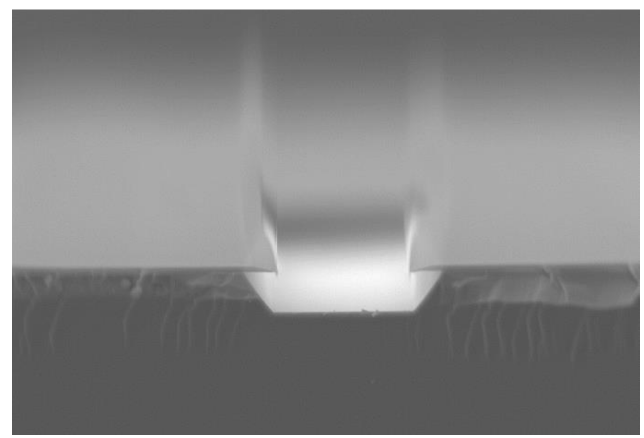


Fabrication of the Si-supported Ge BIB detector wafer

Ishimaru et al. P-02

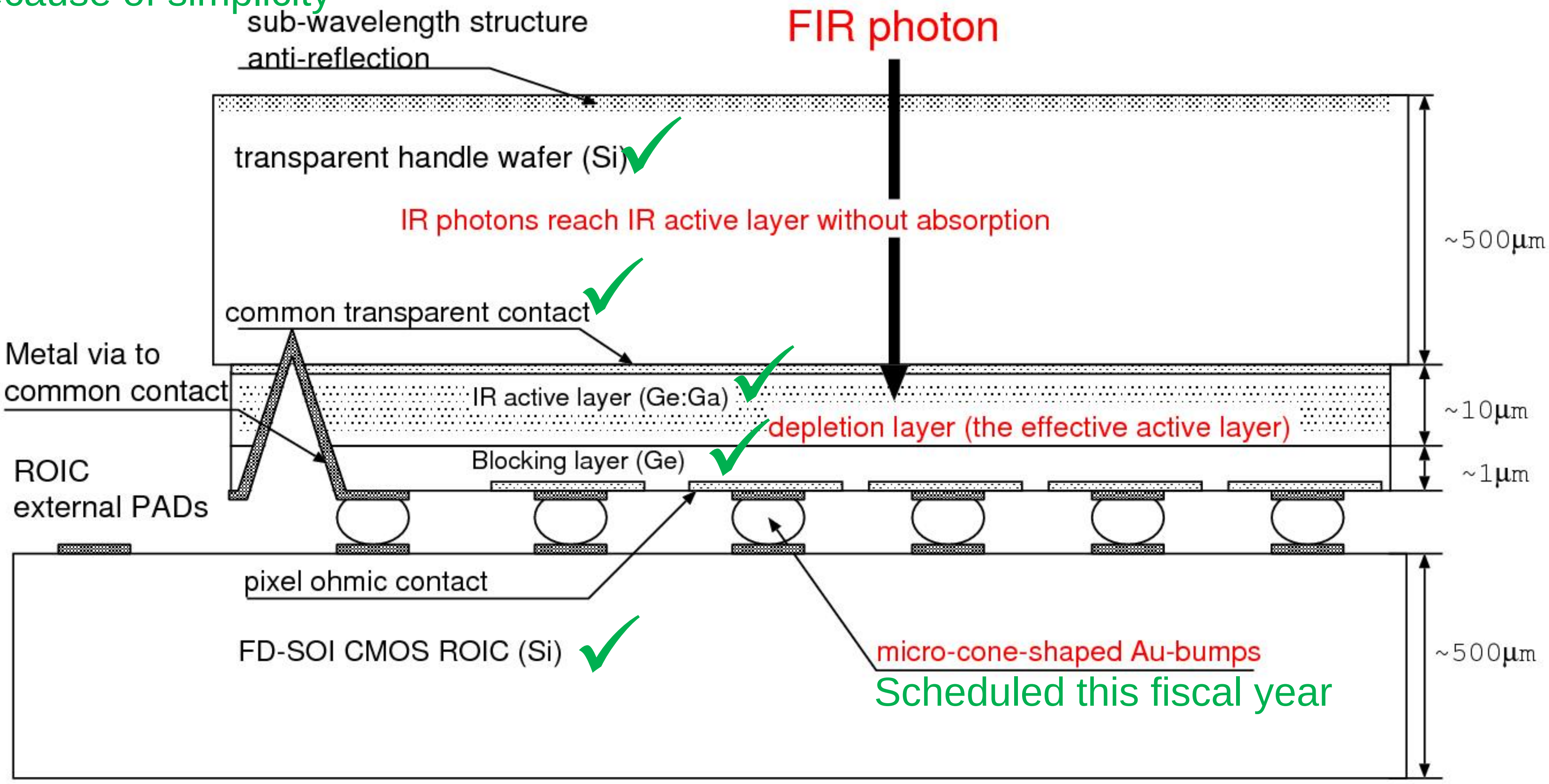






Yamamoto et al. P-63

Technology is ready, but not planned for this demonstration because of simplicity



Scheduled this fiscal year

summary

- We have developed Ge:Ga BIB far-infrared detector by SAB technology.
- We have also developed low-power high gain cryogenic CTIA ROIC by FD-SOI CMOS technology.
- We have demonstrated Si-supported Ge detector and NpD Au-bump hybridization for fabrication of Far-infrared image sensors.
- Fabrication of 32 x 32 FIR image sensor will be completed this fiscal year.
  - Nagase et al. P-34 FD-SOI CMOS cryo-ROIC
  - Ishimaru et al. P-02 Ge BIB detector fabrication
  - Yamamoto et al. P-63 Sub-wavelength structure anti- reflection
  - Maeda et al. P-61 Balloon-borne telescope observations
  - Wada et al. P-92 IR-SOIPIX, a monolithic MIR image sensor