Depleted Fully Monolithic CMOS Active Pixel Sensors in High Resistivity 150 nm Technology for LHC

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Introduction

- CMOS active pixel sensors have sensor part and readout circuitry in one chip.

This eliminates the need for fine pitch bump bonding between sensor and readout circuitry. As a result:

- Easier to produce
- Potentially cheaper production of pixel modules
Introduction

- Particle physics experiments in high radiation and high rate environment:
  - High radiation tolerance (TID, NIEL)
  - Fast response time
  - Fast readout

<table>
<thead>
<tr>
<th></th>
<th>ATLAS-LHC</th>
<th>ATLAS-HL-LHC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Outer</td>
<td>Inner</td>
</tr>
<tr>
<td>Timing [ns]</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>Particle Rate [kHz/mm²]</td>
<td>1000</td>
<td>10000</td>
</tr>
<tr>
<td>NIEL [nₑq/cm²]</td>
<td>2x10¹⁵</td>
<td>10¹⁵</td>
</tr>
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<td>10¹⁵</td>
</tr>
<tr>
<td>TID [Mrad]</td>
<td>80</td>
<td>50-80</td>
</tr>
<tr>
<td>TID [Mrad]</td>
<td></td>
<td>&gt;500</td>
</tr>
</tbody>
</table>

Depleted Monolithic Active CMOS Pixel Sensors (DMAPS)
  - Charge collection by drift
  - Full readout architecture
150 nm Technology

- LFoundry 150 nm CMOS: High Resistive wafer (>2kΩcm) and High Voltage
  → sufficient (~150μm) depletion
  \[ d \propto \sqrt{HV \times HR} \]
- Radiation tolerant technology
- Multiple wells up to 4 wells
  → PMOS and NMOS can be used in pixel readout
  → Digital signal processing in pixel
- Large fill factor approach
  😊 Short charge collection path
  😞 Capacitance between wells requires dedicated circuitry
- Back side processing

Top view

- Readout
- Collection well (fill factor ~ 50%)

Side view

- p-substrate

- HV
150 nm Technology

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  → PMOS and NMOS can be used in pixel readout
  → Digital signal processing in pixel
- Large fill factor approach
  ☺ Short charge collection path
  😞 Capacitance between wells requires dedicated circuitry
- Back side processing
Prototype chips

- **CCPD_LF**
  - Pixel size: 33 μm x 125 μm
  - Chip size: 5 mm x 5 mm
  - Fast R/O with FE-I4
  - Thickness: 750, 300, 100 μm
  - Bonn/CCPM/KIT

- **LF-CPIX**
  - Pixel size: 50 μm x 250 μm
  - Chip size: 10 mm x 10 mm
  - Fast R/O with FE-I4
  - Thickness: 750, 200, 100 μm
  - Bonn/CCPM/IRFU

- **LF-MonoPix (Full Monolithic)**
  - Pixel size: 50 μm x 250 μm
  - Chip size: 10 mm x 10 mm
  - Column drain R/O architecture
  - Thickness: 750, (200, 100) μm
  - Bonn/CCPM/IRFU

Sensor + Analog (Disc.)
- Pixel size: 33 μm x 125 μm
- Chip size: 5 mm x 5 mm
- Fast R/O with FE-I4
- Thickness: 750, 300, 100 μm
- Bonn/CCPM/KIT

Sensor + Analog
- Pixel size: 50 μm x 250 μm
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Sensor + Analog + Digital
- Pixel size: 50 μm x 250 μm
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**Pixel design**

- **Charge sensitive amplifier**
- **In-pixel 4-bit DAC for threshold trimming**
- **Hit register (1-bit counter)**
- **8-bit time stamp @ 40 MHz**
  - *Time, charge of signal*

- **Full-custom dig. circuit**
  - *Minimized area => for less $C_d$*
  - *Low noise circuit design for critical dig. blocks*
    - *eg. current steering logic, RAM r/o by source follower*

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CCPD_LF, LF-CPIX

LF-MonoPix

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11th International "Hiroshima" Symposium - Dec 10-15 2017, Okinawa, Japan
- The guard rings have been improved to increase the breakdown voltage.
- The increase of the leakage current around the full depletion voltage has been suppressed by improving the backside process.

Breakdown = 280V

measured by I. Caicedo
**Pixel profile (laser response)**

**DUT:**
- Chip: LF-CPIX
- Thickness: 100 μm
- w/o metarization
- Bias voltage: -200V
- Laser:
  - Wave length = 680 nm
  - Beam size: 2.5 μm

**Row (short)**

![Graph showing normalized intensity vs. position for row (short)]

- σ = 2.4 μm

**Column (long)**

![Graph showing normalized intensity vs. position for column (long)]

- σ = 2.5 μm

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N-well

P-well

Top view

Laser

-200V

HV

100 μm

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Sigma of beam profile saturates around bias voltage of 17V
→ **Full depletion** voltage = \( \sim 17V \) for the chip thickness of 100 \( \mu \)m
The prototype chips (CSA+Discr.) were irradiated with X-ray up to 50 Mrad

- Input transistor of CSA
  - NMOS
  - PMOS
  - CMOS

- Bias voltage: -100V

- Gain degradation: <5%
- Noise increase: ~30%

- No significant difference between the 3 flavors
Radiation hardness (TID)

The threshold is still tunable after TID=50Mrad ($\sigma<100e$ cf. readout noise $\approx 200e$)

• Increase of the tuned threshold dispersion is 20e
Radiation hardness (NIEL)

- The neutron irradiation test was done in JSI and the MonoPix were annealed 80min @60C

I-V curve of MonoPix

- Breakdown voltage is higher than 200V
The MPV is decreased after neutron irradiation of $1 \times 10^{15}\text{n}_{\text{eq}}/\text{cm}^2$.
Hit efficiency

- **Un-irradiated**
  
  Chip: MONOPIX un-irradiated  
  DAC setting: default  
  TH: tuned by noise + 4mV (~1750e)  
  HV: -200V  
  Temp: dry ice  
  Source: 2.5GeV electron

- **$1 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$**
  
  Chip: MONOPIX irradiated  
  DAC setting: default  
  TH: tuned by noise (~1500e)  
  **HV**: -130V  
  Temp: dry ice  
  Source: 2.5GeV electron

![Graph showing hit efficiency](image1)

99.6%

![Graph showing hit efficiency](image2)

98.9%
In the irradiated sample, the degradation of the efficiency observed not only at the corner of pixels but also in the middle of the pixel.
Time walk (preliminary)

- Measurement setup
- Time walk of seed pixel

- The time walk of MonoPix was increased after the irradiation.
  - CSA or discriminator’s degradation due to background TID of the reactor?
- This might be improved by...
  - Optimization of the parameters (current of CSA, discriminator etc)
  - Higher bias voltage, Back side process

Threshold: 1500 e
Bias: -200V (0 n$_{eq}$/cm$^2$)
-130V (1 x 10$^{15}$n$_{eq}$/cm$^2$)
DAC setting: Default
Temperature: cooled by dry ice

2bins=98.7 ± 0.9%
2bins=83.0 ± 0.8% un-tuned!
Conclusion and outlooks

• Depleted Monolithic Active CMOS Pixel Sensors (DMAPS) in High Resistivity 150 nm Technology has been developed
  – Full monolithic readout works as expected
  – Break down voltage: >250V
  – Full depletion of 100 µm sensor: ~17V

• Radiation hardness has been tested by X-ray and neutron
  – TID
    • Degradation of gain = ~5%
    • Increase of noise = factor of 1.3
  – NIEL
    • Break down voltage still higher than 200V
    • Hit efficiency 98.9% after irradiation
    • MPV decreased → Backside process are planned
    • Time walk → optimization of operating parameters (current of CSA, Discr.)
Backup
both have
  • PMOS input transistor
  • Bias voltage: -100V

Gain degradation:
  LF-CPIX < CCPD_LF 😐
Noise increase:
  LF-CPIX ≈ CCPD_LF 😞

What makes the difference? not 100% clear ...
Pixel size, small changes in MOSFET size, global DAC of the chip, wafer, process...
Power consumption of CSA (CCPD_LF)
Change of the feedback current was measured by the pulse height and width of CSA output

- DUT: LFCPIX
- Flavor: PMOS-CSA
- Bias voltage: 100V

No change in the feedback of CSA
Measurement setup

• Laser: Wave length = 680 nm → Attenuation length of Si = 4 μm
  Beam size ~ 2.5 μm
• Chip: LF-CPIX v2 100 μm backside processed (without metallization)
  Readout: analog output of CSA

11th International "Hiroshima" Symposium - Dec 10-15 2017, Okinawa, Japan
The edge pixel collects charges created outside of the pixel matrix.
The crosstalk was observed in the neighbor pixels.

\[
\begin{align*}
\text{Signal(next row)} &= 1.8\% \\
\text{Signal(next column)} &= 0.15\%
\end{align*}
\]
Cross talk

• Capacitors between pixels cause the cross talk

\[
\text{Signal(neighbor)} = \text{Signal(laser)} \times \frac{C}{C + C_{\text{in}}}
\]

Signal(next row) = 1.8 %
Signal(next column) = 1.5 %

C(row) = 19 fF
C(column) = 1.5 fF

C (4 neighbors) = 40 fF

cf. \(C(\text{all}) = 400 \, \text{fF}\)

Measured by M. Daas and M. Loepke in Bonn

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sLHC meeting – Jun 14, 2017
Threshold dispersion

- **Un-irradiated**
  - Chip: MONOPIX un-irradiated
  - DAC setting: default
  - TH: tuned by noise + 4mV
  - Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
  - Enabled readout: col 16-20
  - HV: -200V
  - Temp: dry ice
  - Source: 2.5GeV electron

- **$1 \times 10^{15} \text{n}_{eq}/\text{cm}^2$**
  - Chip: MONOPIX irradiated
  - DAC setting: default
  - TH: tuned by noise
  - Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
  - Enabled readout: col 16-20
  - HV: -130V
  - Temp: dry ice
  - Source: 2.5GeV electron

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Noise occupancy

- **Un-irradiated**
  
  Chip: MONOPIX un-irradiated  
  DAC setting: default  
  TH: tuned by noise  
  Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix  
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  Source: 2.5GeV electron
Measurement setup

MONOPIXs (irradiated, un-irradiated)

- **MIMOSA x 6**
  - Pixel size: 18.2 μm x 18.2μm
  - 1152 μs/frame (rolling shutter)
- **FE-I4 x 1**
  - Pixel size: 250 μm x 50 μm
  - Timing resolution: 25ns (triggered by scintillator + TLU)
• **Un-irradiated**

  Thickness of chip: 750µm  
  Chip: MONOPIX un-irradiated  
  DAC setting: default  
  TH: tuned by noise + 4mV  
  Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix  
  Enabled readout: col 16-20  
  HV: -200V  
  Temp: dry ice  
  Source: 2.5GeV electron

• **$1 \times 10^{15}$n$_{eq}$/cm$^2$**

  Thickness of chip: 750µm  
  DAC setting: default  
  TH: tuned by noise  
  Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix  
  Enabled readout: col 16-20  
  HV: -130V  
  Temp: dry ice  
  Source: 2.5GeV electron

![Graph showing residual distribution with σ=35.4µm and σ=38.6µm](image)

![Graph showing residual distribution with σ=36.7µm](image)

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Residual

• **Un-irradiated**

  Thickness of chip: 750um
  Chip: MONOPIX un-irradiated
  DAC setting: default
  TH: tuned by noise + 4mV
  Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
  Enabled readout: col 16-20
  HV: -200V
  Temp: dry ice
  Source: 2.5GeV electron

  

• **$1 \times 10^{15} n_{eq}/cm^2$**

  Thickness of chip: 750um
  DAC setting: default
  TH: tuned by noise
  Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
  Enabled readout: col 16-20
  
  **HV: -130V**
  Temp: dry ice
  Source: 2.5GeV electron

  
  ![Graph 1](#)

  **Background = 0.6%**

  ![Graph 2](#)

  **Background = 0.3%**

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