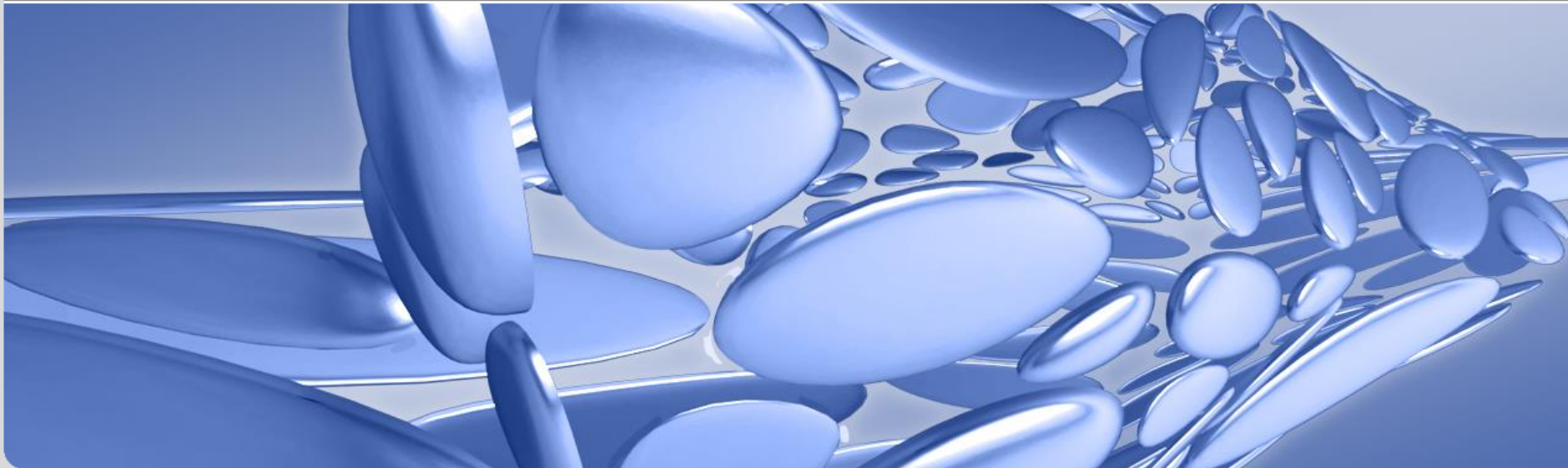


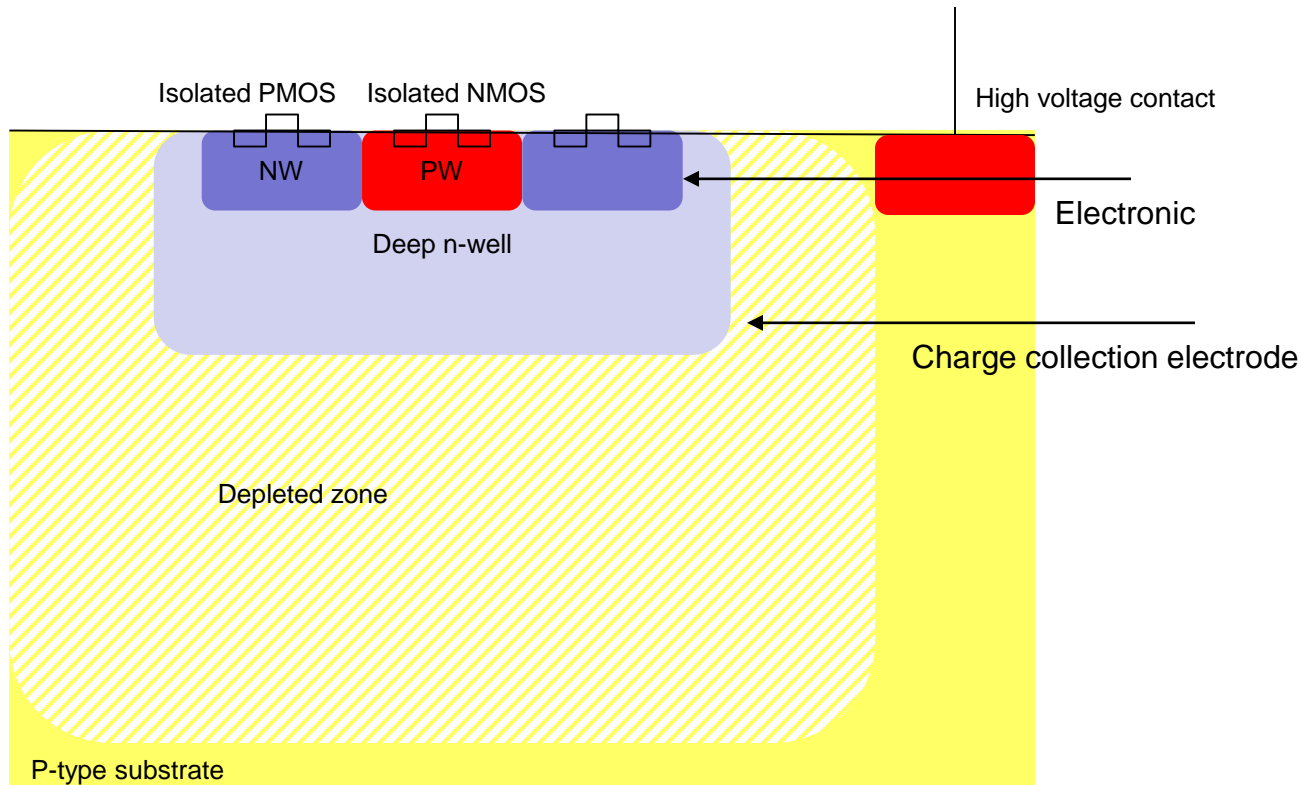
# HVCMOS Sensors - Progress towards final tracking sensor designs for Mu3e and ATLAS experiments

Ivan Peric,

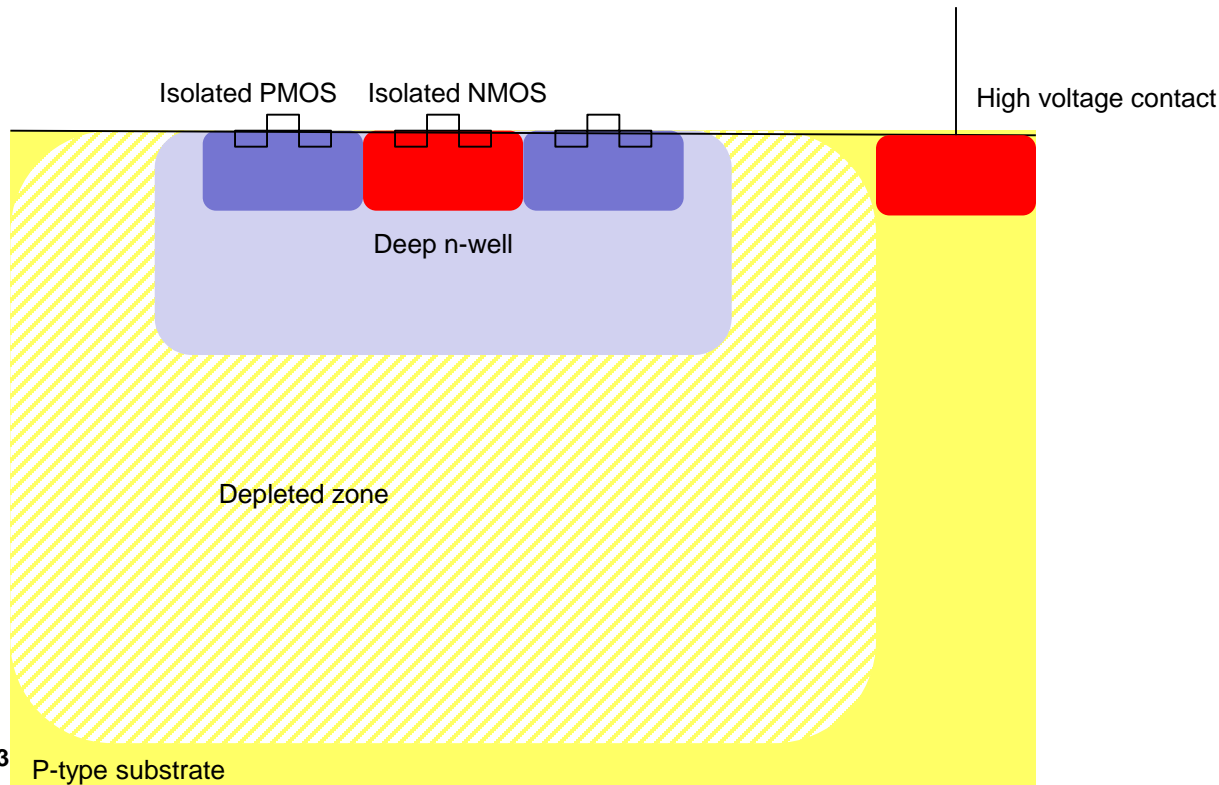
Mridula Prathapan, Alena Weber, Rudolf Schimassek, Felix Ehrler, Winnie Wong, Patrick Pangaud, Eva Vilella Figueras, Raimon Casanova Mohr, Heiko Augustin, Hui Zhang, Niklaus Berger



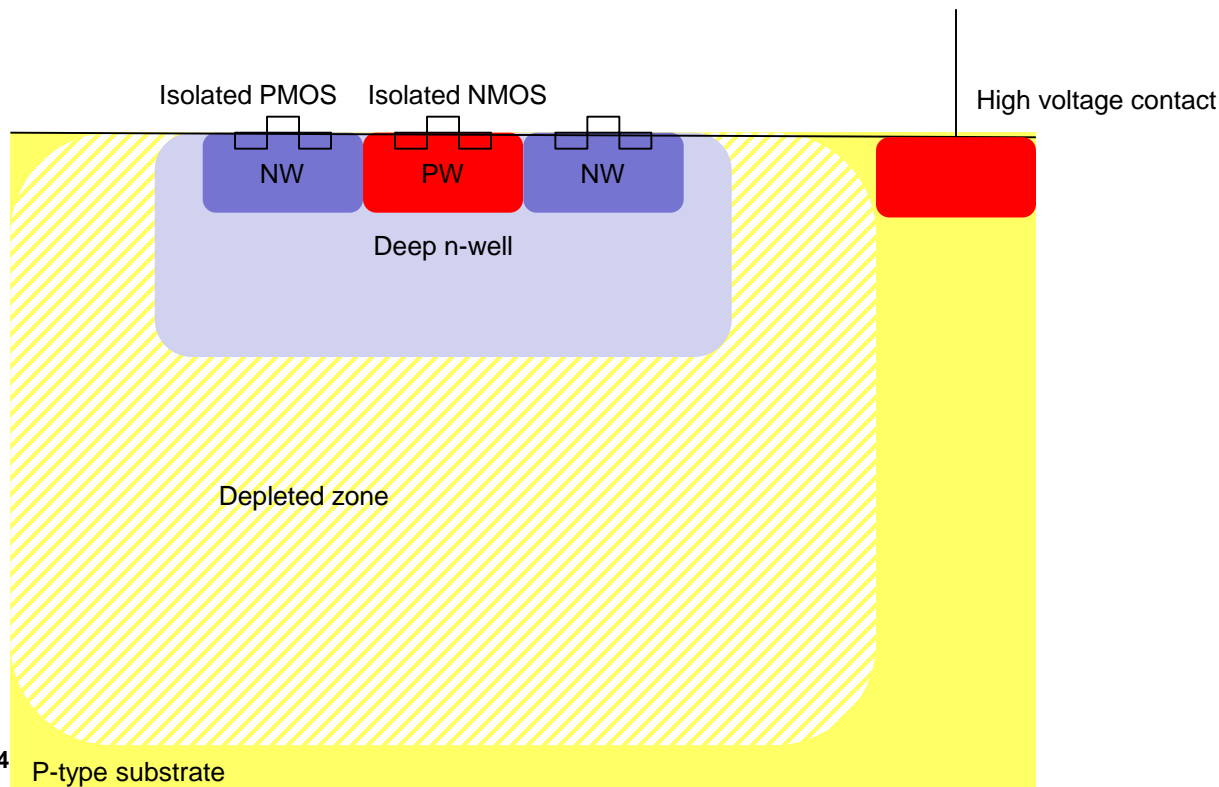
- The HVCMOS sensors allow construction of radiation hard particle pixel detectors in standard CMOS technologies



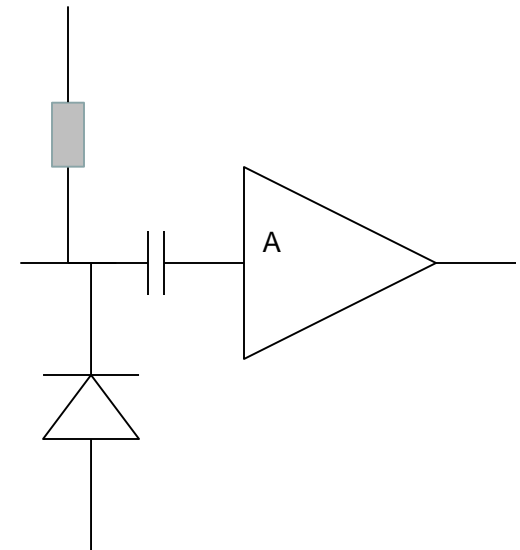
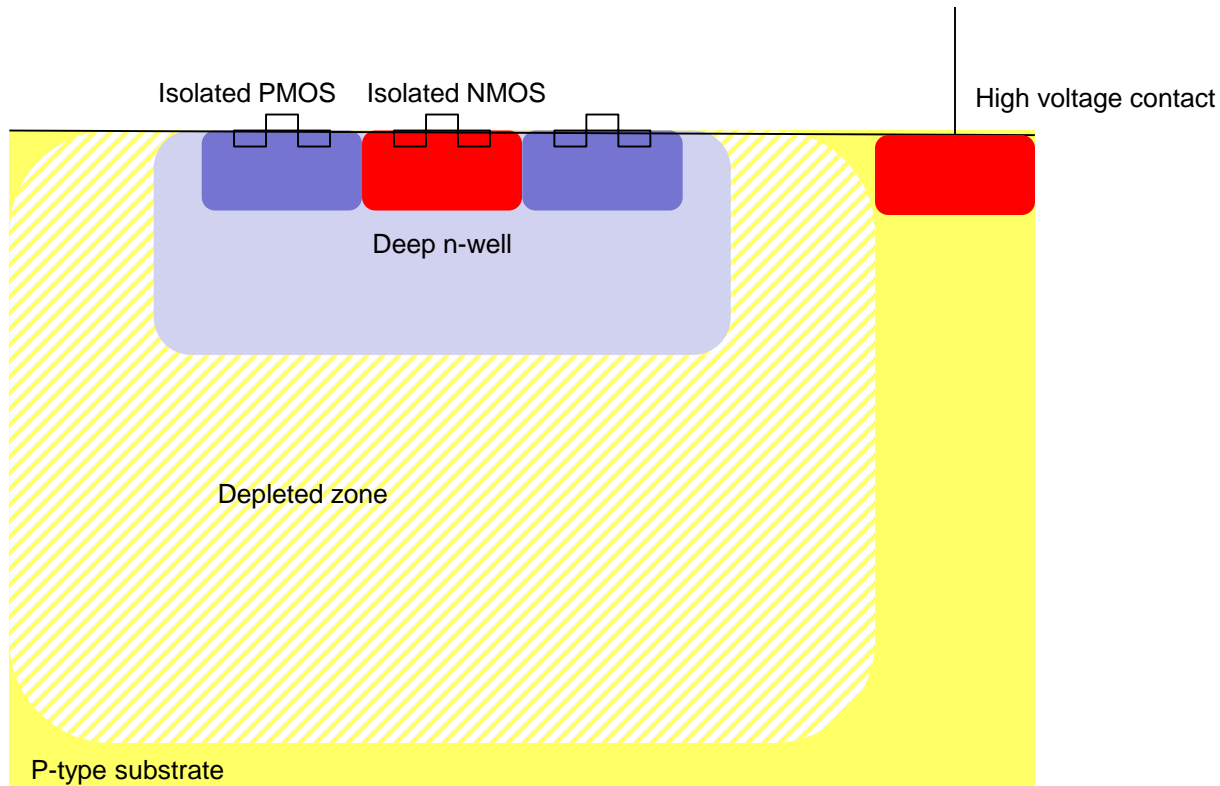
- Advantages:
- High radiation tolerance (fast charge collection, short drift path, vertical depletion)
- Biasing from front side (no need for backside contact)
- Large depletion layer can be induced



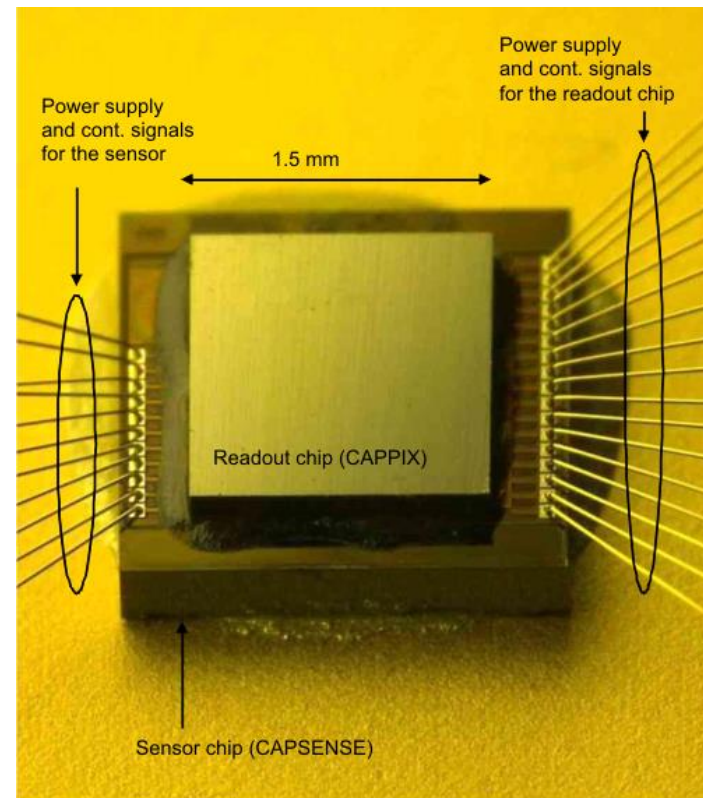
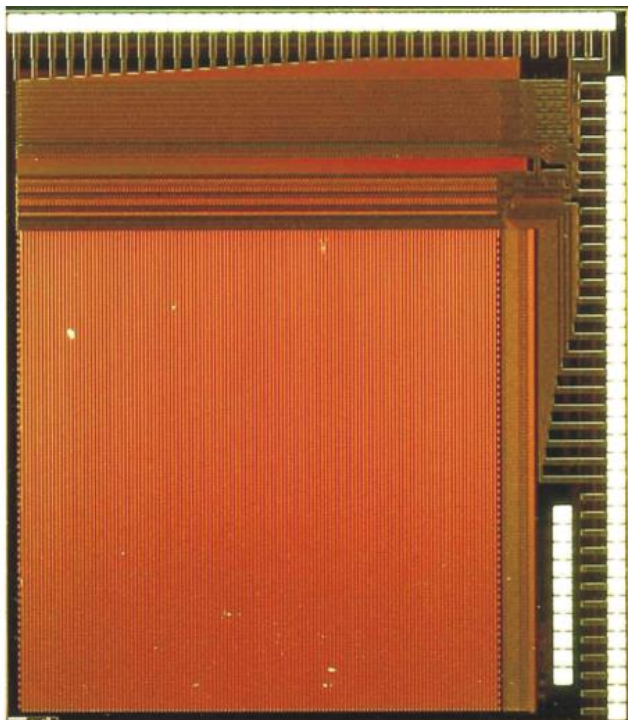
- Disadvantage:
- High capacitance
- PW-DNW dominates
- Typically: for pixel size  $50\mu\text{m} \times 150\mu\text{m}$ , (PW size  $22\mu\text{m} \times 12\mu\text{m}$ )
- DNW: 70fF, PW-DNW: 110fF



- N-well is 1) substrate for PMOS transistors and 2) charge collecting electrode.



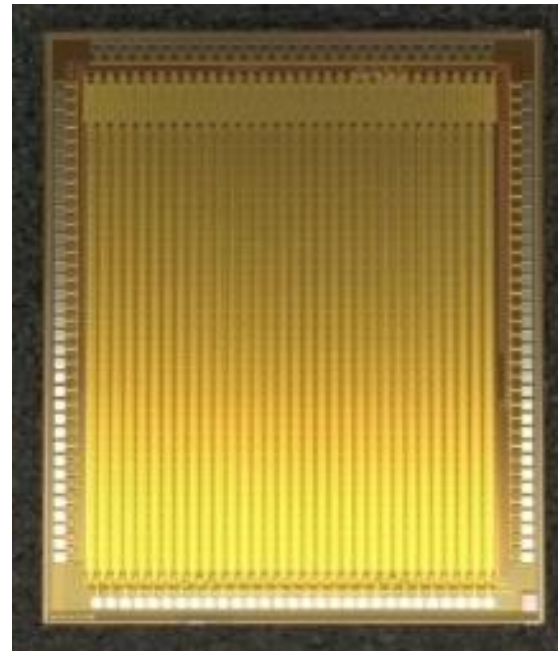
- Development of these sensors started in 2006. In the first phase we have proven the functionality.



- Since 2011 developments for Mu3e, ATLAS and CLIC
- Mu3e - monolithic readout
- (Sensor contains all the readout circuits on chip)
- ATLAS - CCPD readout
- (Sensor was readout by the pixel readout ASIC that was capacitively coupled to the sensor)
- Sensors have been produced in standard AMS H18 process without any modification and within MPW runs

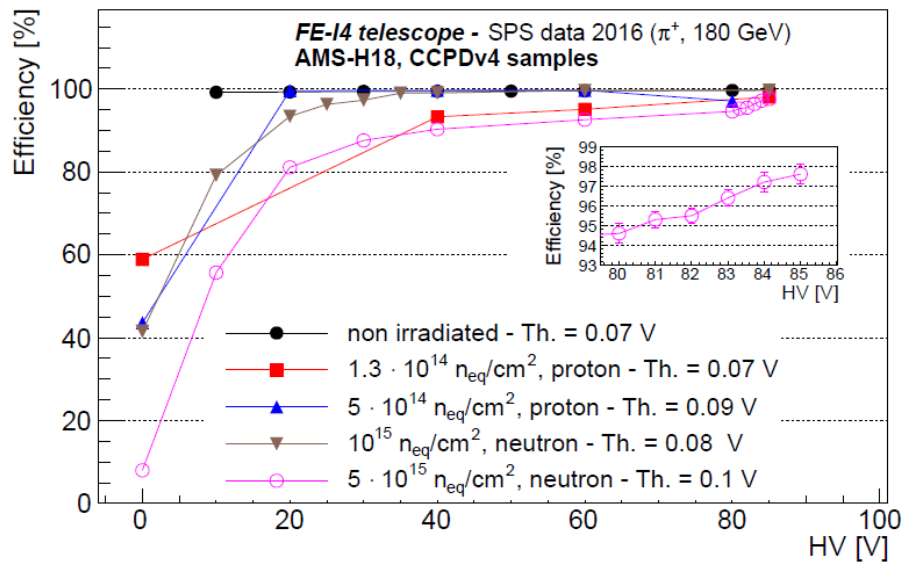


CCPD (1-8)

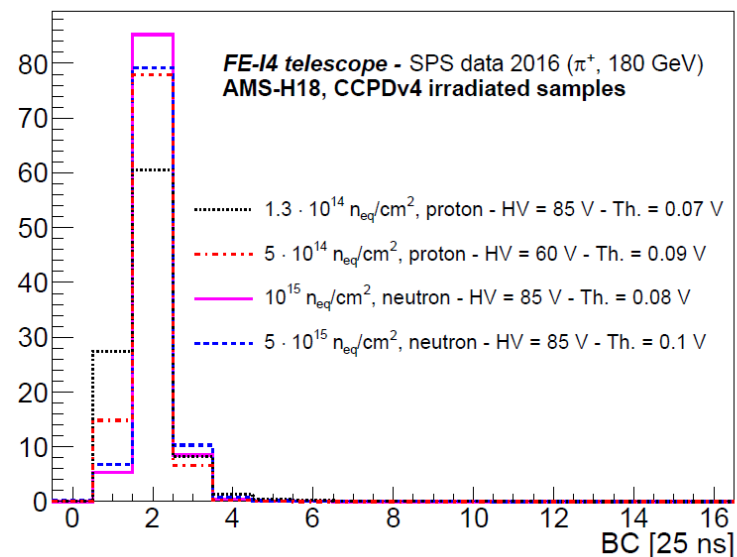


MuPixel 7

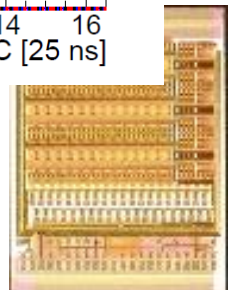
- Achievements:
- Time resolution  $\sim 25\text{ns}$ , radiation hardness of  $100\text{MRad}$  and  $5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ . Fast readout on sensor chip with high bandwidth amplifiers. Possibility to thin sensors to  $\sim 50\mu\text{m}$ .



M. Benoit et al.,  
“Testbeam results of irradiated AMS H18 HV-CMOS pixel sensor prototypes”  
arXiv:1611.02669 [physics.ins-det]

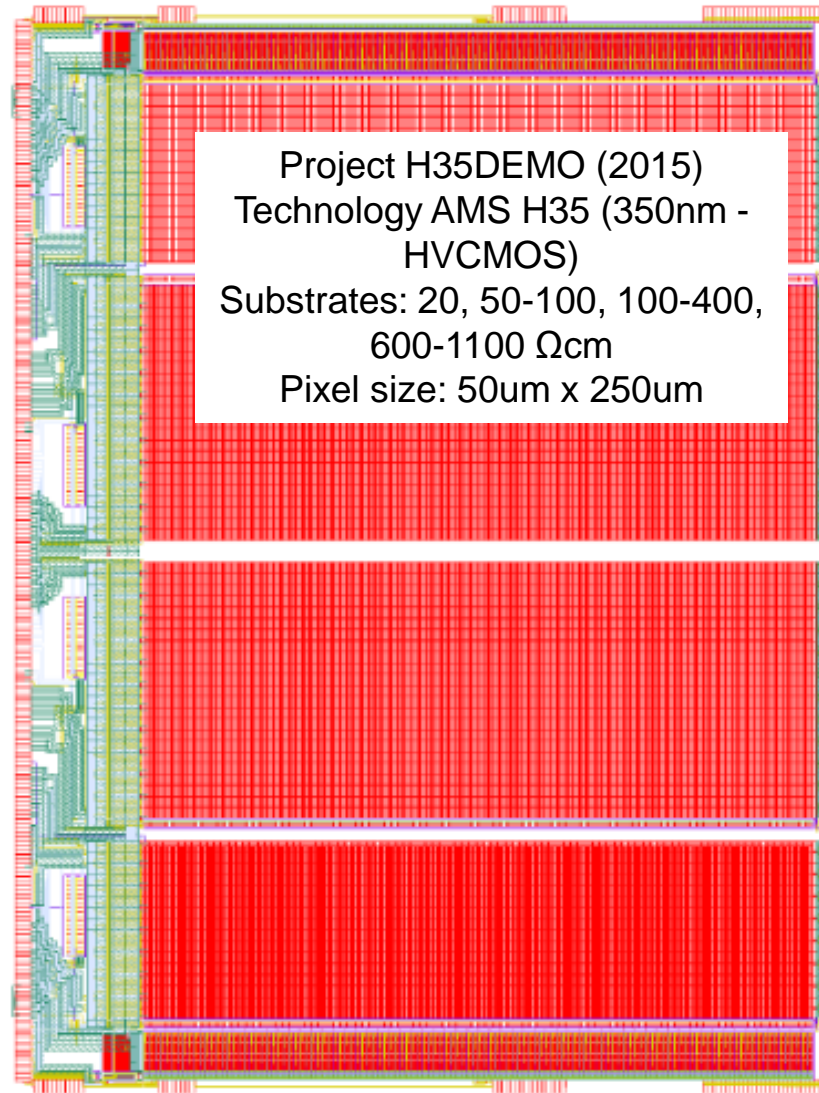
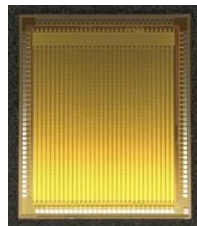


Low resistivity  
Absolute efficiency measured  $>99\%$   
Whole matrix used (full readout)  
2 bins 95%





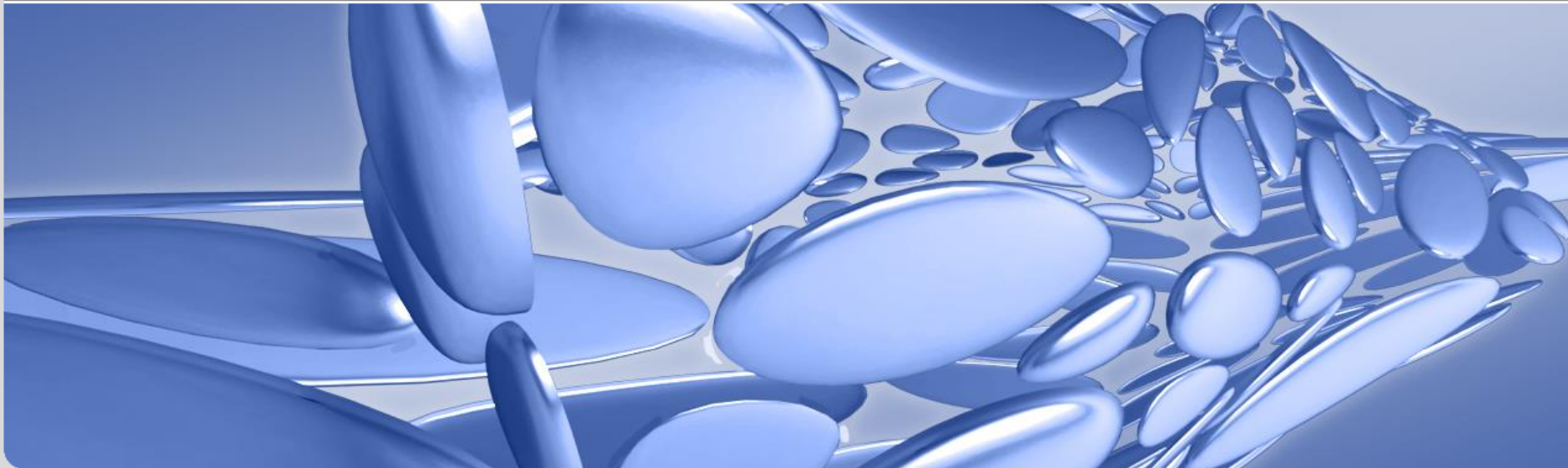
- Since 2015 large sensors have been designed and submitted



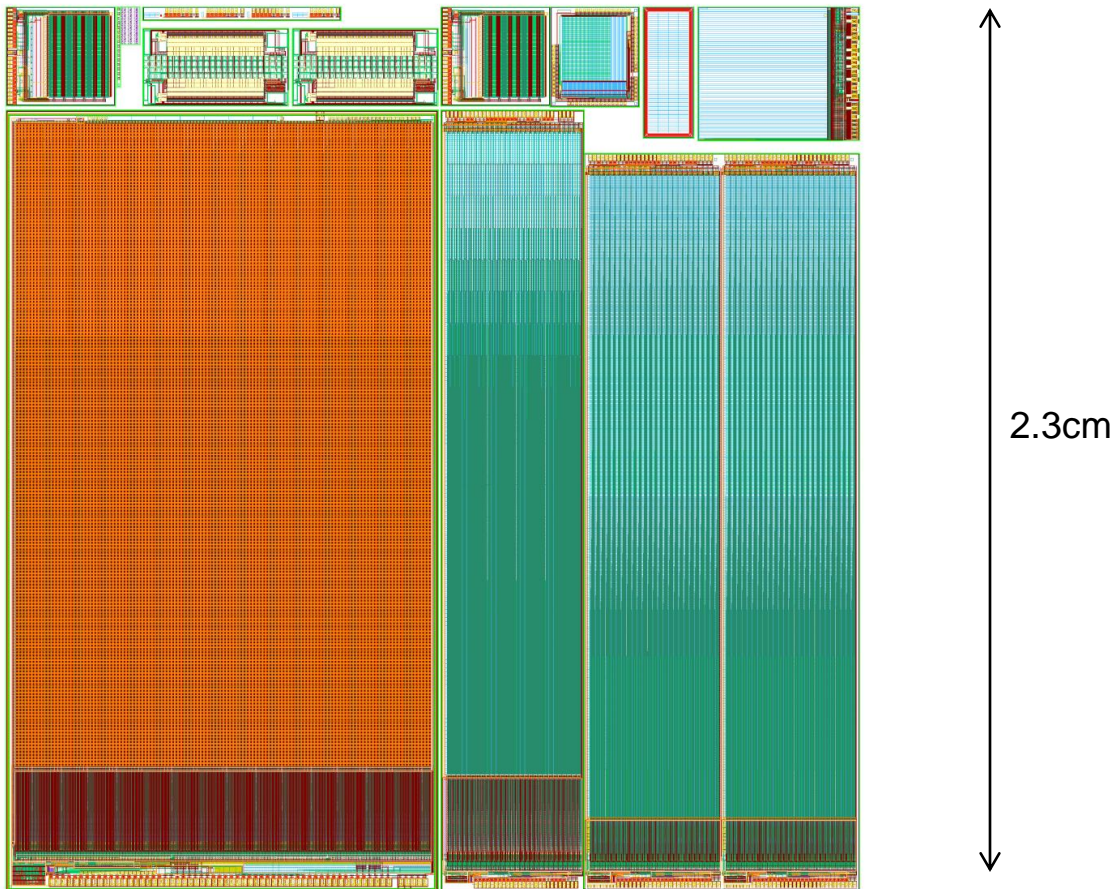
Project H35DEMO (2015)  
Technology AMS H35 (350nm -  
HVC MOS)  
Substrates: 20, 50-100, 100-400,  
600-1100  $\Omega\text{cm}$   
Pixel size: 50 $\mu\text{m}$  x 250 $\mu\text{m}$

2.5cm

## Monolithic Sensors in AMS aH18 Technology



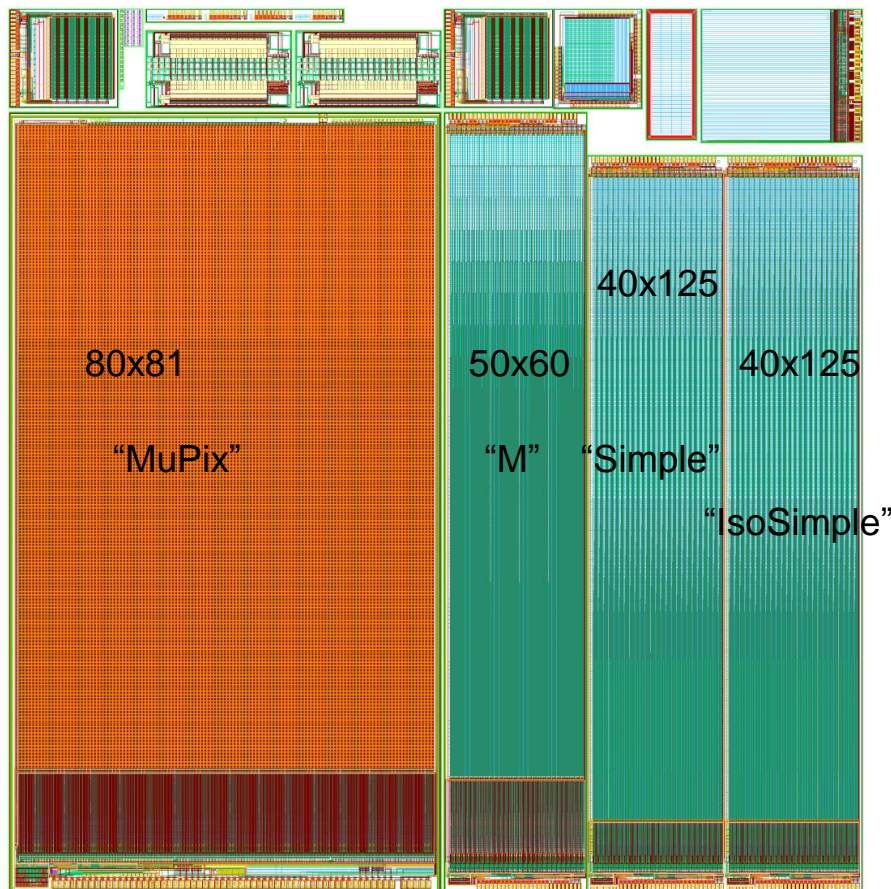
- In 2017 we have designed and submitted reticle size preproduction designs for Mu3e and ATLAS
- The sensors have been submitted within an engineering run





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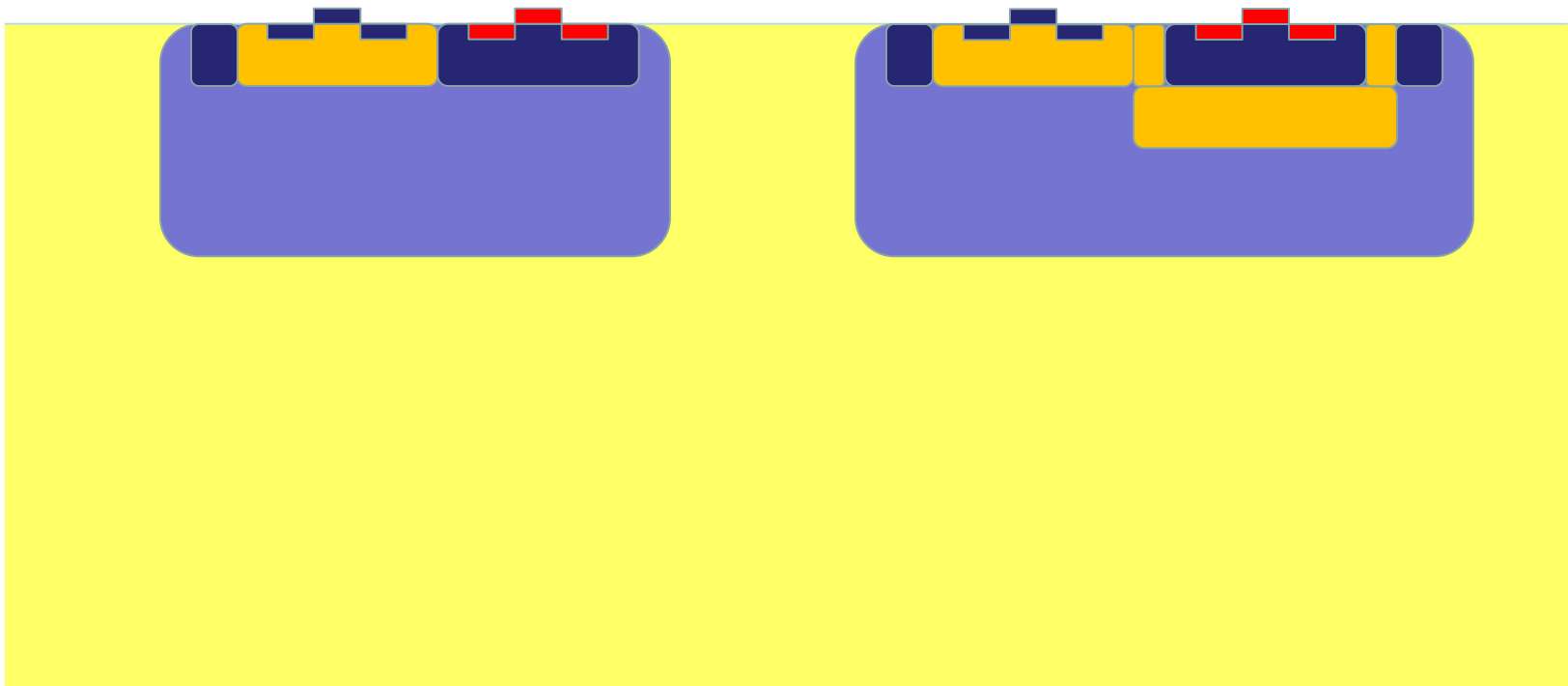
MuPix - sensor for mu3e, with radiation hardened design. The chip uses analog pixels and column drain readout.



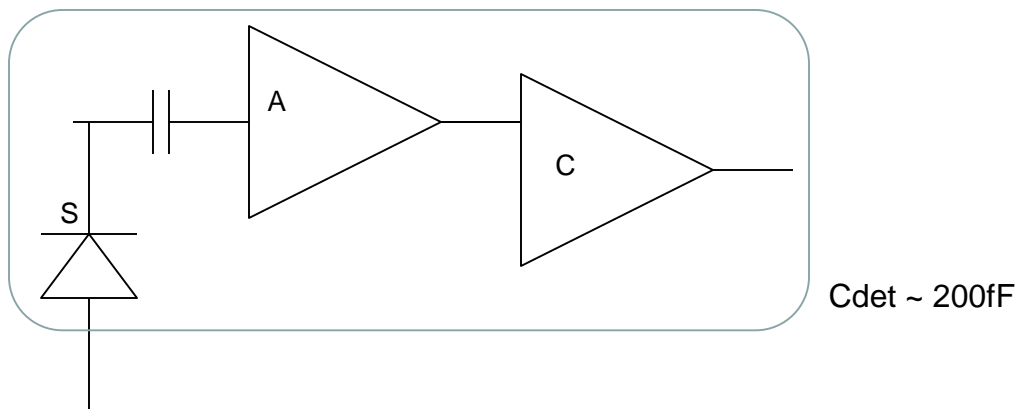
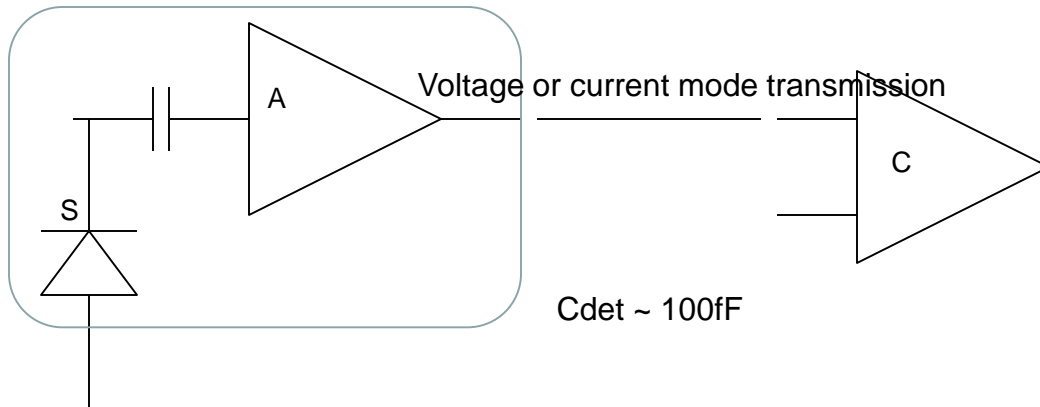
ATLASpix. The design variant M2 uses the novel triggered readout with parallel pixel to trigger-buffer data transfer. "Simple" chips use the column drain readout. All sensors for ATLAS use the pixels with comparators. The simple variant ISO, uses the comparator with deep p-well.

2.3cm

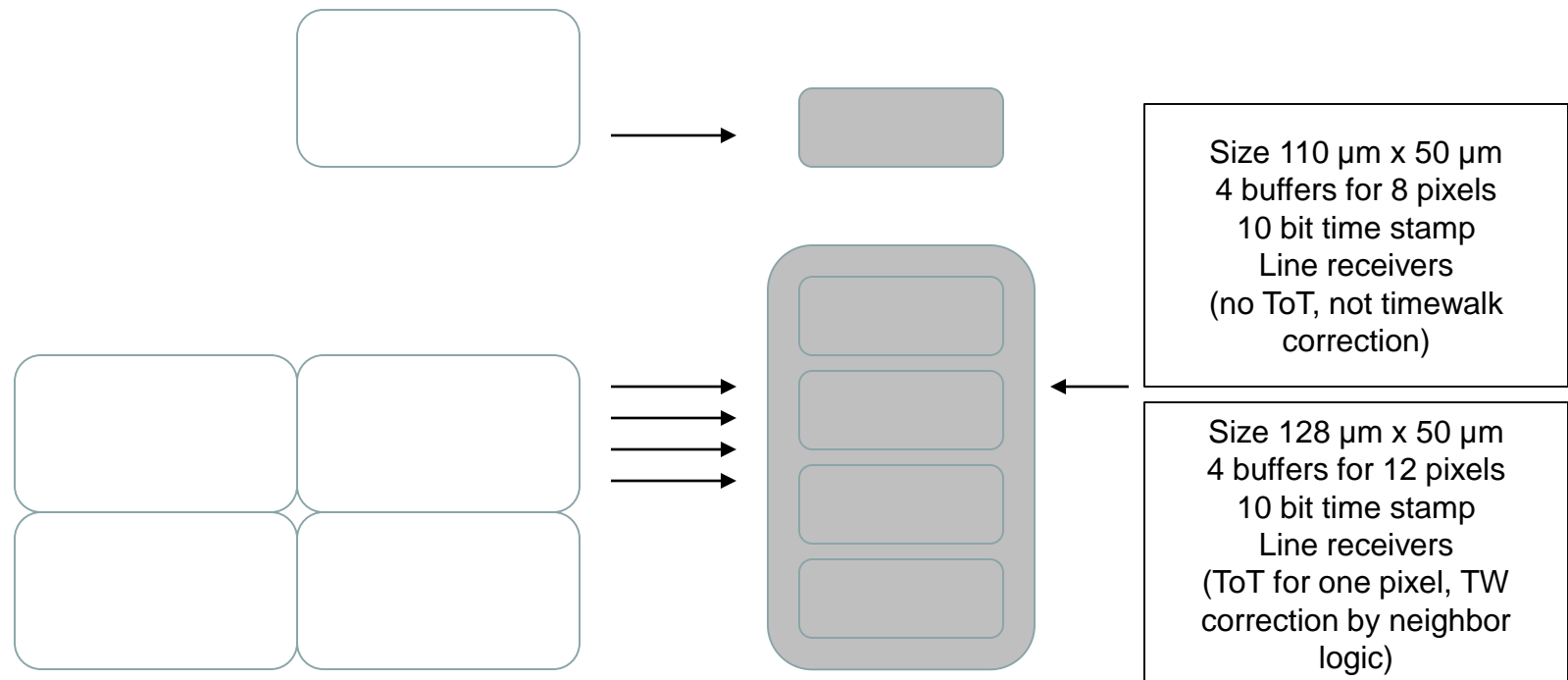
- High resistivity substrates have been used (80/200 $\Omega$ cm)
- Deep p-well implant has been added.
- Isolation of PMOS transistors from the deep n-well is possible



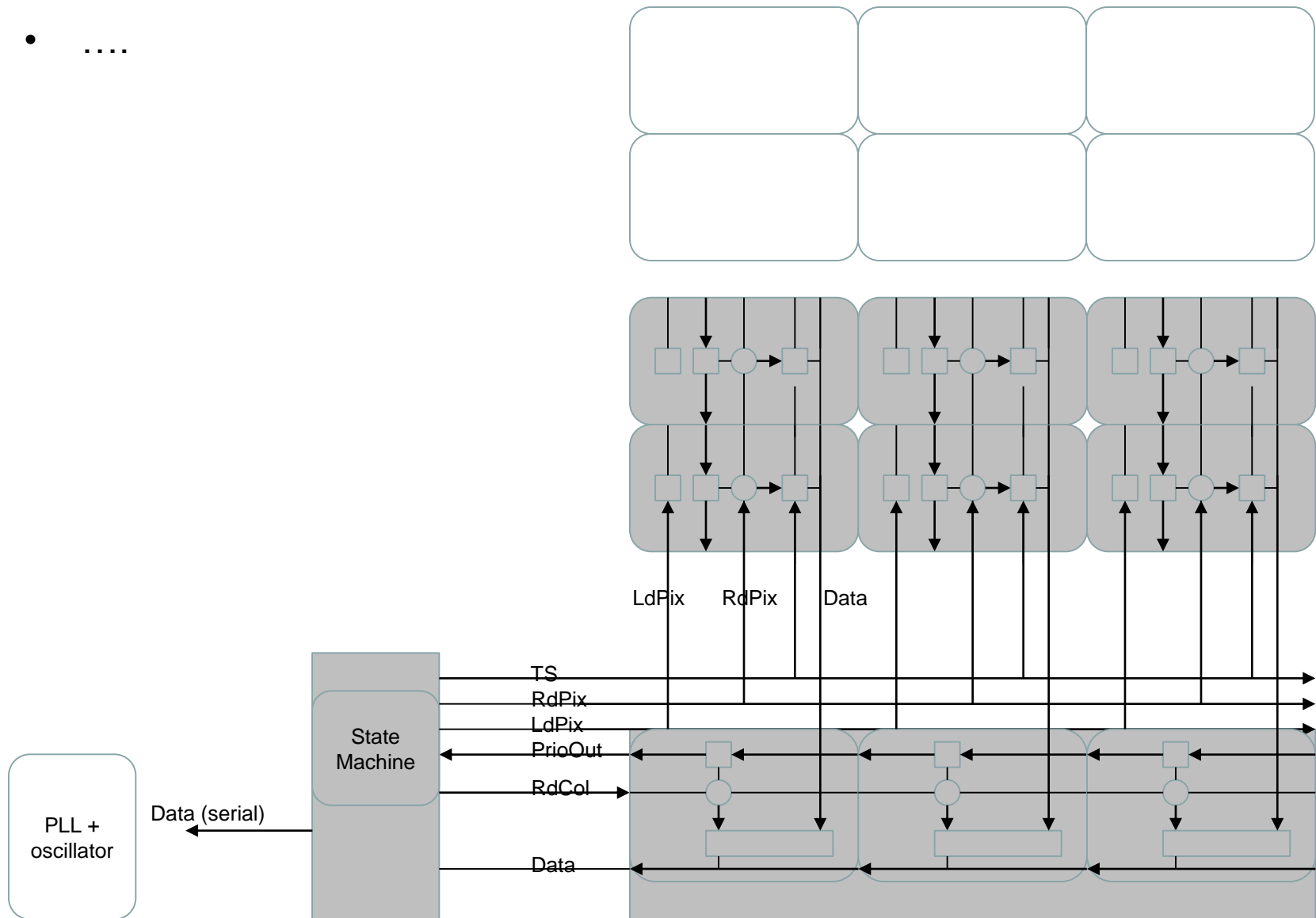
- Two pixel types
- Analog pixels contain only charge sensitive amplifiers and signal driver
- Digital pixels contain additionally comparator with threshold tune DACs. The comparator can be with or without the isolation layer (deep PWELL)



- The outputs of the pixels are connected to the periphery readout-cells.
- In the case of simple readout schemes (Simple ATLASPIX and MuPix) every pixel has a dedicated RO cell. For every pixel there is one long line to the periphery cell that works on the column drain principle. (FEI3 like)
- In the case of M2 design 16 pixels are connected to one buffer block of four trigger buffers. The outputs of 16 pixels are compressed to an 8 bit wide bus. Buffers contain trigger circuit (FEI4 like)



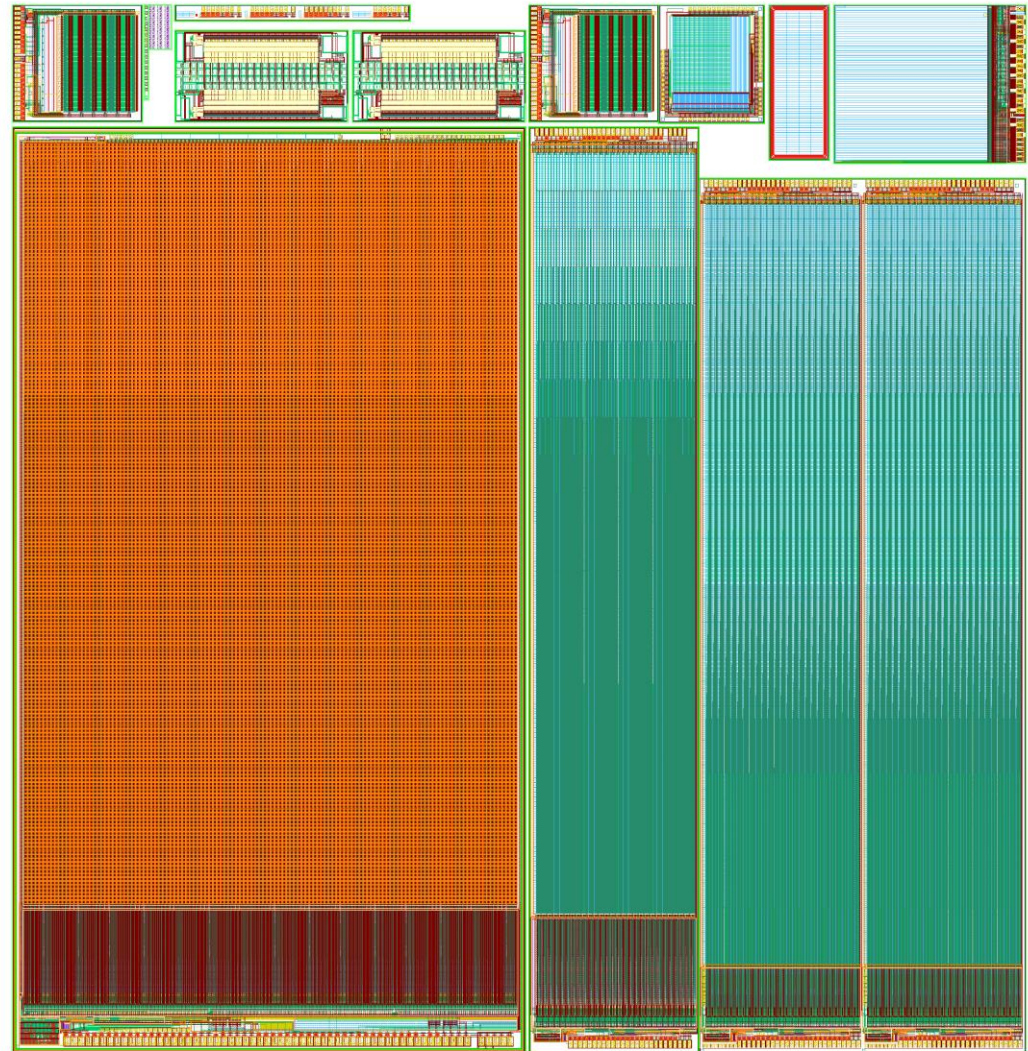
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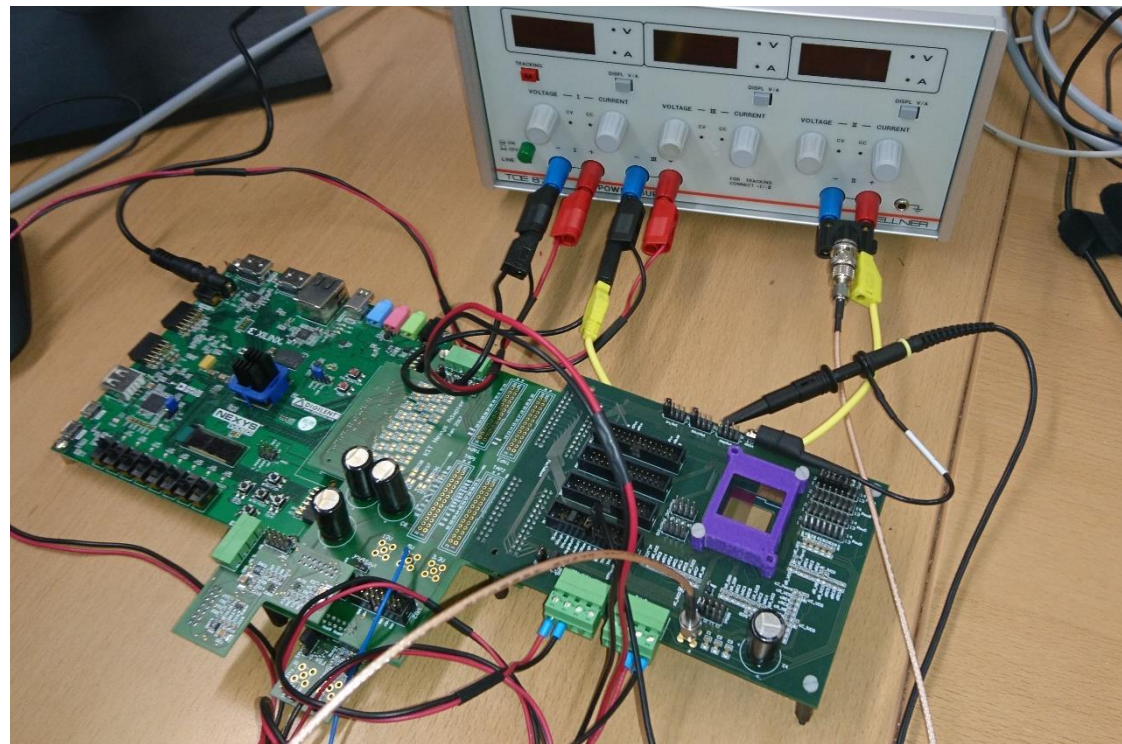


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RO cells at the chip  
periphery, long  
connections are used  
Advantages:  
Smaller digital power  
consumption  
No crosstalk  
No clock in matrix  
Smaller detector  
capacitance  
Disadvantage: larger  
periphery

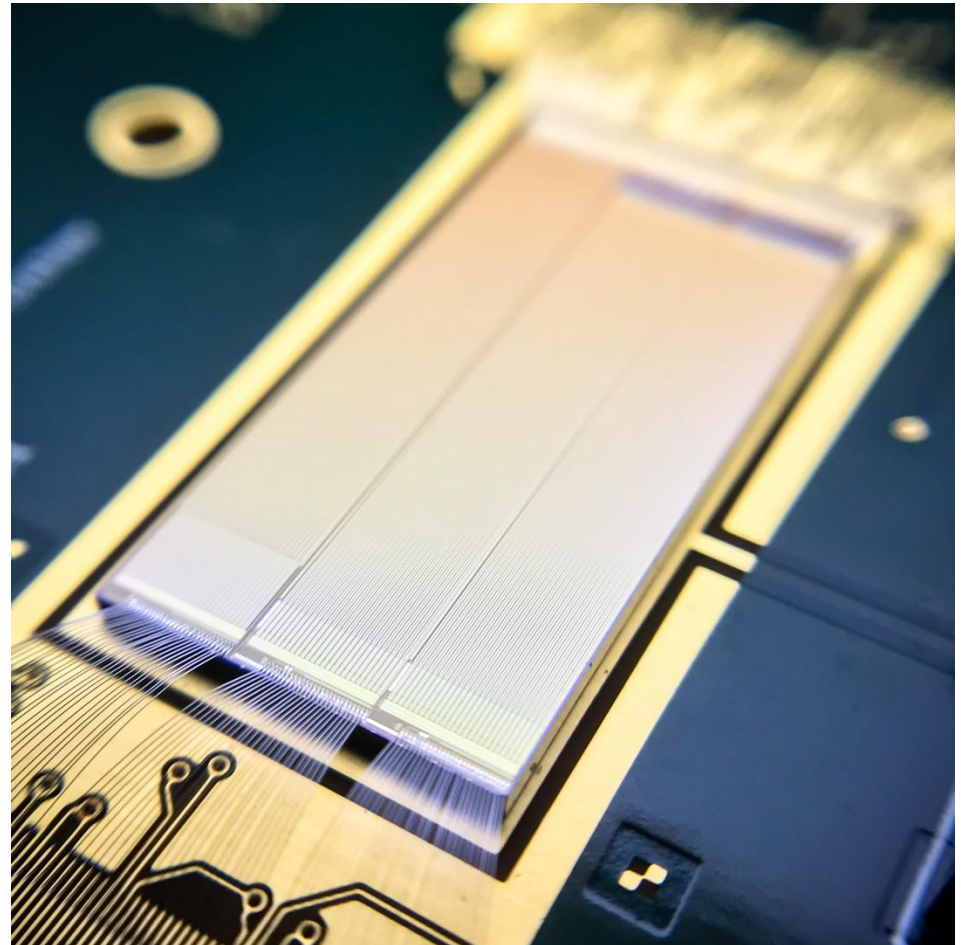


- Since September we are testing the sensors
- New test system

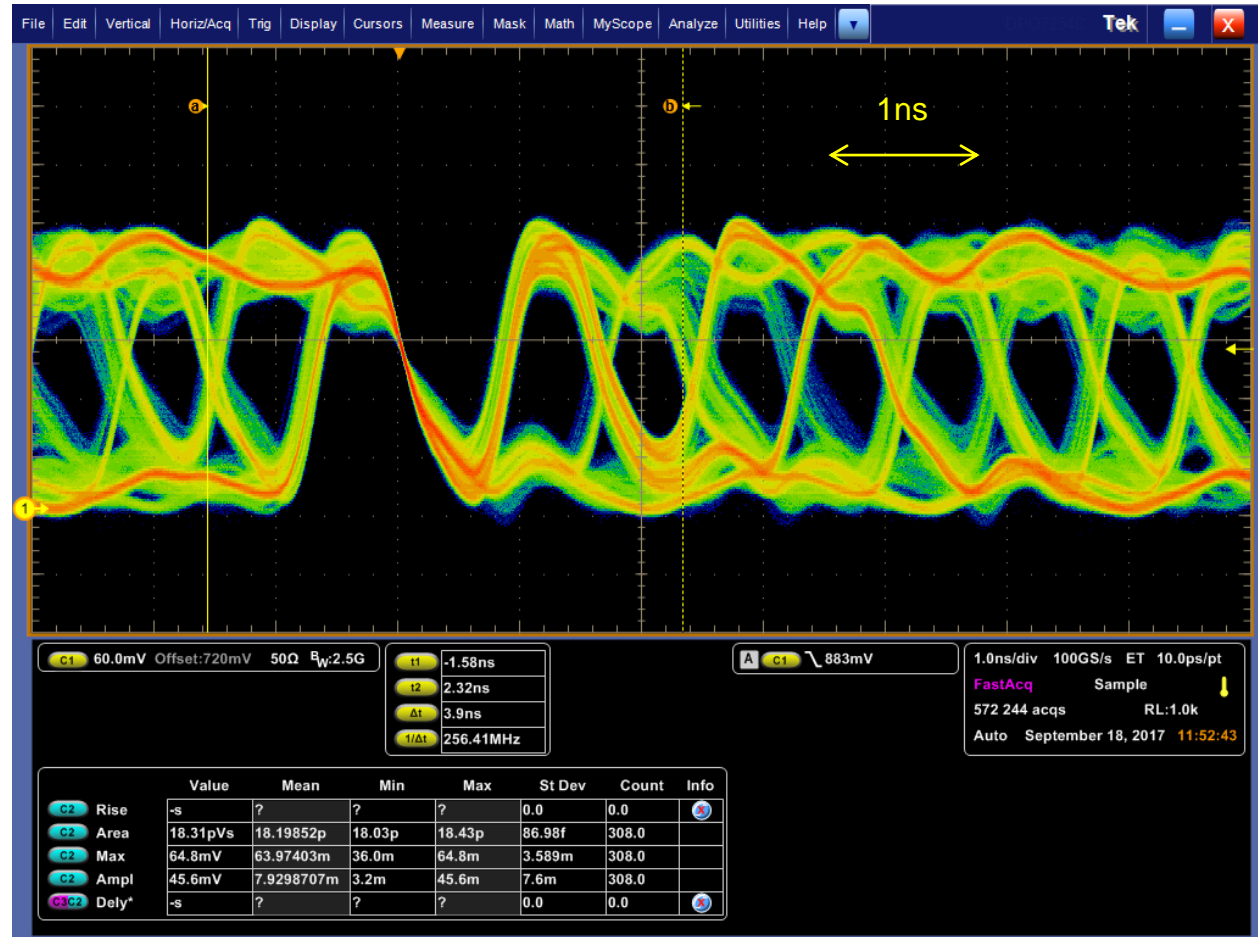




- All circuits of all chips have been tested and are all functional.



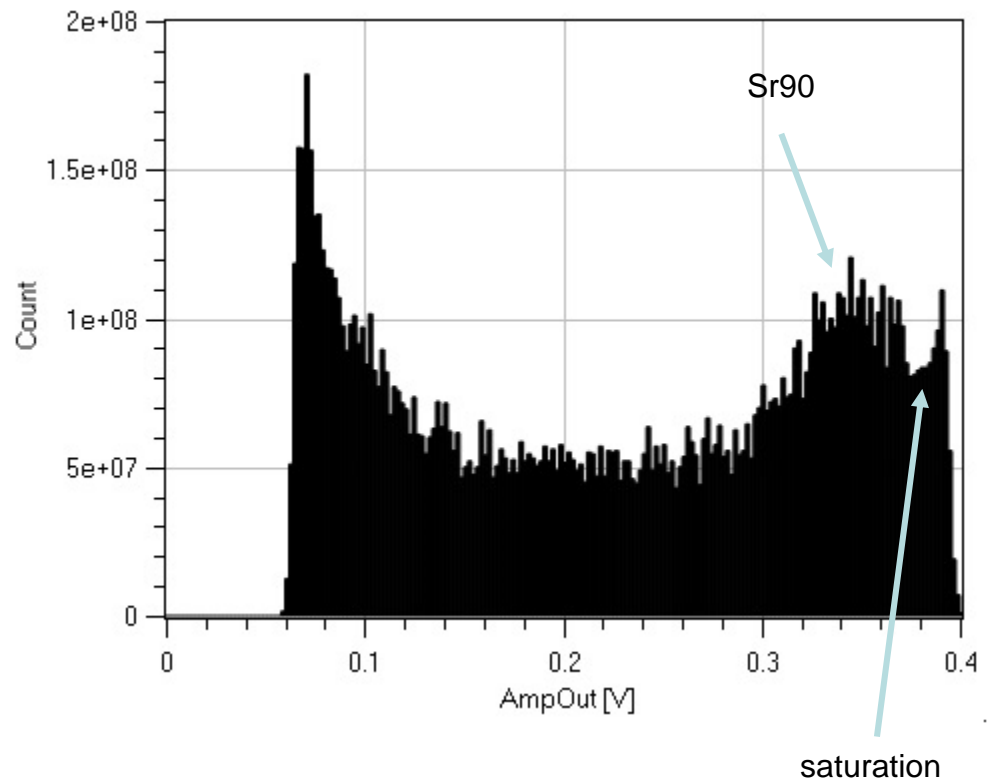
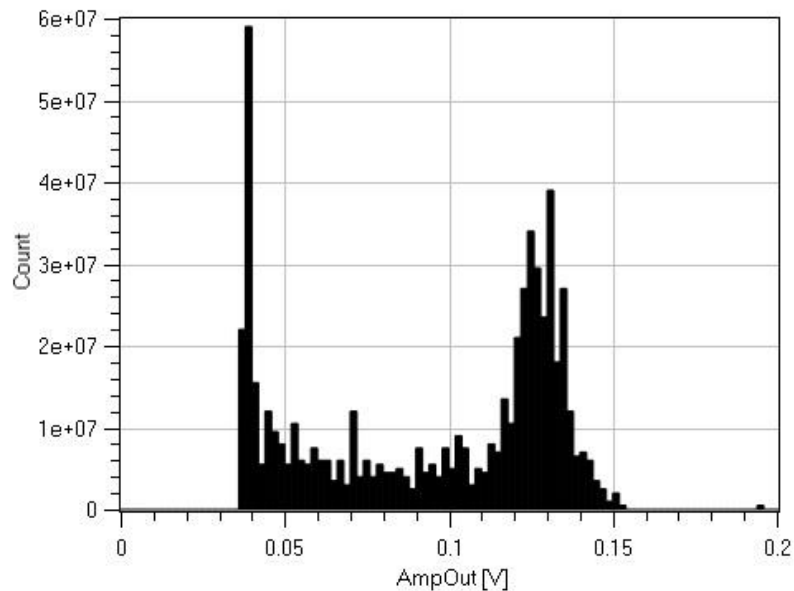
- The readout at 1.2 Gbps was tested. Up to 1.6Gbitps should be possible.



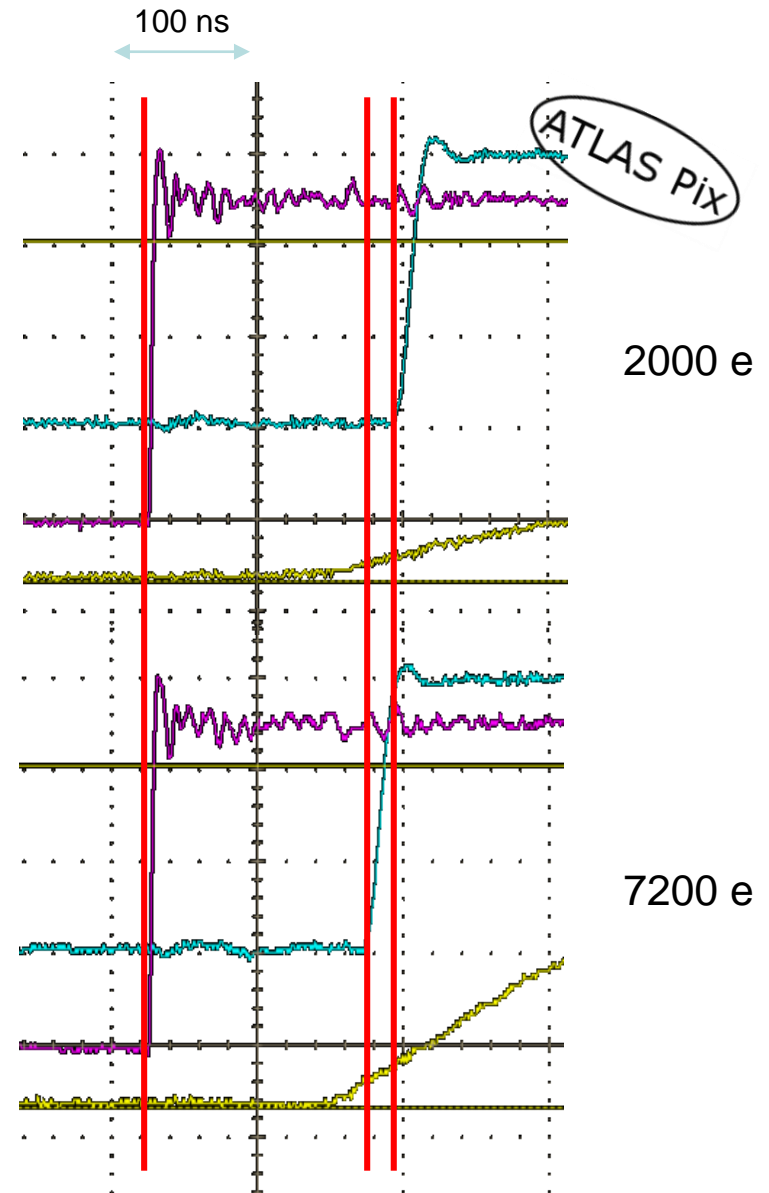
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- $^{55}\text{Fe}$  at 128 mV
  - $^{90}\text{Sr}$  at 348 mV
- (HV = -10 V, 60V possible)



- It is also possible to measure the output of the comparator. In this way, timewalk can be estimated.
- Figure shows the timewalk for ATLASPIX simple design with CMOS comparator
- The signal range was from  $\sim 1/3$  estimated MIP to 1.2MIP

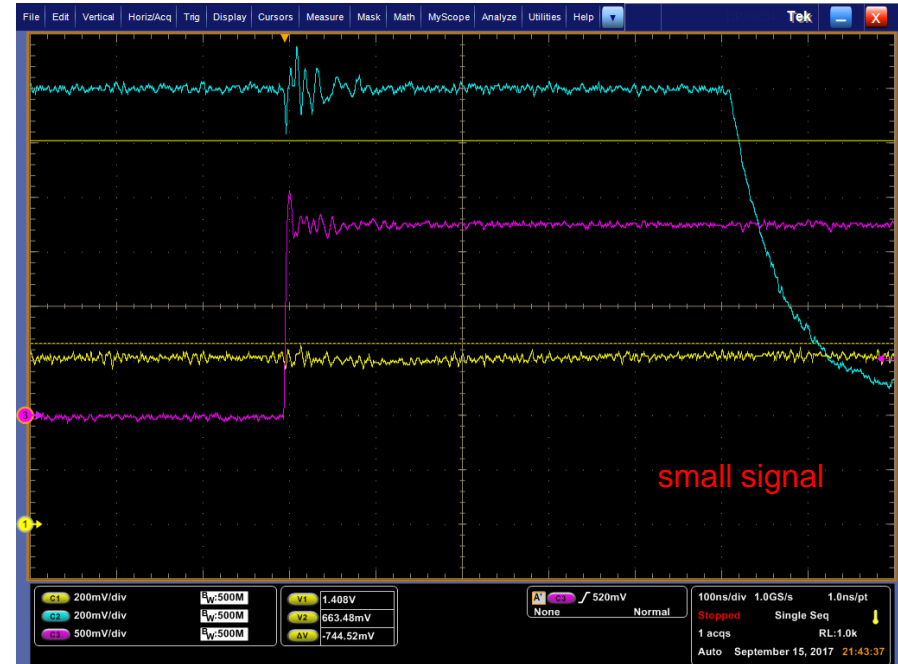
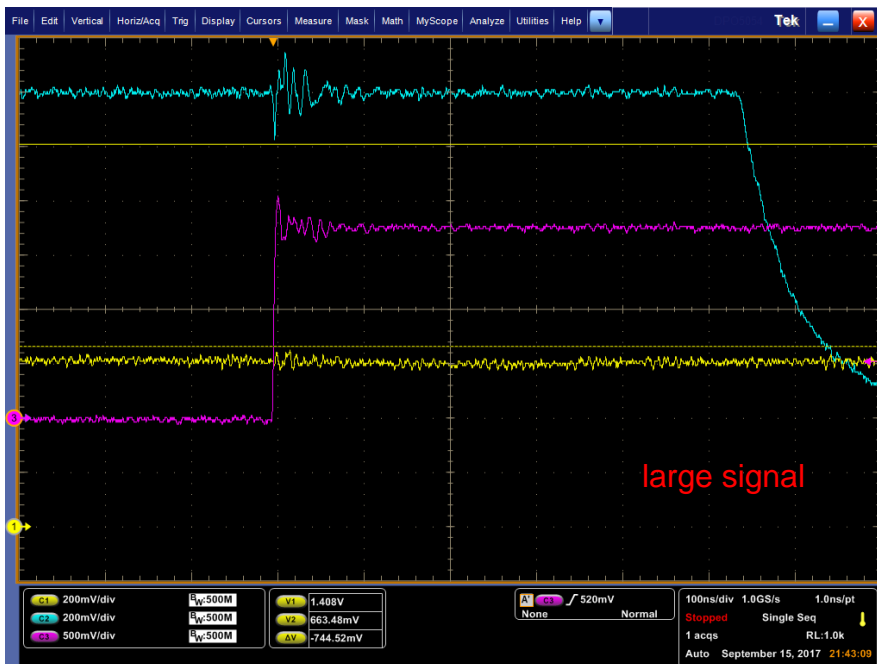


- MuPix
- Low Power consumption:  

$$1.8V \cdot (60mA + 30mA) + 1.1V \cdot 60mA = 228 mW/2cm^2$$

analog
digital
amplifier
- Amplifier power only 30%

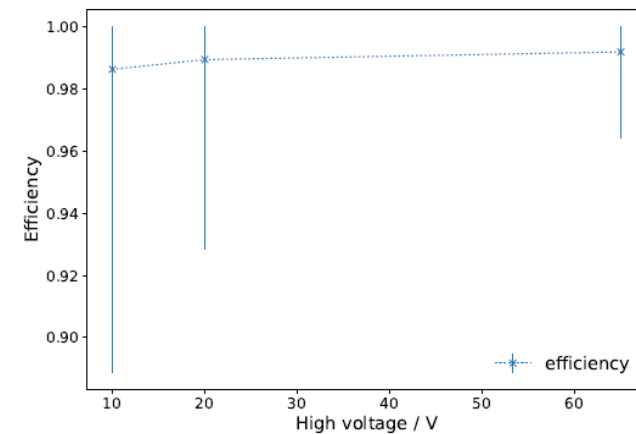
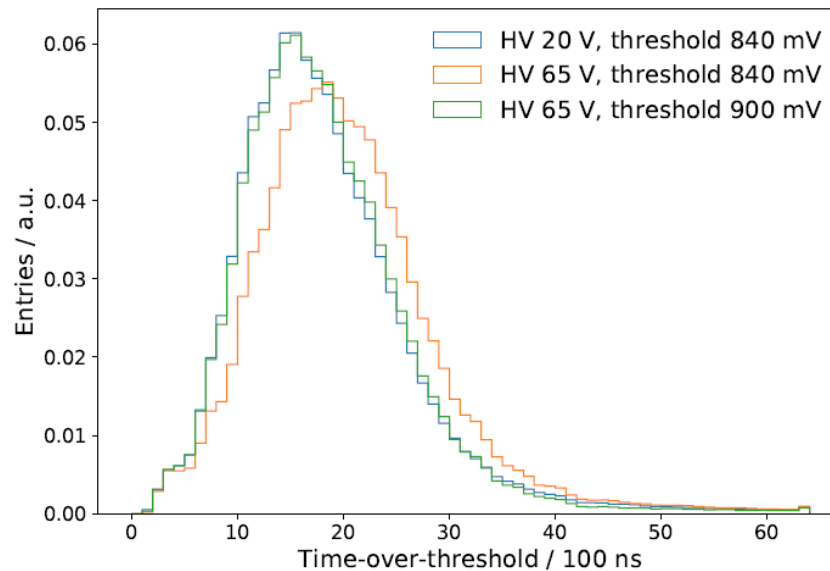
MuPix





- Chips MuPix and ATLASPIX simple have been tested in beam. Full readout chain have been used.

- Detection efficiency of 99% has been measured with ATLASPix and MuPix
- For the results see poster of Moritz Kiehn



- Specifications for ATLAS

Parameter		
Chip size	~19.8mm x 20.6mm	1mm x 2mm (ATLASPix all together)
Chip thickness (μm)	250	So far 750
Pixel size (μm)	50 x 150	From 50 x 60 to 40 x 128
Detector efficiency	>99% in 1 BC	>99% in 3BCs so far
Noise occupancy per pixel	$10^{-6}$	Achieved
Radiation hardness	80 Mrad / $1.5 \times 10^{15}$ $n_{eq}/cm^2$	To be measured
SEU affecting pixel	100 / hour / chip	To be measured
Hit rate	About 10 hits / chip	
Current consumption	240 mA/cm <sup>2</sup> (100 mA/cm <sup>2</sup> )	Achieved

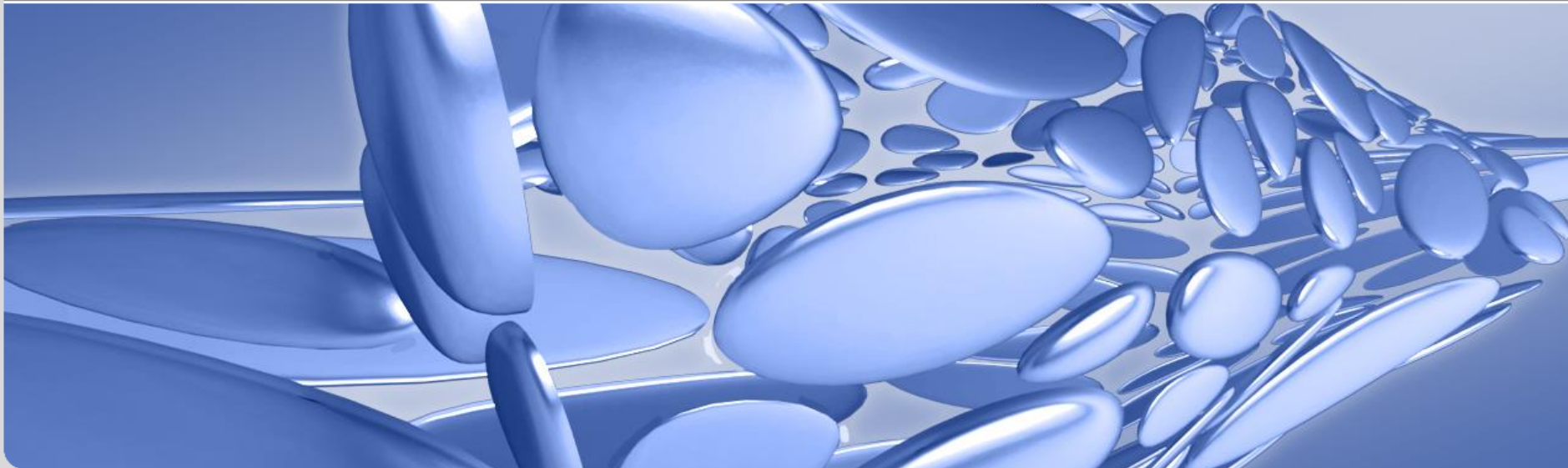
- Large area preproduction HVCMOS sensors have been designed and submitted in AMS aH18 process. The standard technology has been extended by two features – high resistive substrates (80/200 $\Omega$ cm) and deep p-well isolation.
- Pixel sizes are 50 $\mu$ m x 60 $\mu$ m, 40 $\mu$ m x 125 $\mu$ m and 81 $\mu$ m x 80 $\mu$ m. 6 bit ToT and 10 bit time stamps are recorded. Data can be sent digitally at up to 1.6Gbps. One of the designs supports triggered readout with trigger delays of up to 25 $\mu$ s.
- Lab test have been performed. So far only tested the 80  $\Omega$ cm design
- Measured timewalk (single pixels) ~ 20ns, Power consumption ~ 215mW/cm<sup>2</sup>
- Testbeam measurements performed on MuPix and ATLAPix, efficiency > 99% for matrix and full readout
- All features on all sensors are functional
- We are planning 2 x 2 cm large designs for ATLAS and Mu3e. The ATLAS design should be used to make a quad module. The chip periphery will be extended by hit sorting, command decoder, JTAG. Serial powering will be implemented

- Thank you!

- Backup slides

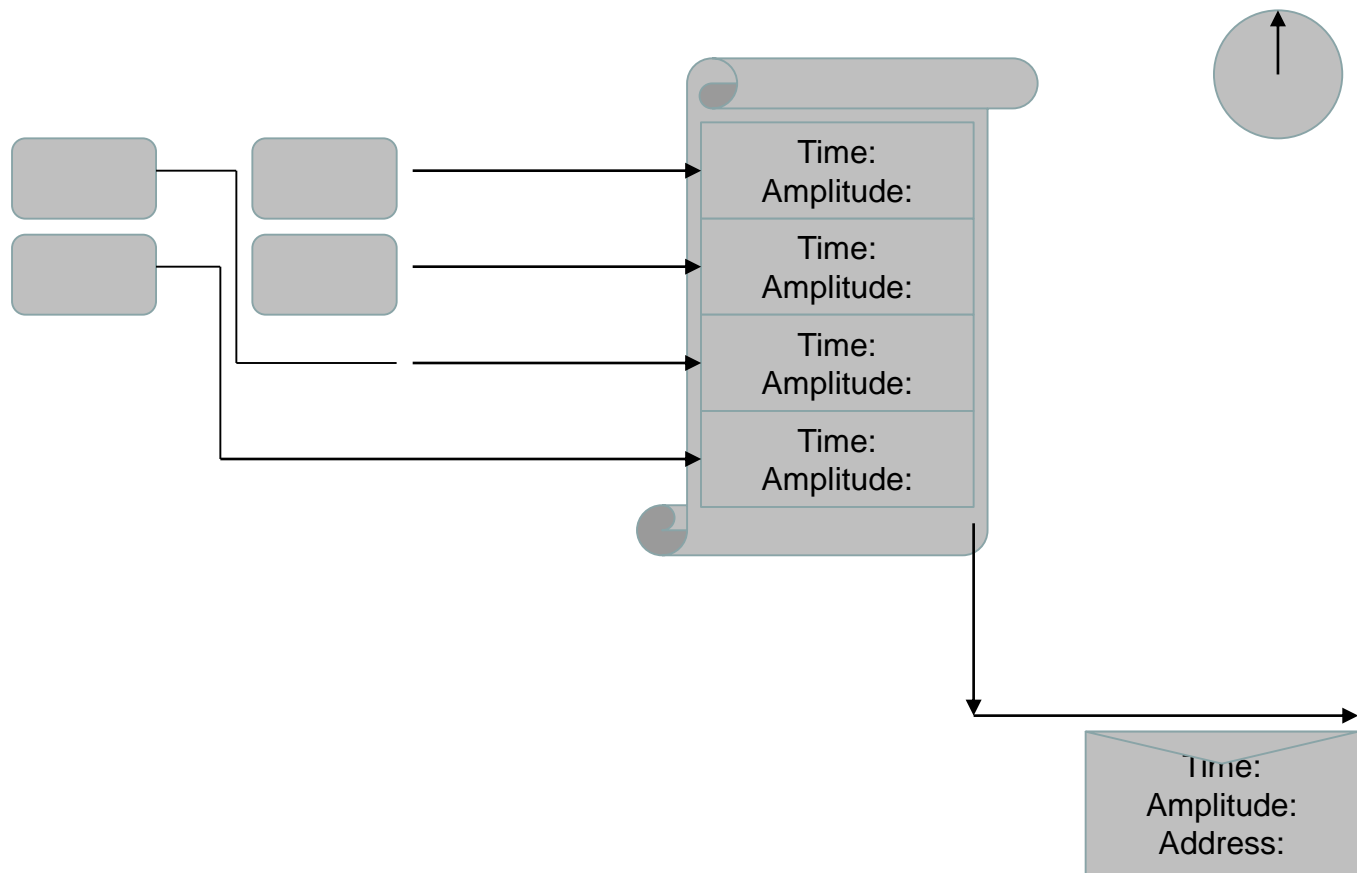
- The RO cell contains the core circuit that contains two hit flags, address ROM, timestamp and time over threshold RAM and a priority circuit.
- The pixel signal generates the pulse at the output of the charge sensitive amplifier. The output voltage is continuously reset. The pulse is connected to the comparator that is for ATLASPIX in the pixel itself and for MuPix in the RO cell. The output of the comparator is the pulse whose rising edge is coincident with the particle hit and width proportional with the charge amount.
- The pulse sets the first hit flag. The second one is set synchronously with a clock LDPIX. Periphery starts the readout by issuing a signal RD. The priority circuit will mark the first hit flag in the column. Only the marked cell will process the RD and put its data on the bus. Falling RD edge deletes the flags. In this way the data are transferred to the end of column cells. The same type of readout is used to transfer the data from EOCs to the digital part.
- The data format is 10 bit timestamp, 6 bit time over threshold and 16 bits row and columns addresses.
- The digital block contains a state machine that controls the readout. The state machine issues LDPIX and reads the data from RO cells to EOC and from EOC as long as the RO cells are empty. The data are formatted 8b10b and serialized with 1.6GBps.
- The chip contains PLL with input clock of 160MHz. Transmission of one hit takes 25ns/link.

## Readout types

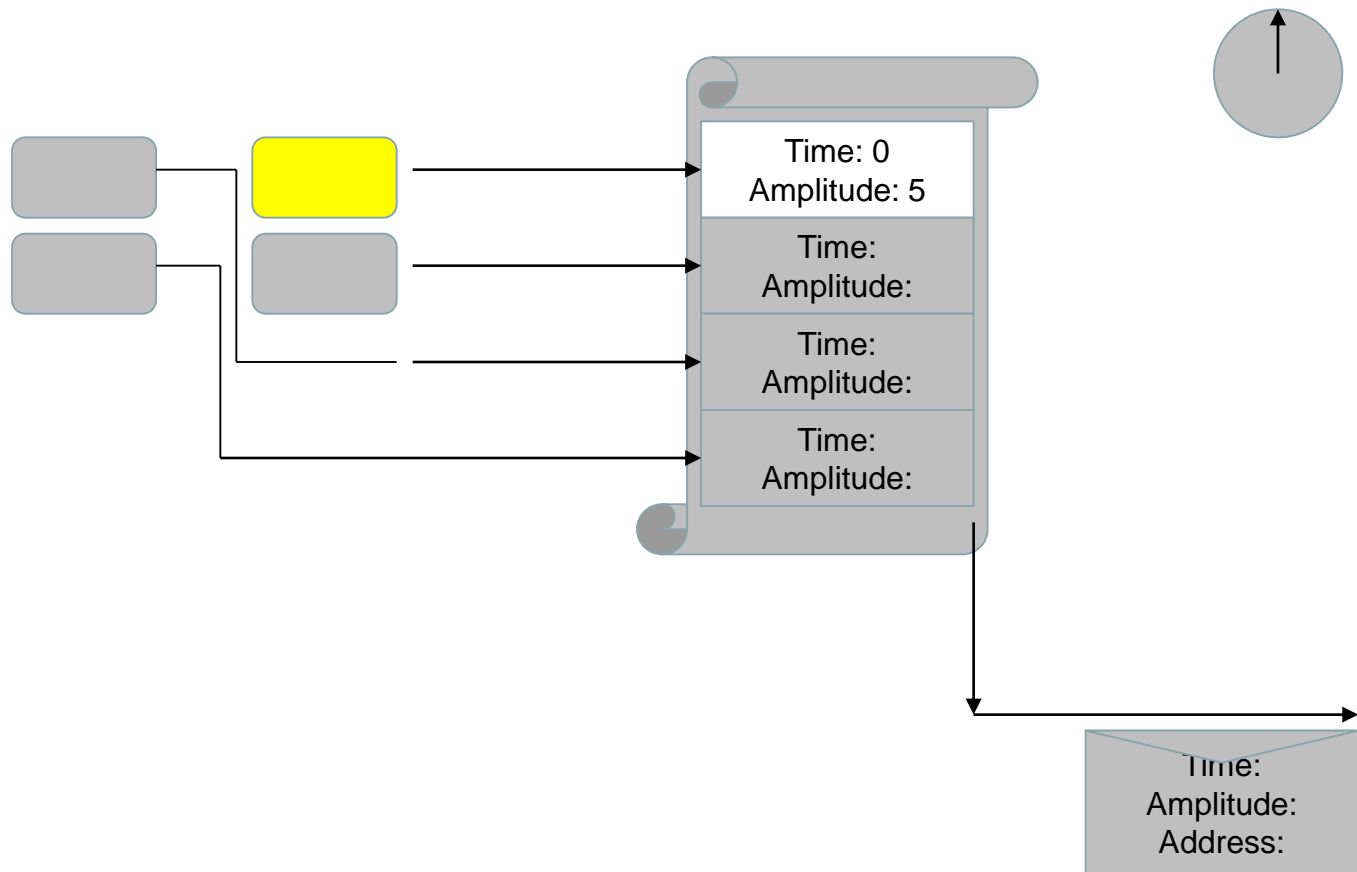




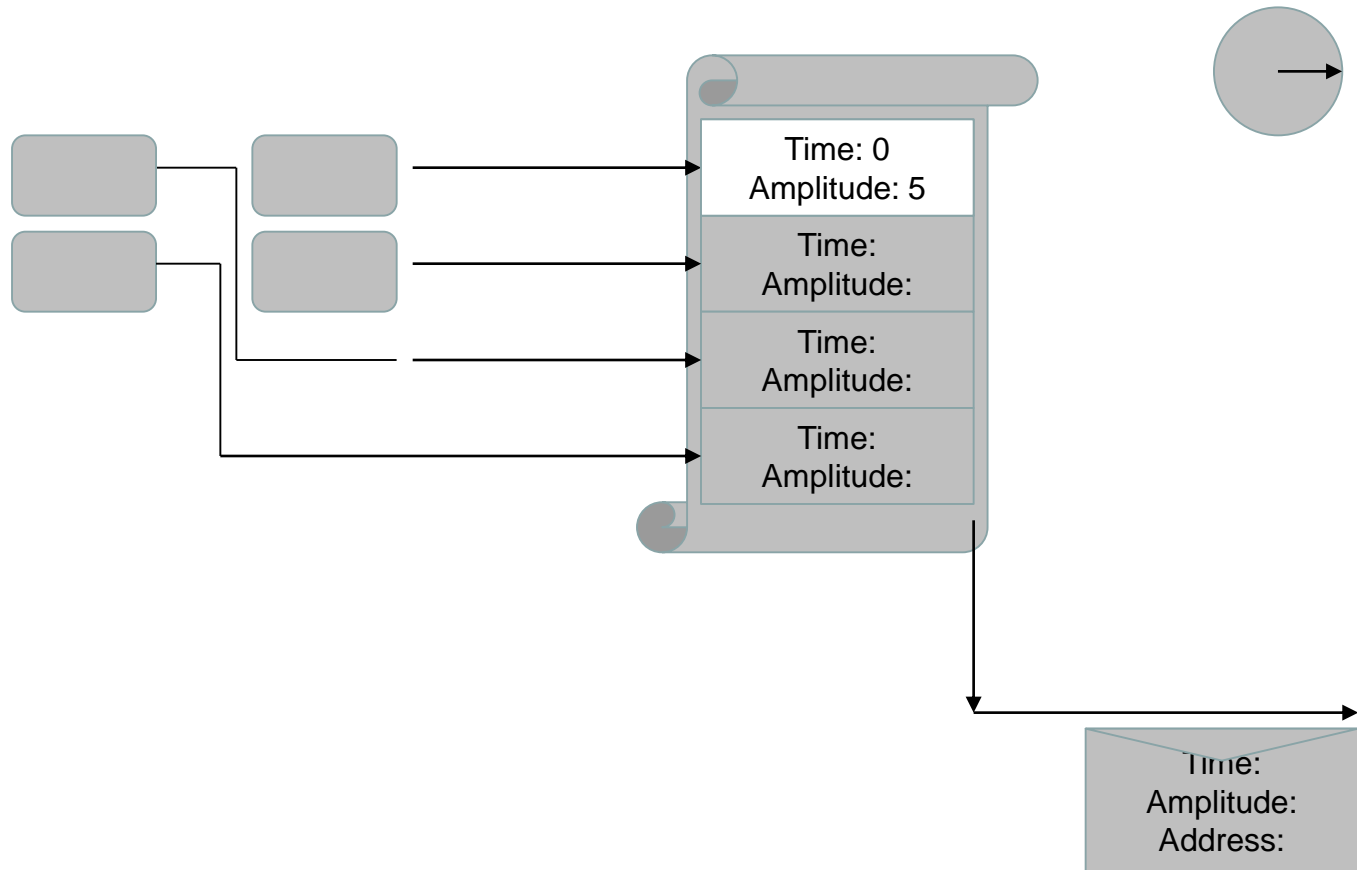
- Hit driven, triggerless, readout (MuPix8, Simple ATLASPix)



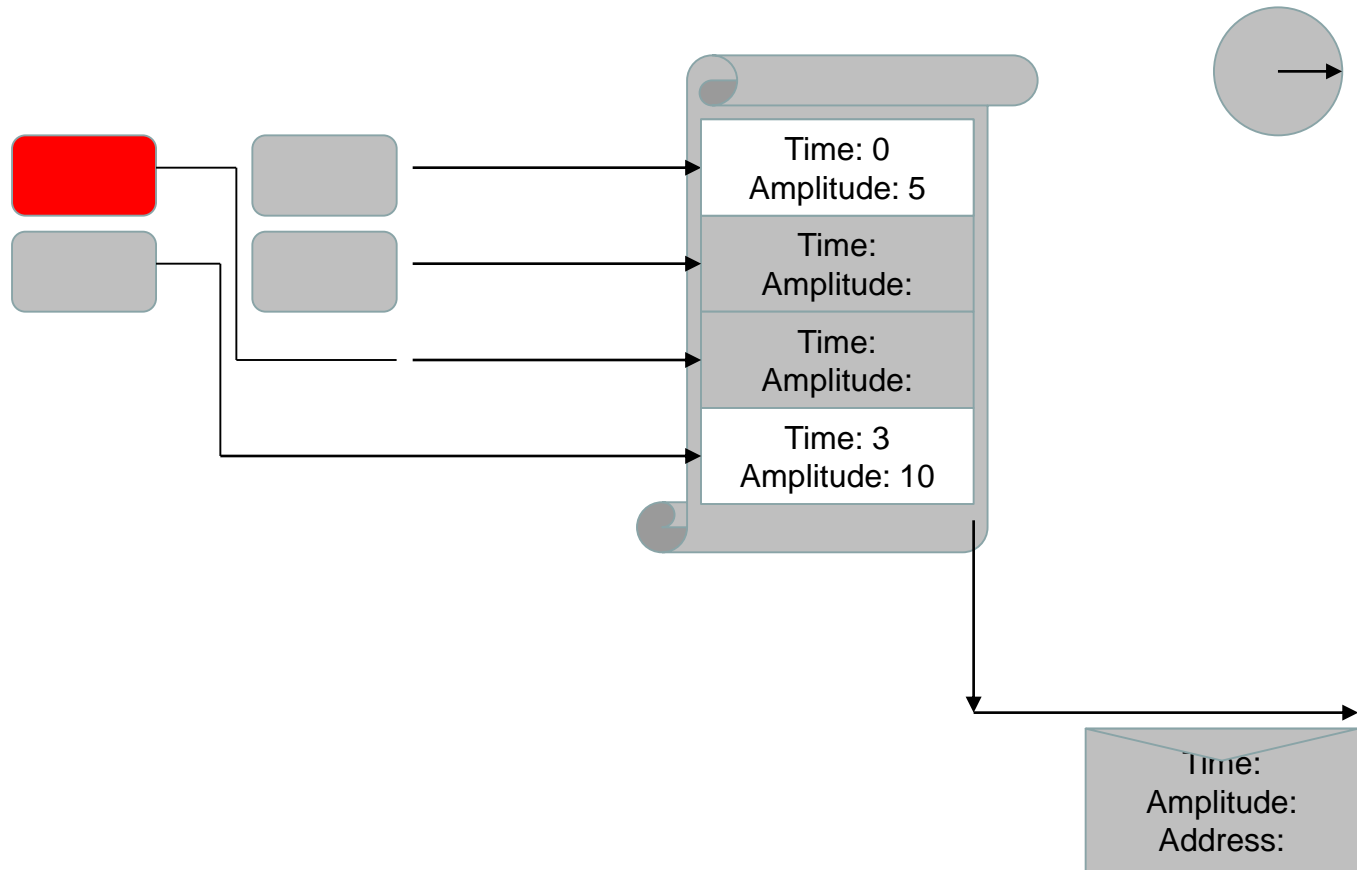
- Hit driven, triggerless, readout



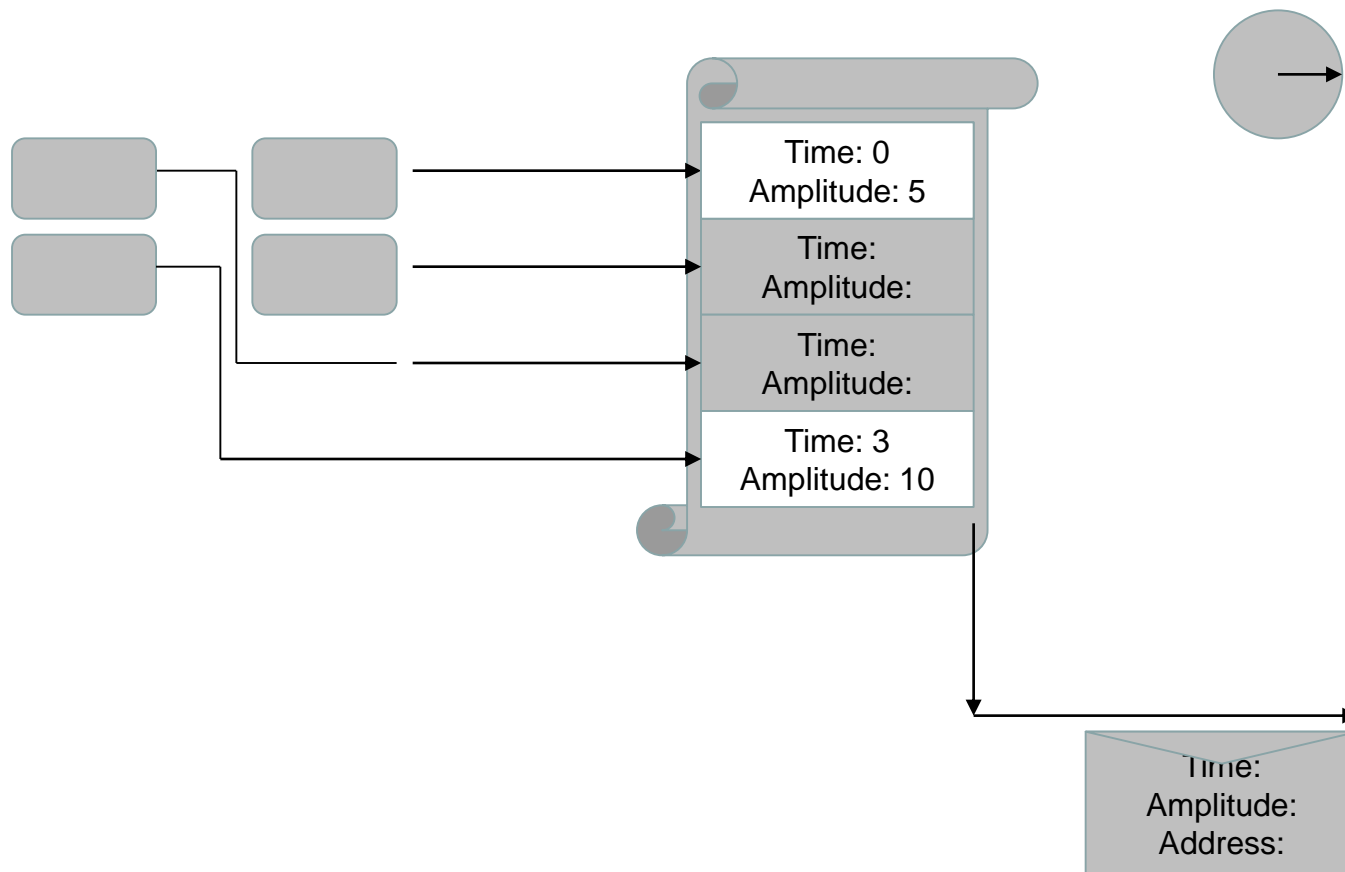
- Hit driven, triggerless, readout



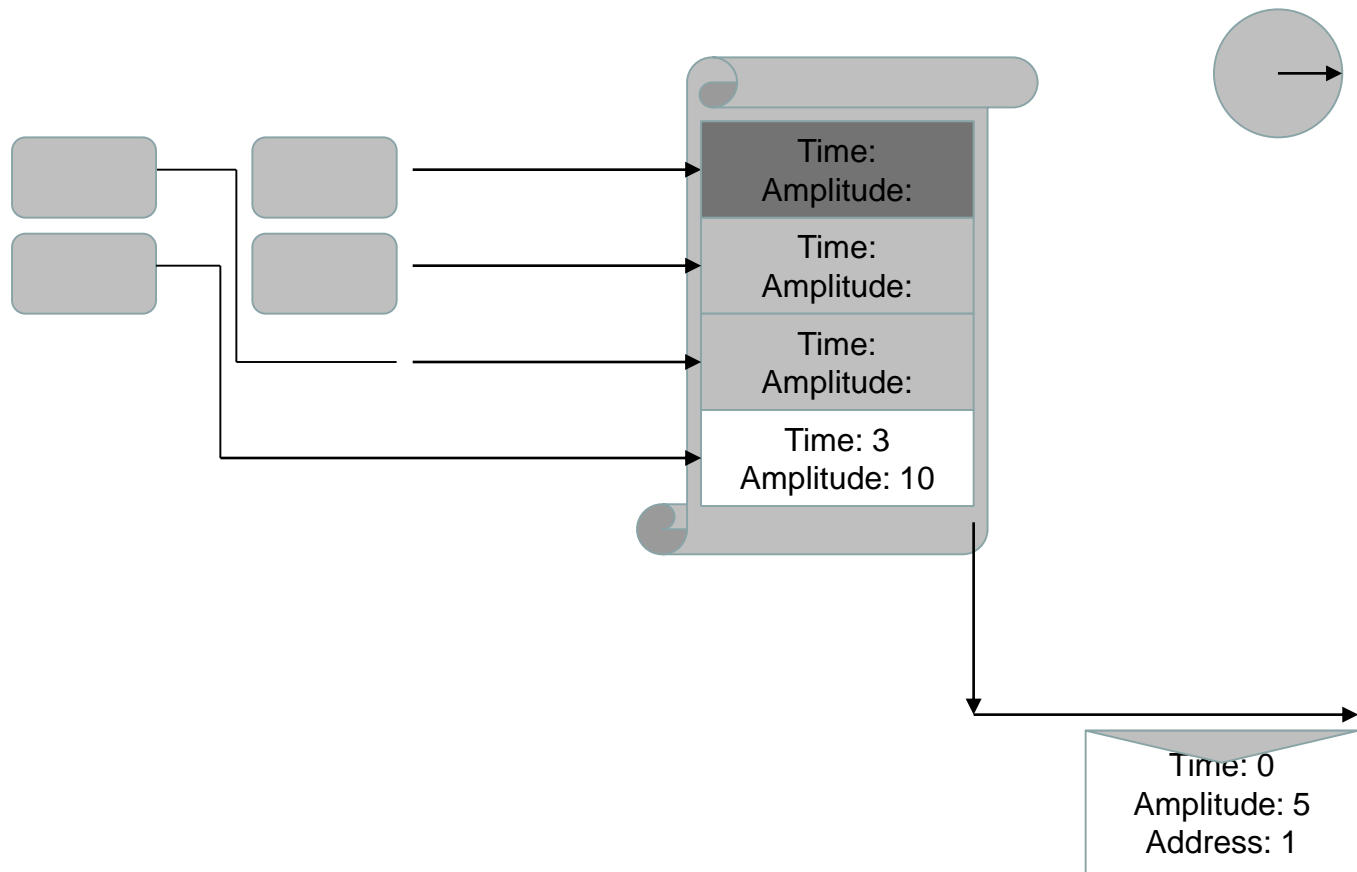
- Hit driven, triggerless, readout



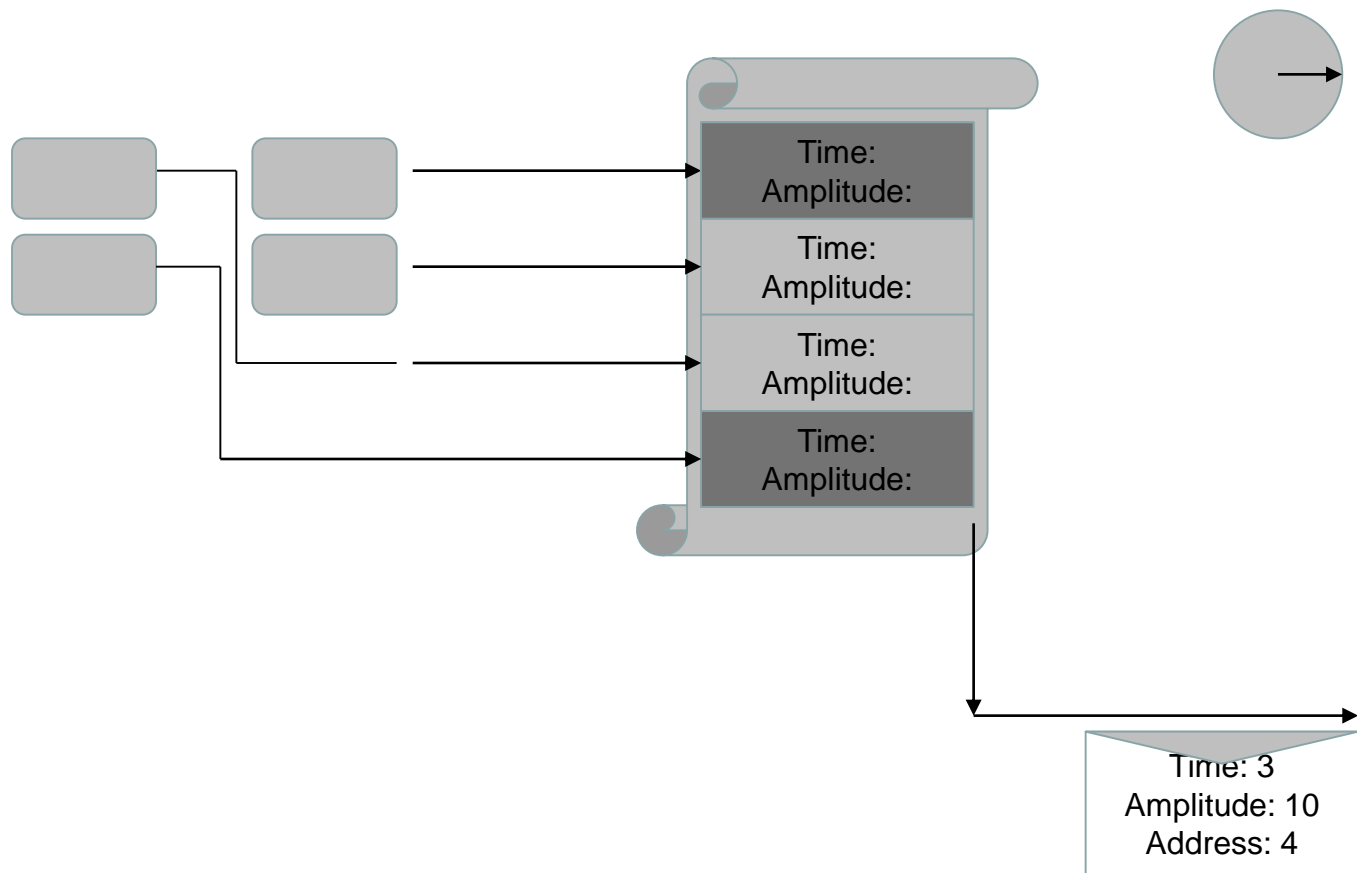
- Hit driven, triggerless, readout



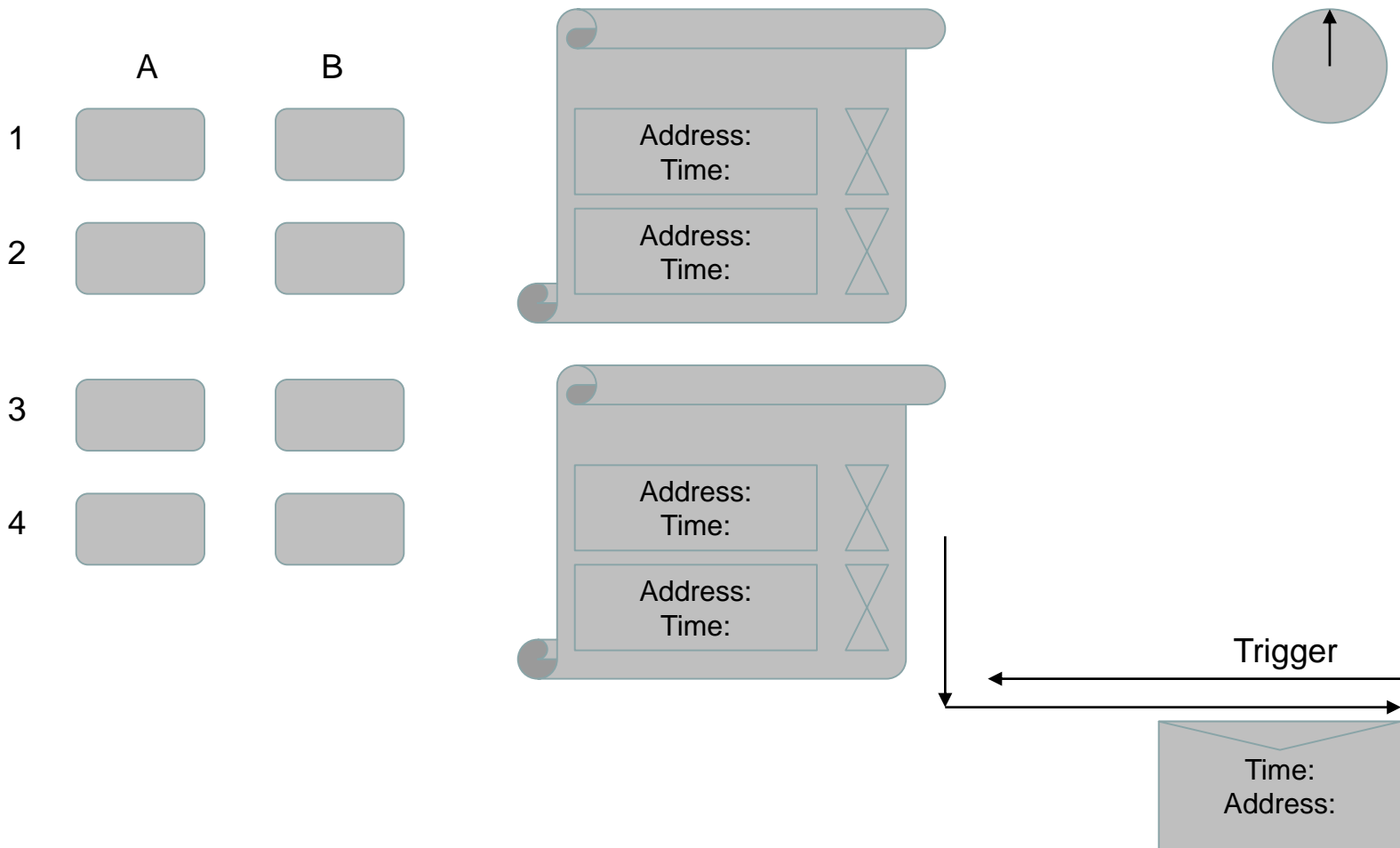
- Hit driven, triggerless, readout



- Hit driven, triggerless, readout

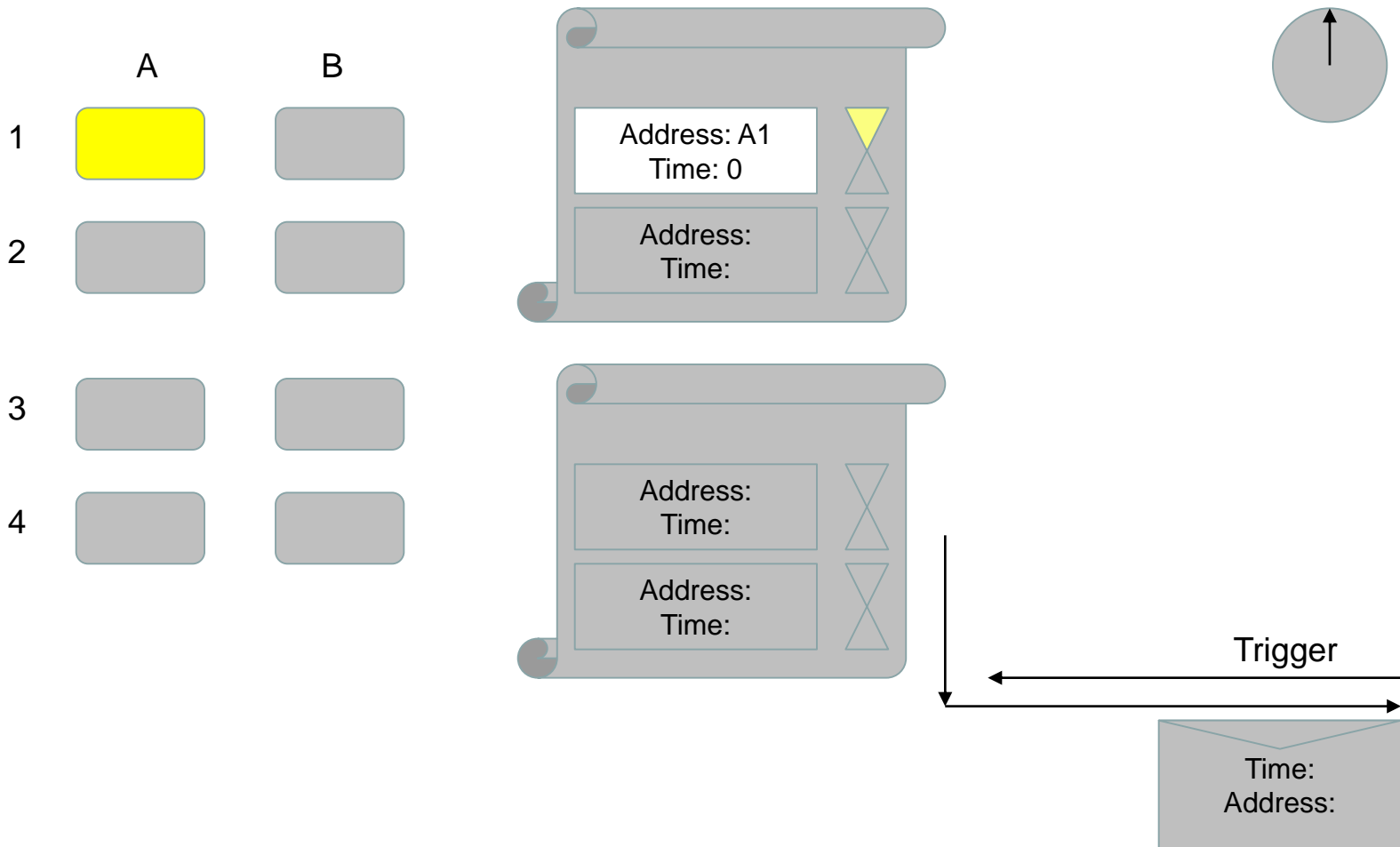


- Triggered readout (M ALTASPix)

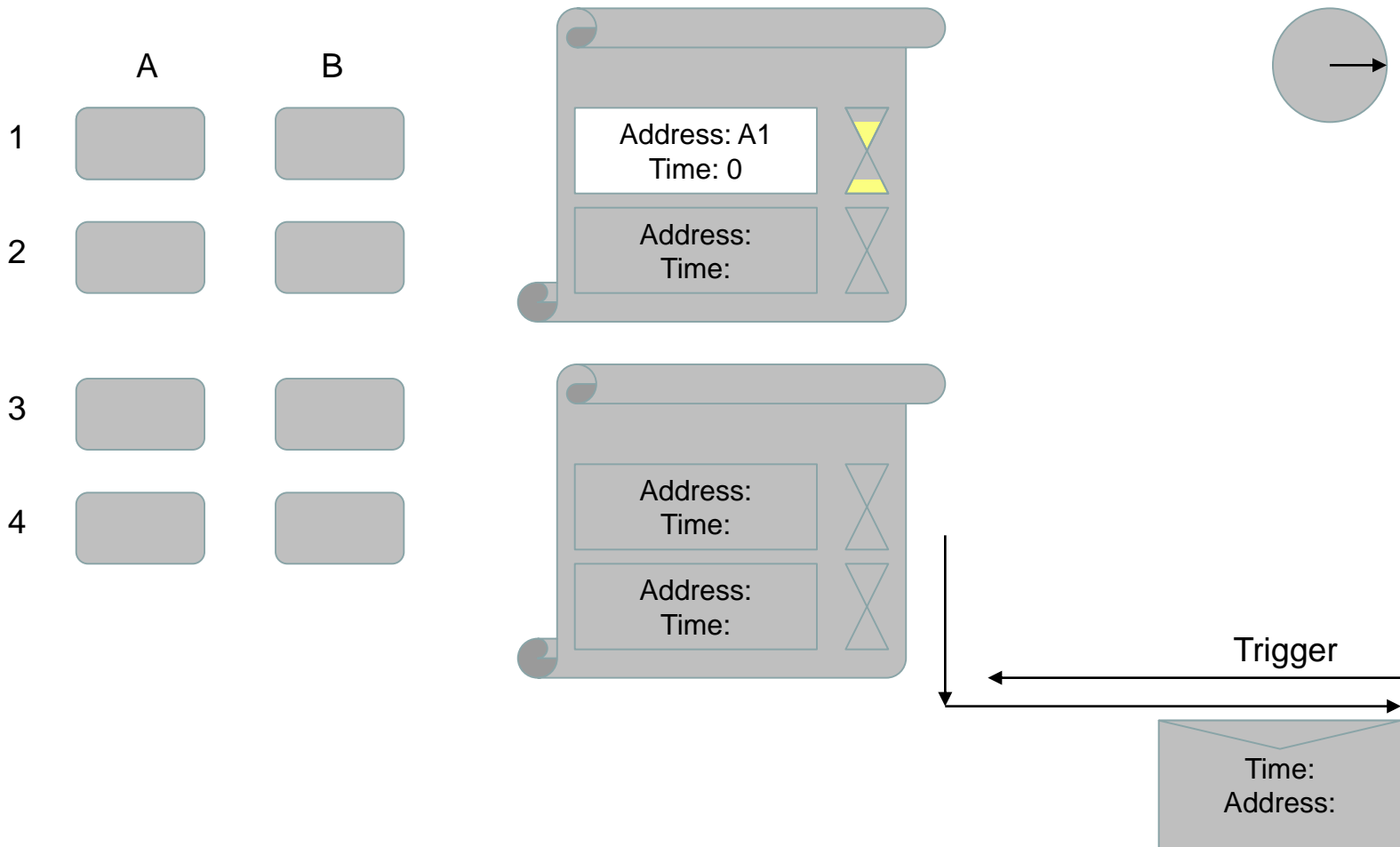




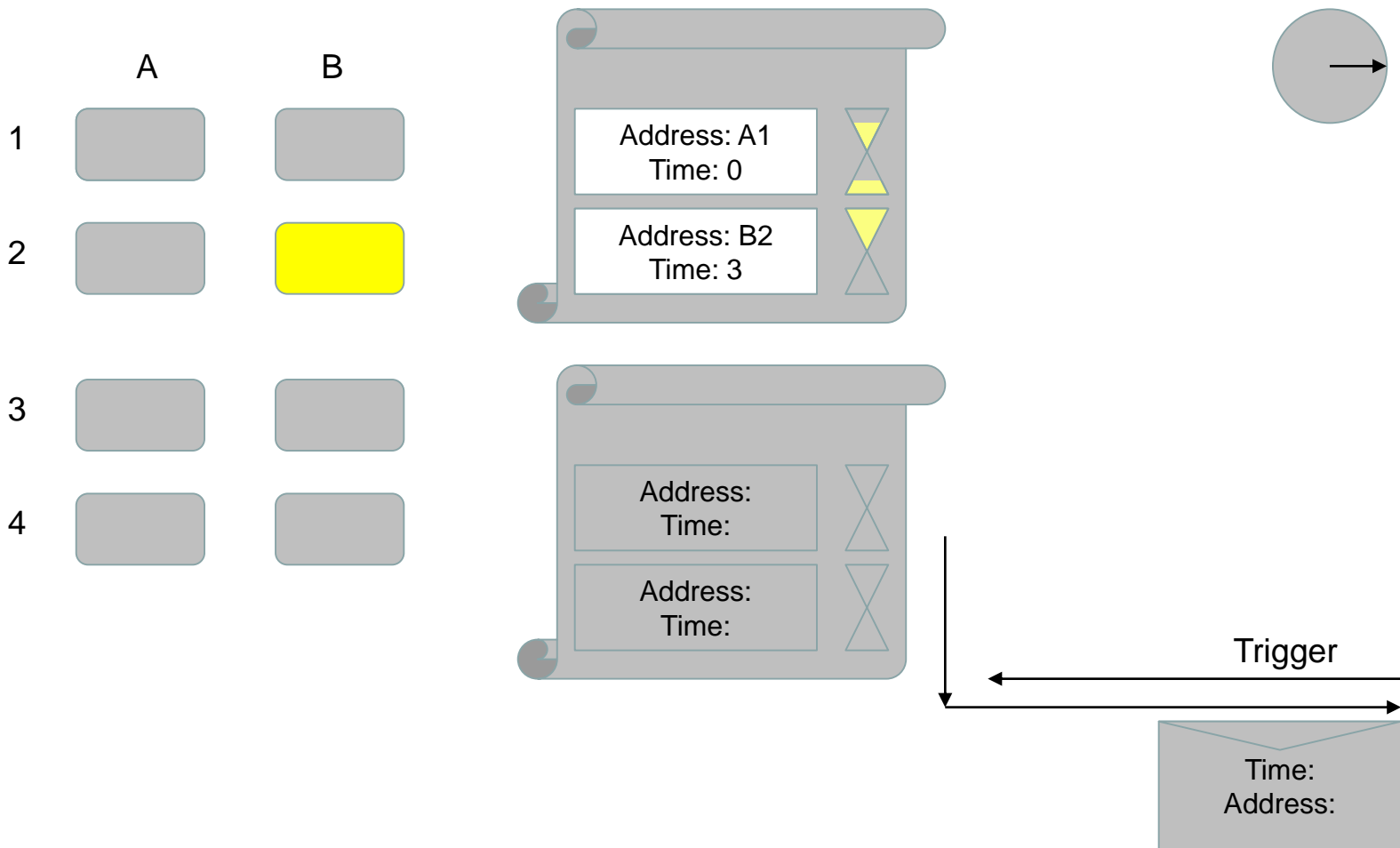
- Triggered readout



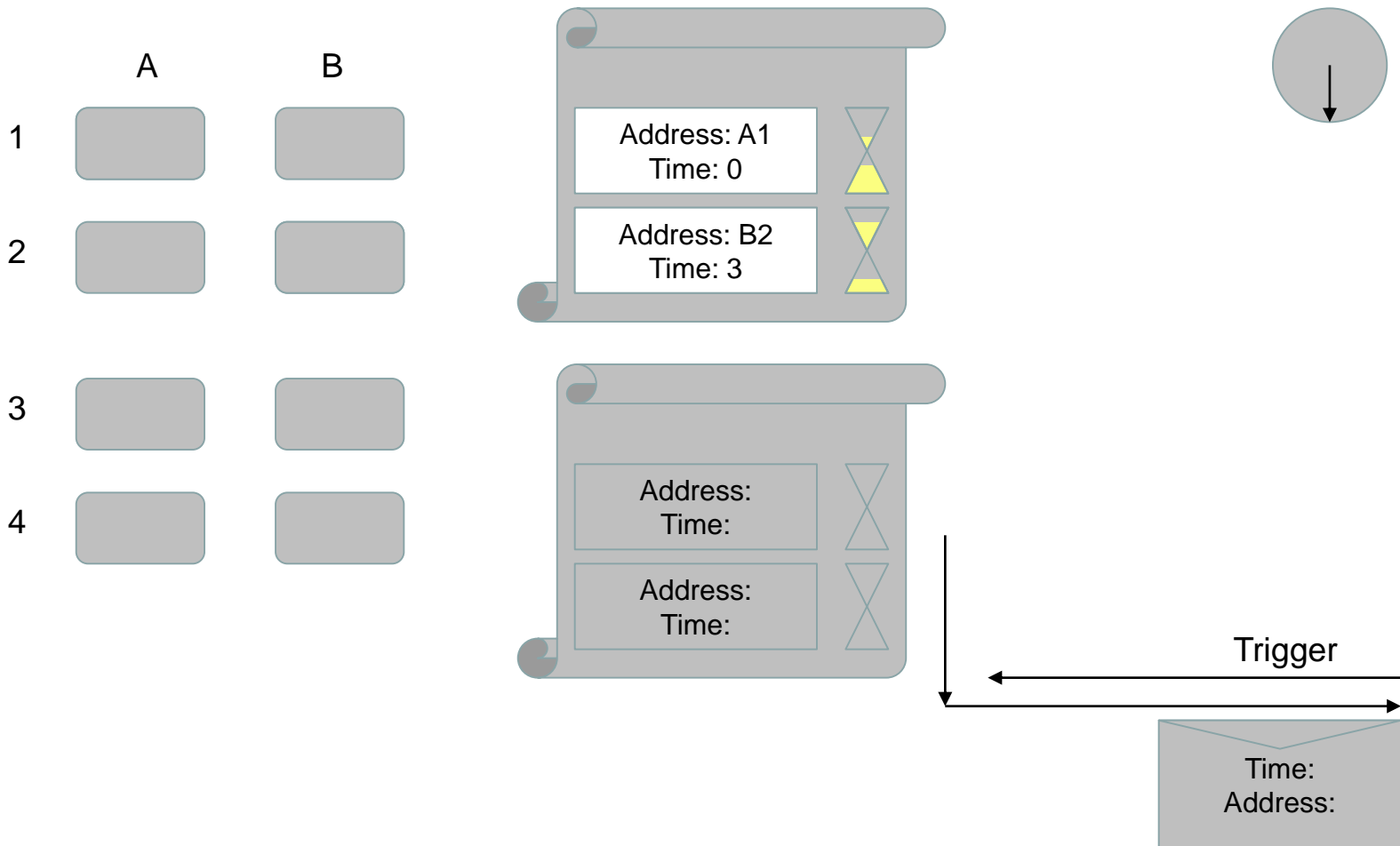
- Triggered readout



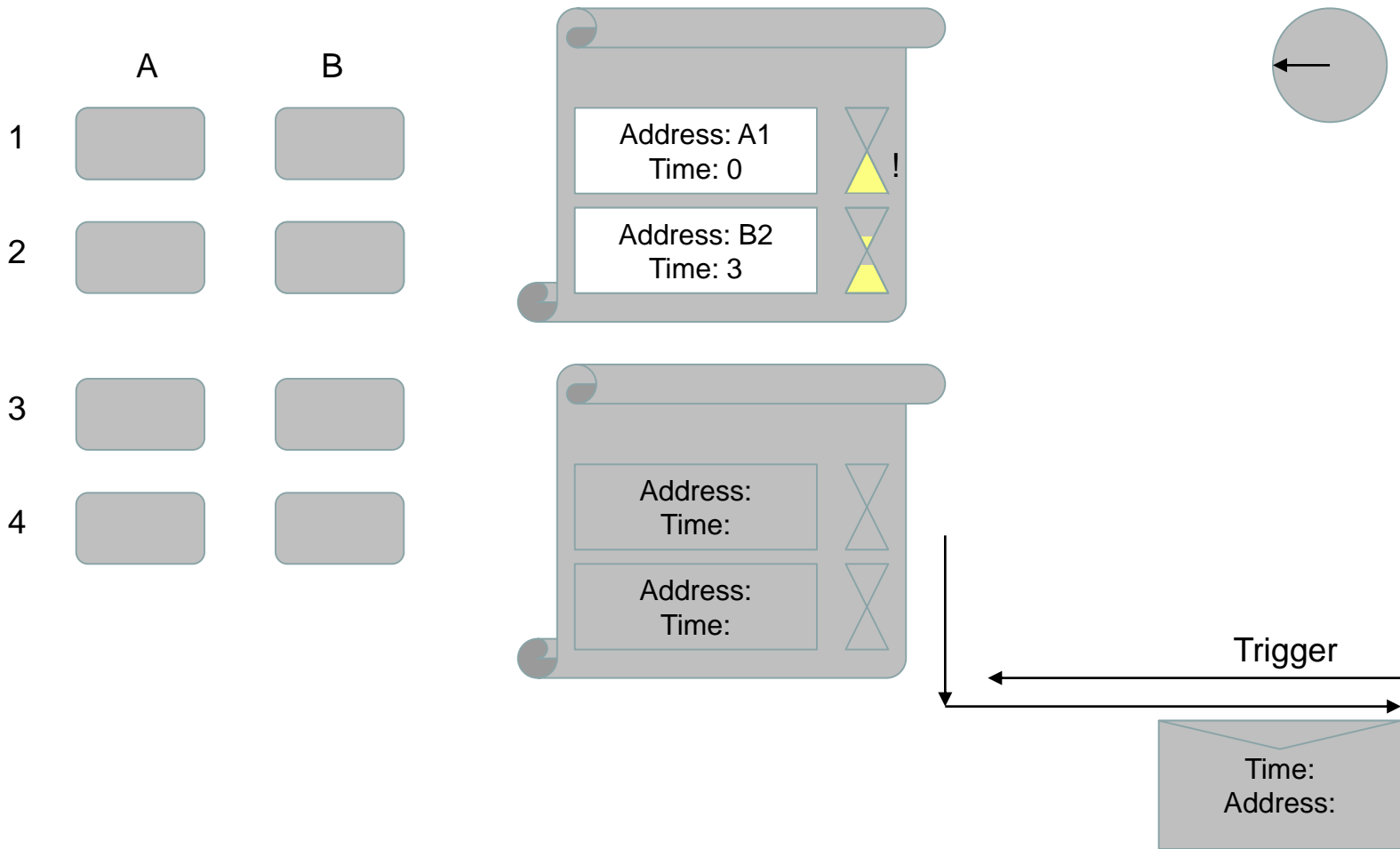
- Triggered readout



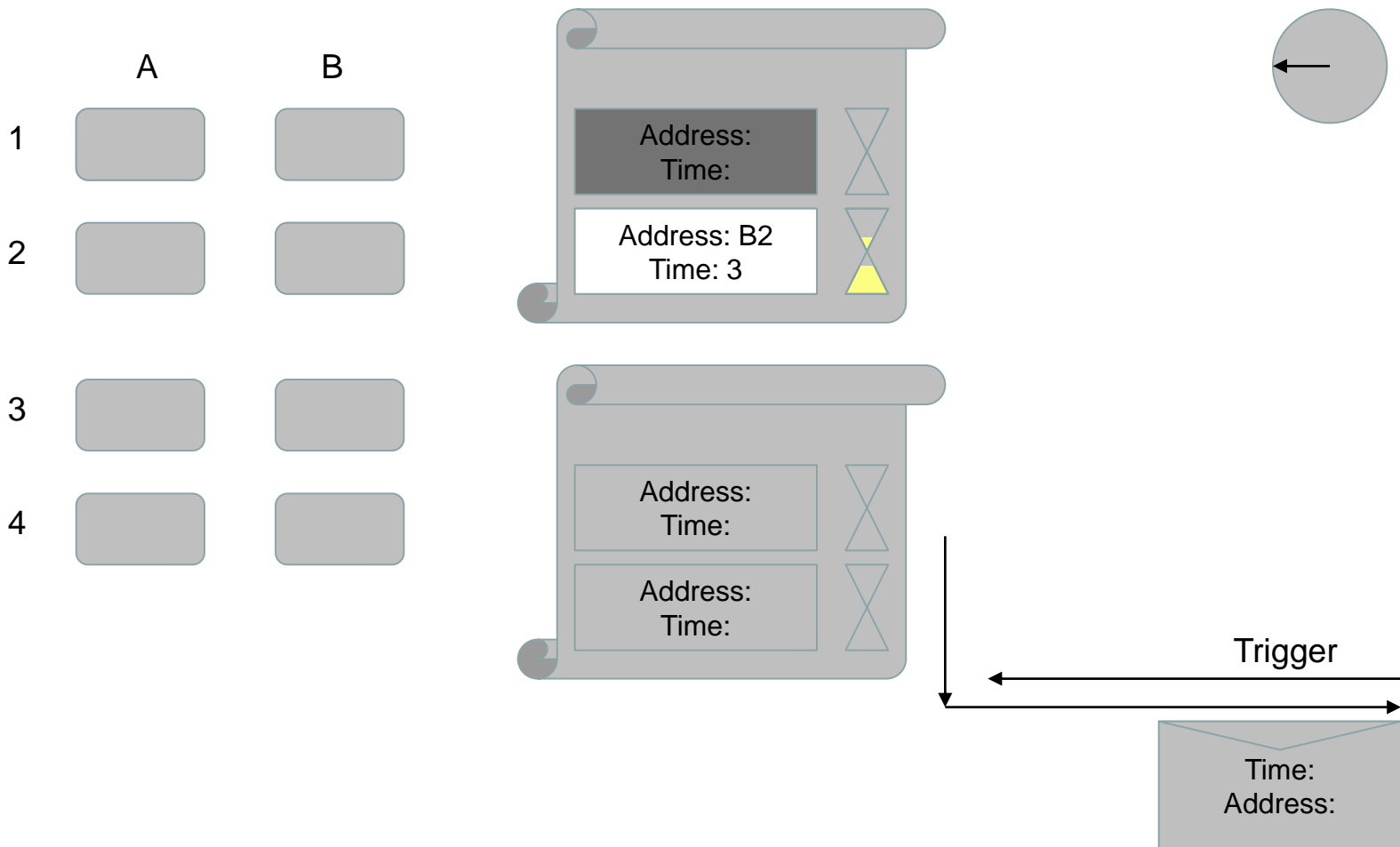
- Triggered readout



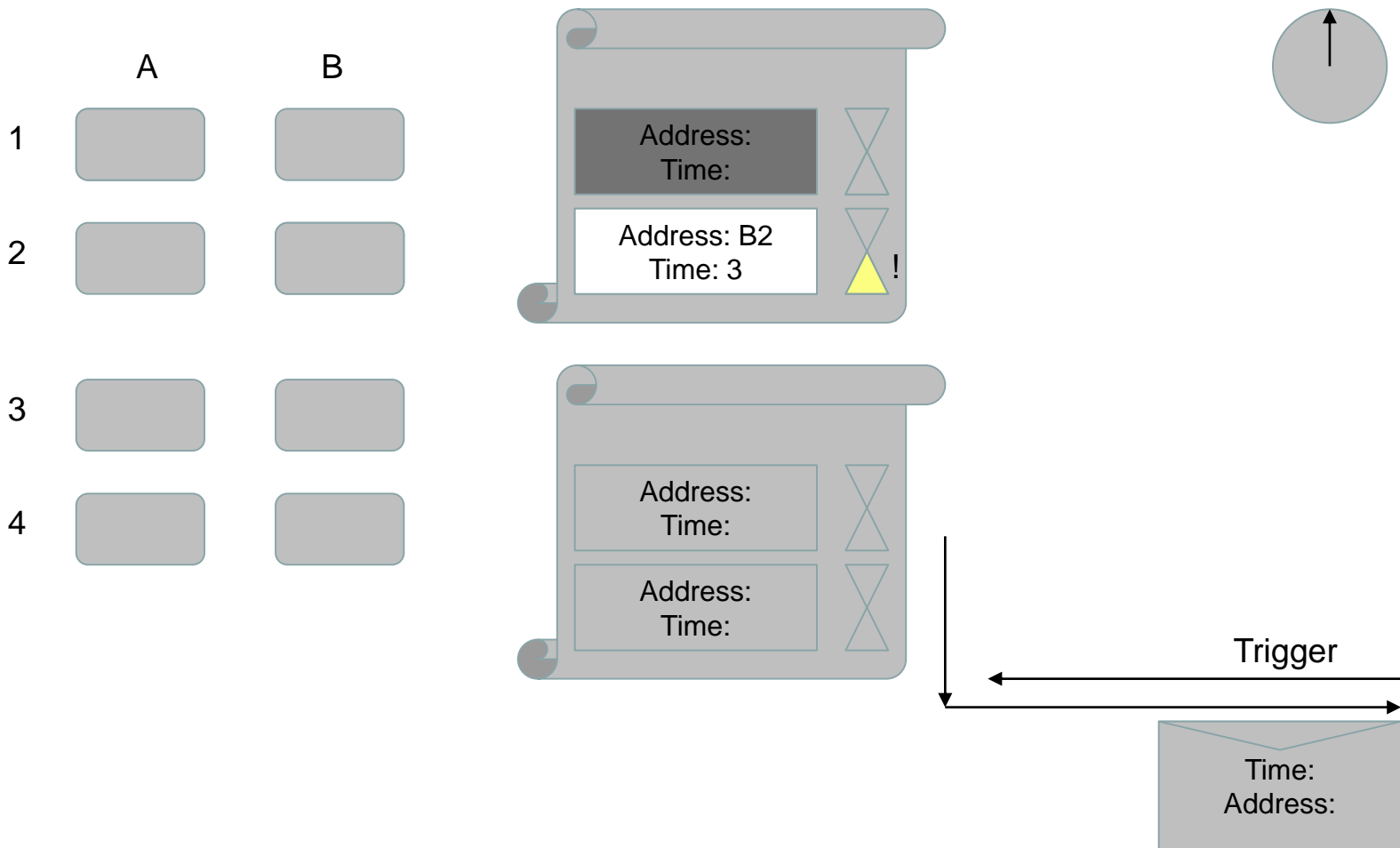
- Triggered readout



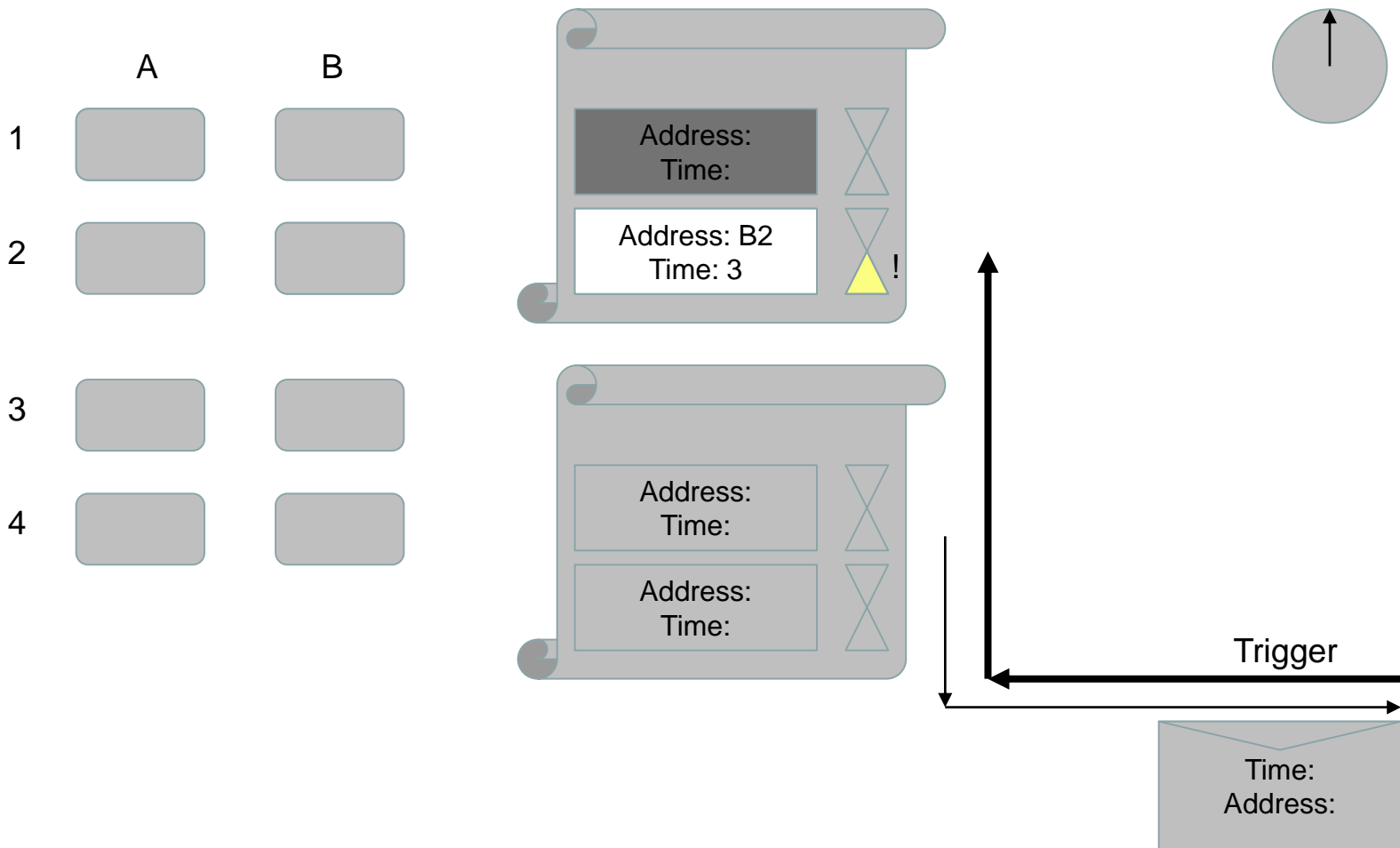
- Triggered readout



- Triggered readout

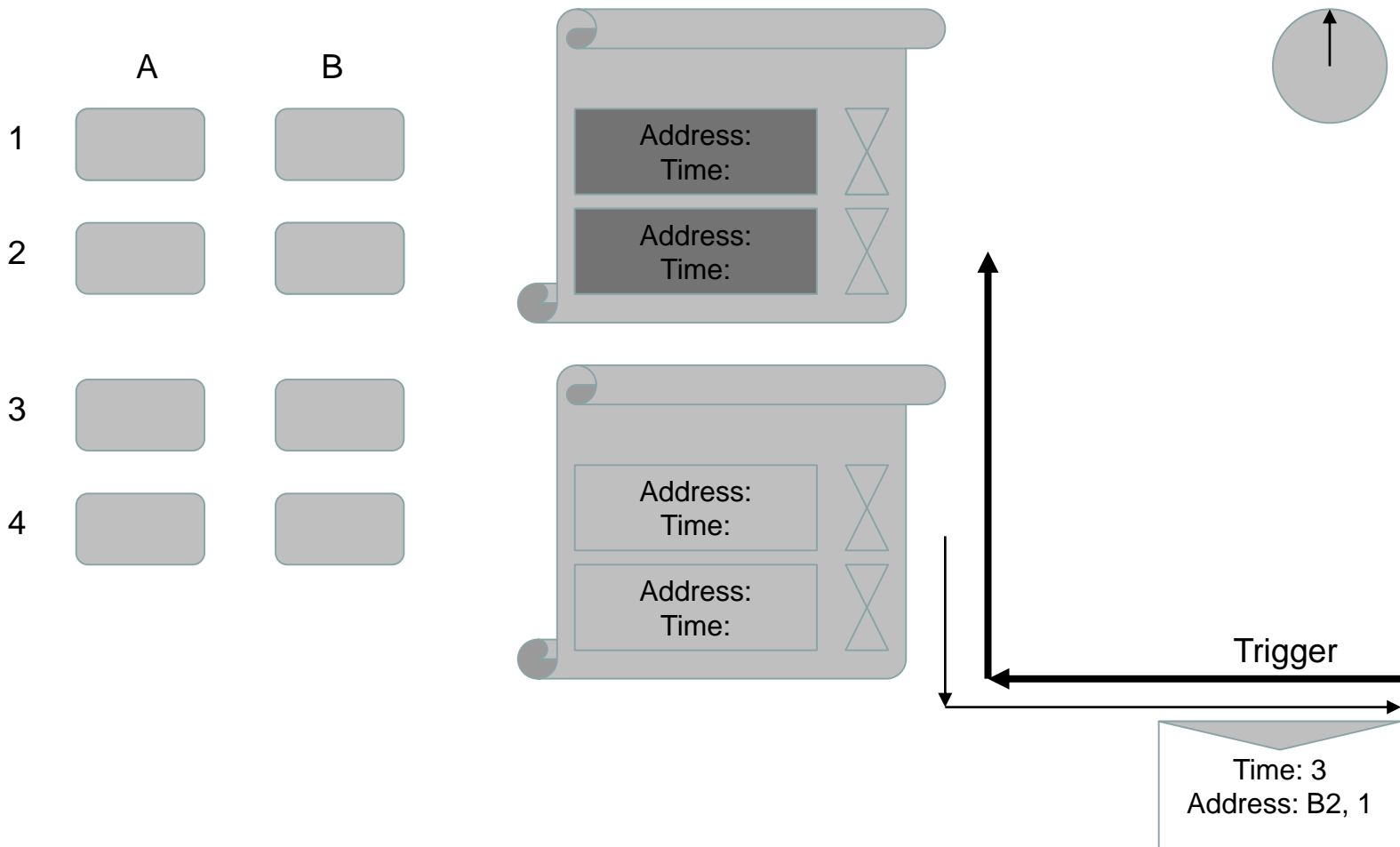


- Triggered readout

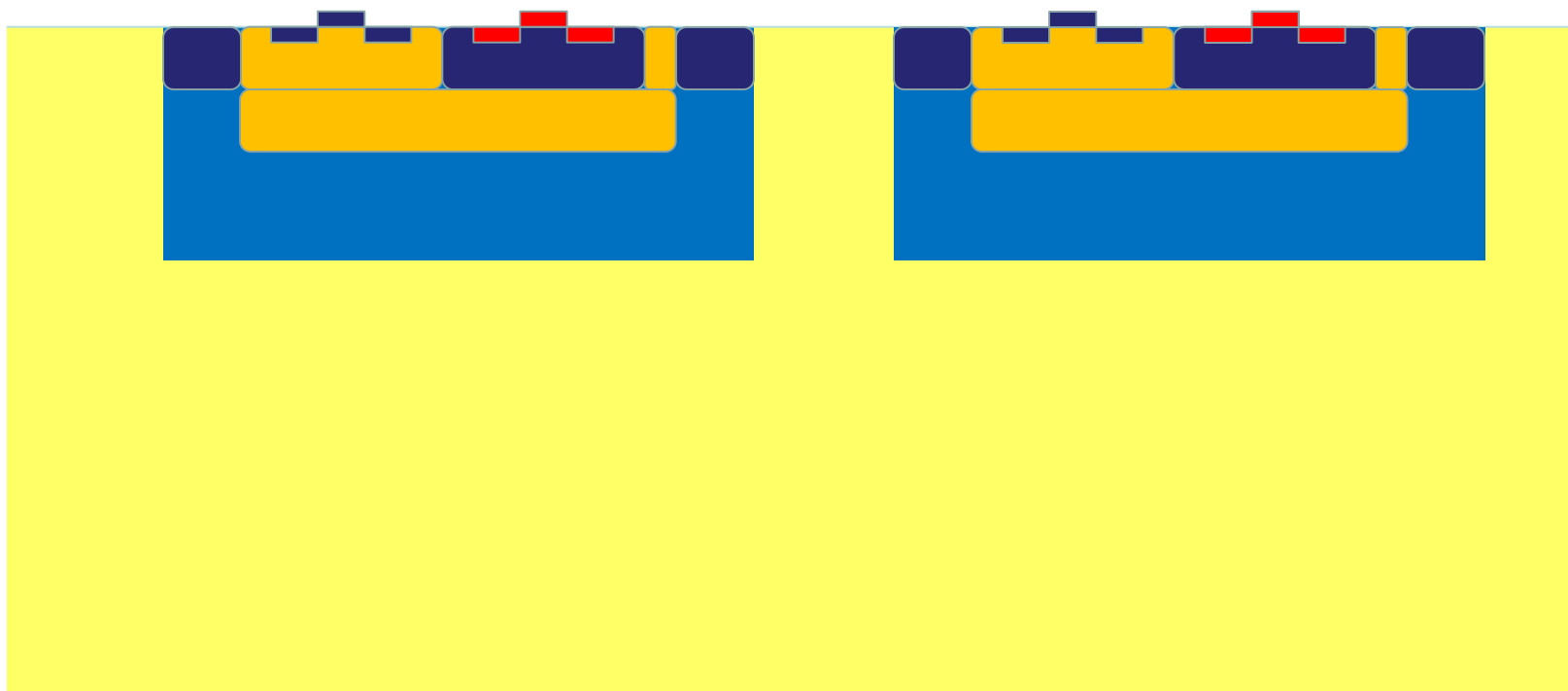




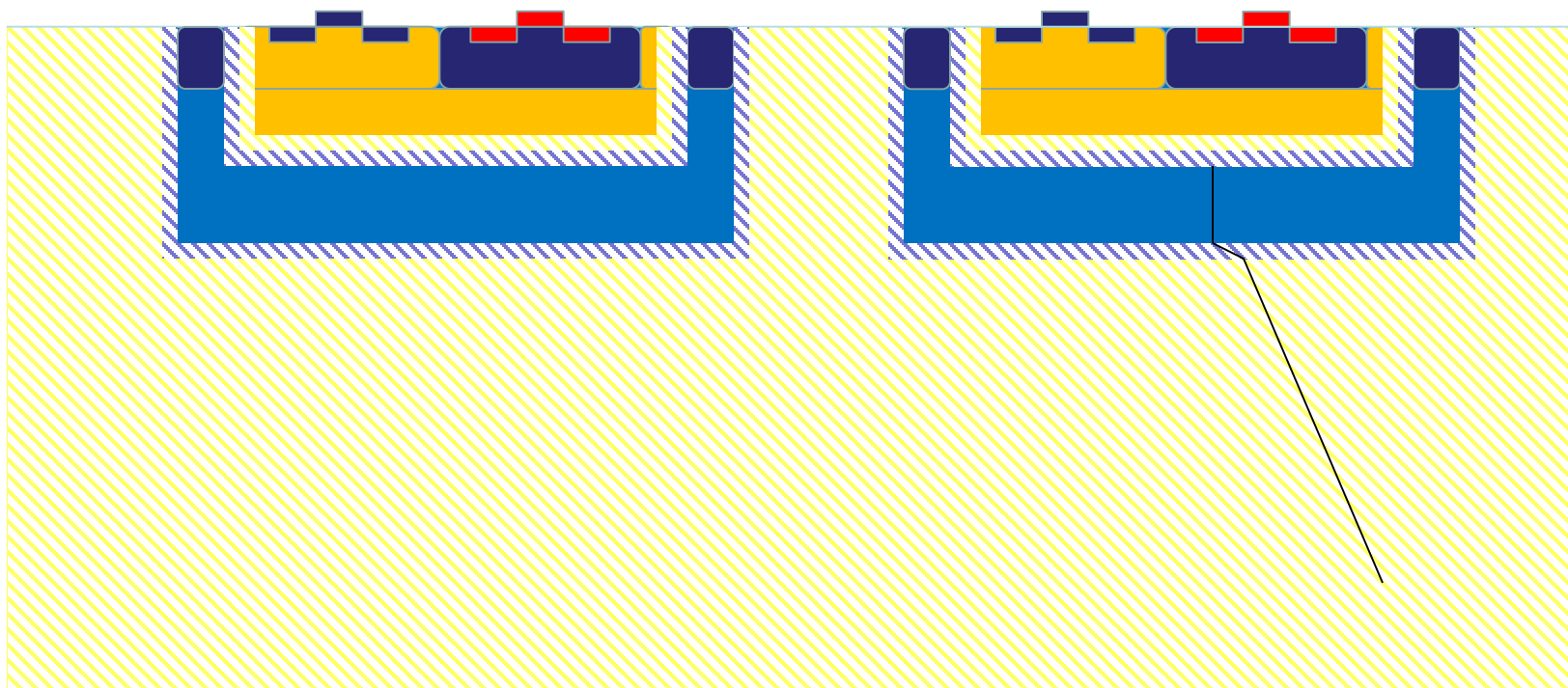
- Triggered readout



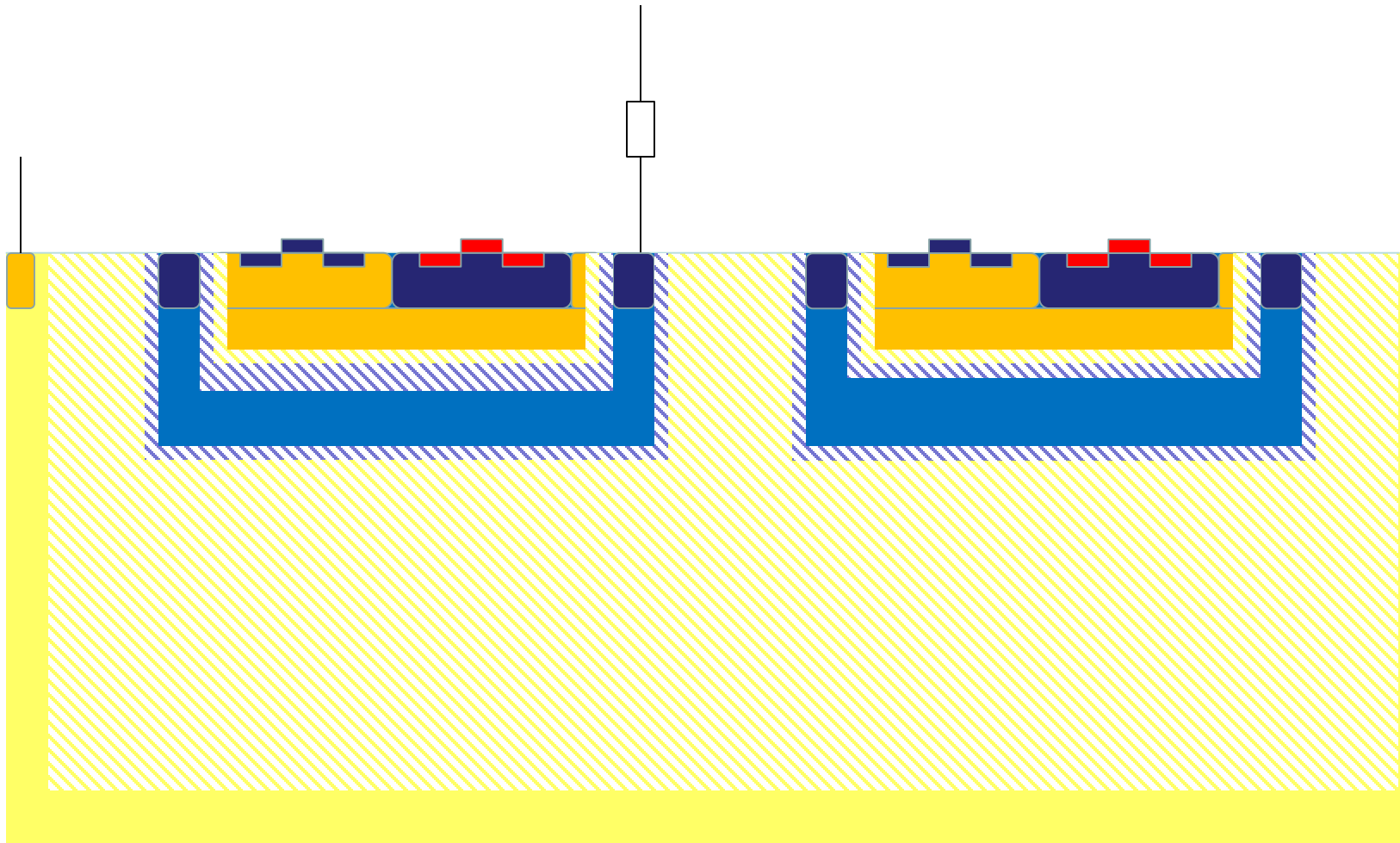
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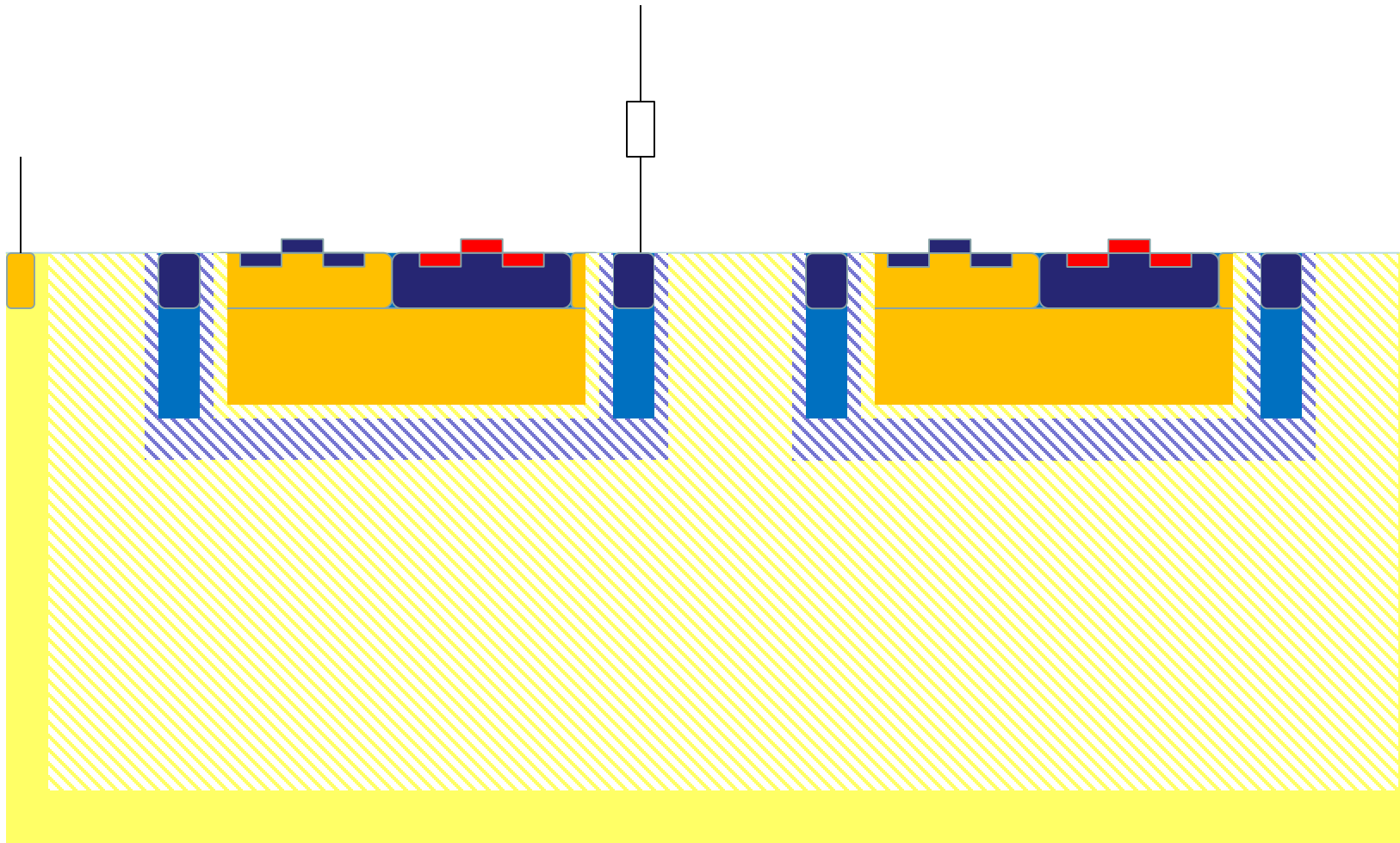
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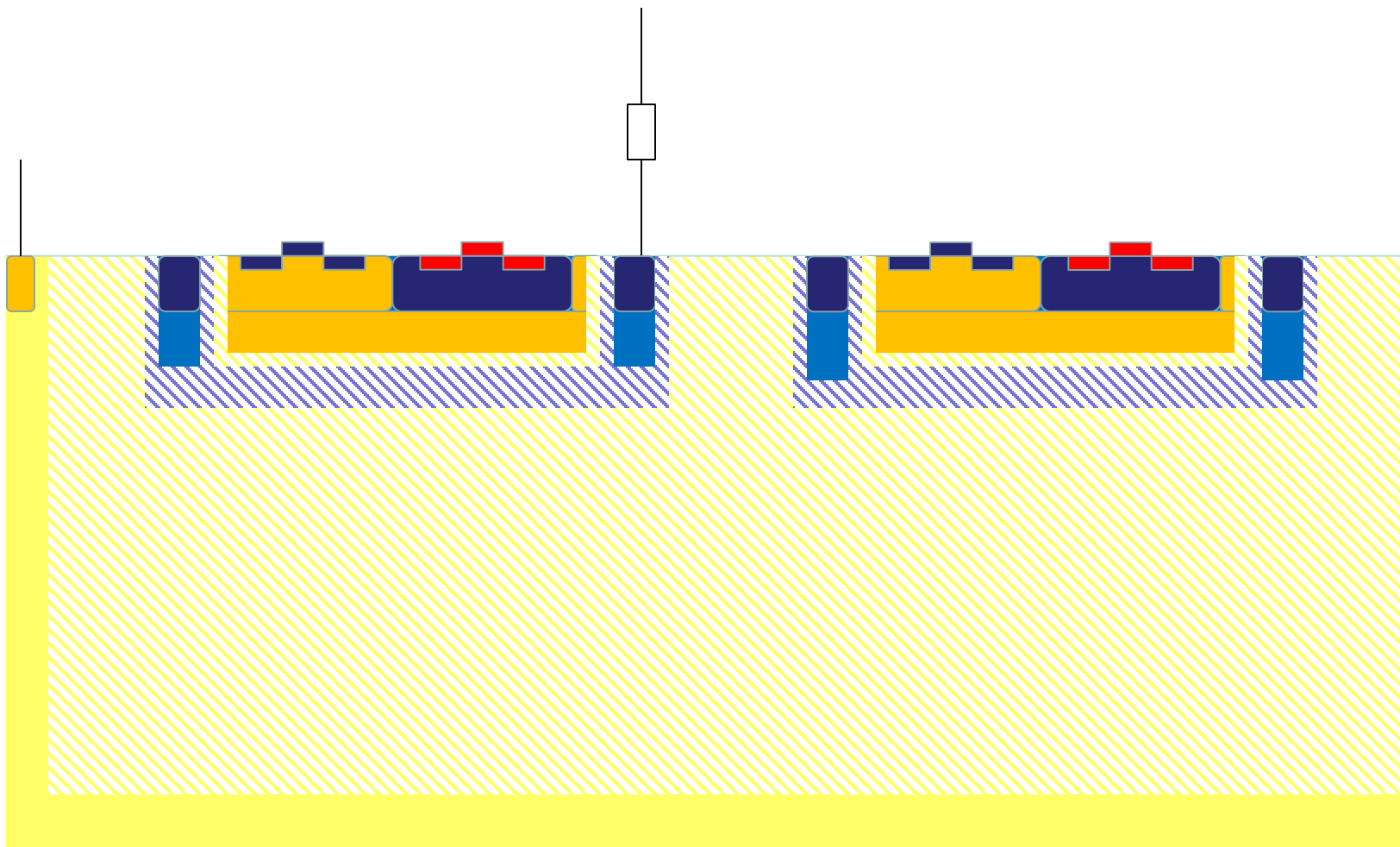
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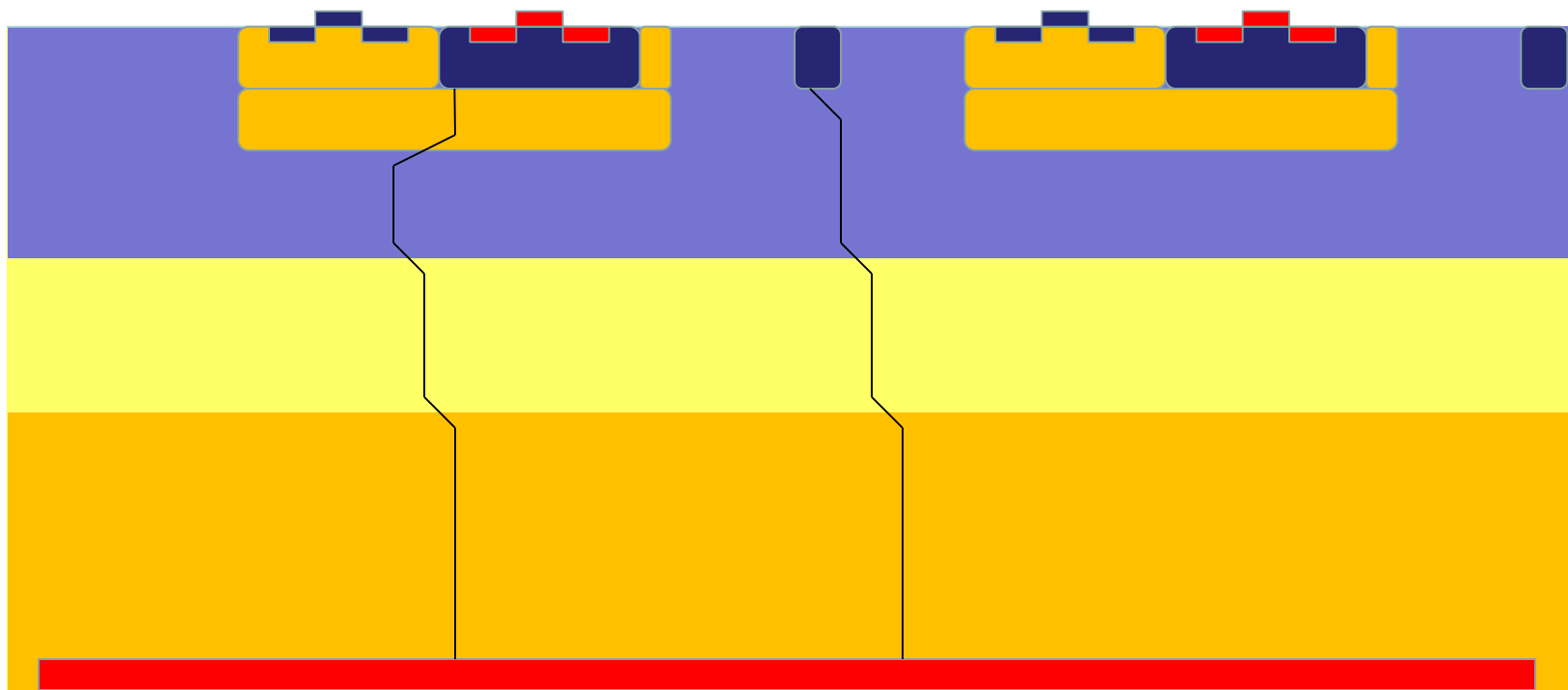
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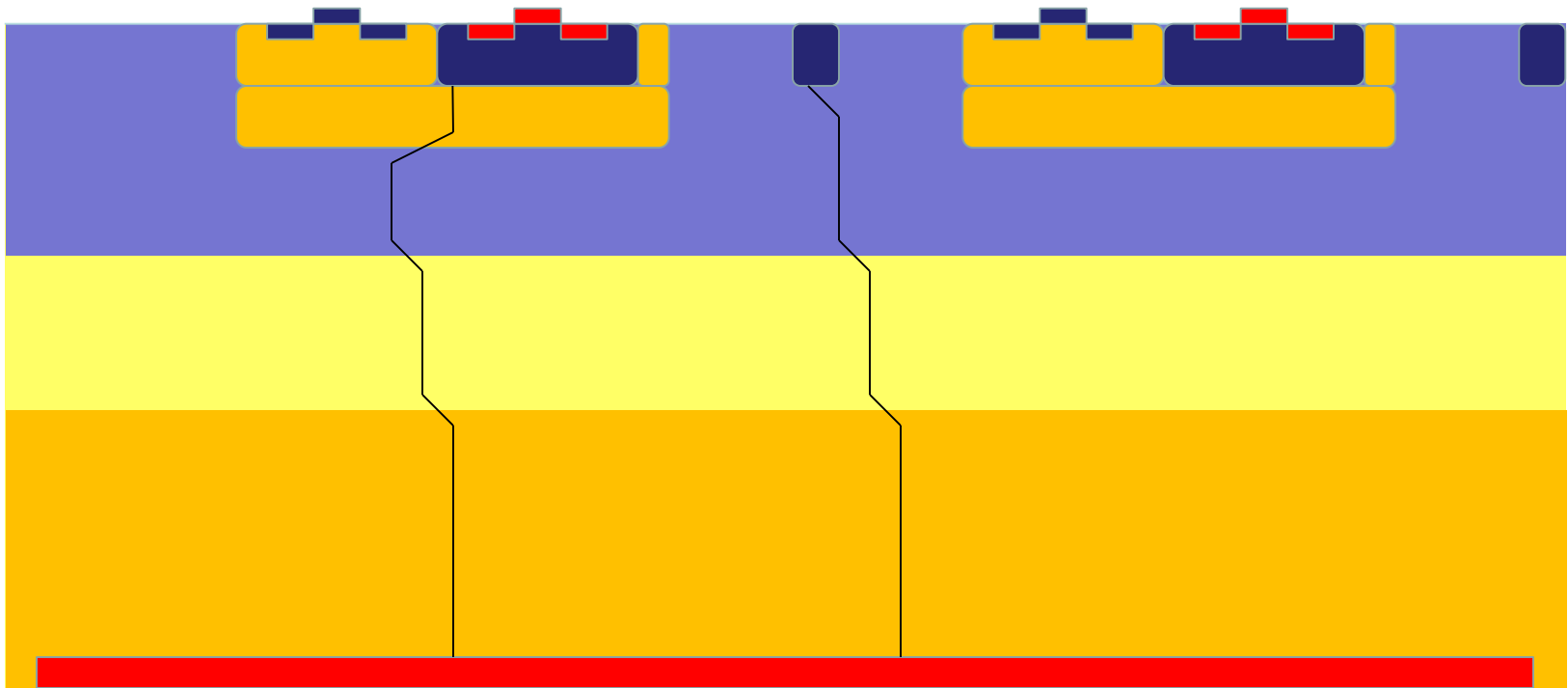
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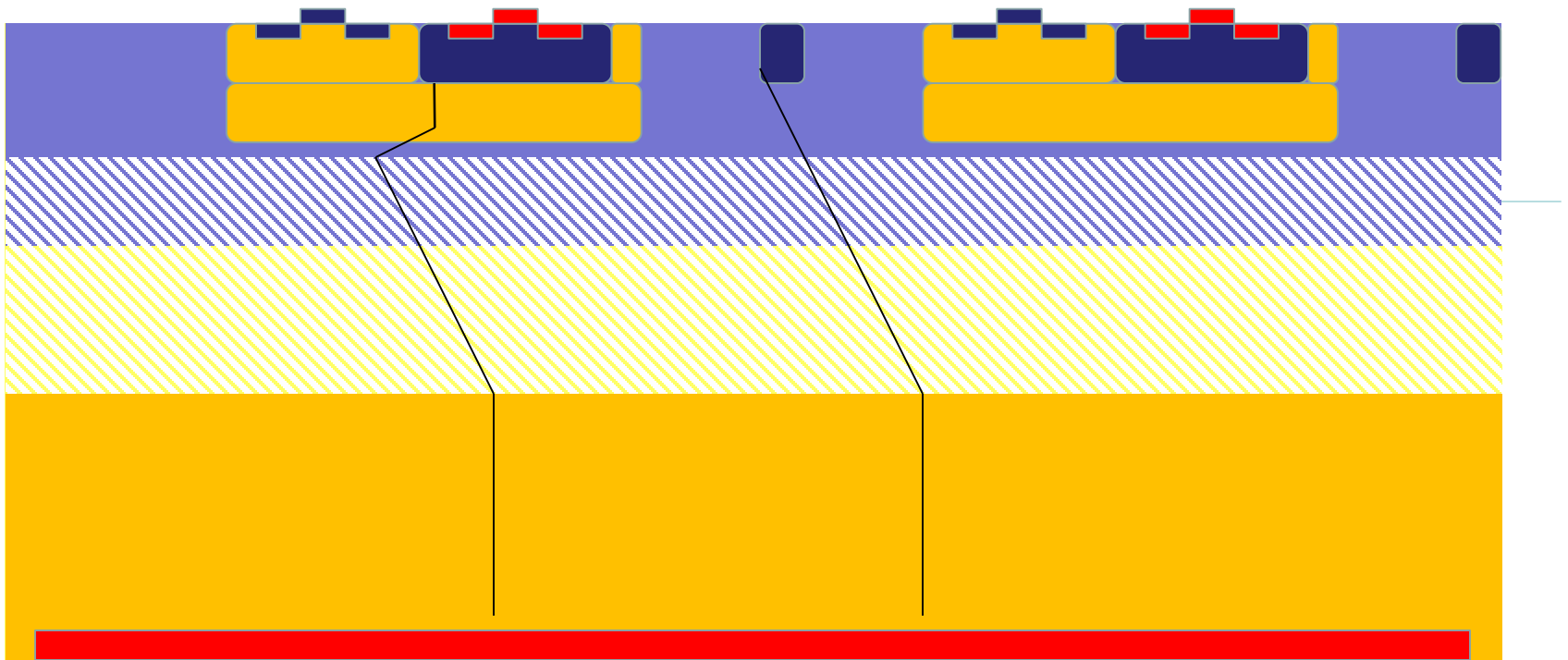


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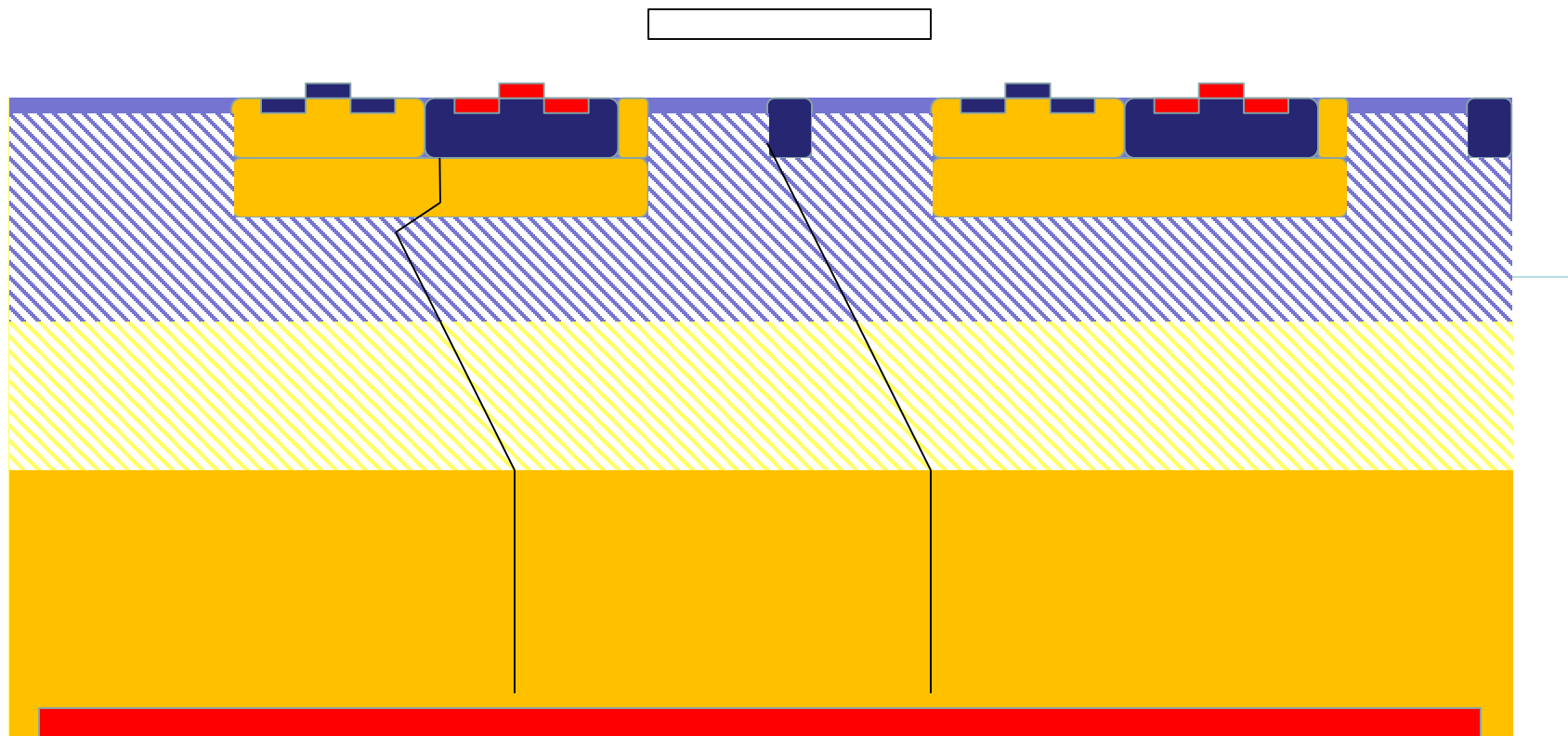




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For efficiency  $Th < 0.25 S$

$$Th \sim N + \text{Sigma}(Th) + \text{Crosstalk}$$

$$N \sim (C_{det} + \textcircled{C_{in} + C_f}) \frac{1}{\sqrt{gm T_{peak}}} \quad \begin{matrix} 60 \\ 85 \end{matrix}$$

$$T_{peak} > \frac{(C_{det} + \textcircled{C_{in}})(C_{out} + C_f) + \textcircled{C_{out}C_f}}{C_f gm} \quad 960$$

$$gm \sim I_{bias}$$

15.4

$$T_{res} = T_{peak} \frac{Th}{S}$$

$$T_{res} \sim T_{peak} \frac{N}{S} \sim (C_{det} + C_{in} + C_f) \frac{\sqrt{T_{peak}}}{S \sqrt{gm}}$$