Radiation Hardness of Silicon-on-Insulator Pixel Devices
- Ten years of struggle -

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Project supported by
JSPS Grant-in-Aid for Scientific Research on Innovative Areas
OUTLINE

• SOI Pixel and Radiation Damage
• TID Damage and Compensation
  - First Results
  - BPW
  - Double SOI
    TrTEGs
    INTPIXh2
    FPIX2
    FPIX3
• Conclusions
SOI PIXEL

SOI: SILICON-ON-INSULATOR
CMOS circuitry fabricated on buried oxide (BOX)
LAPIS 0.2um FD-SOI

Features:
• monolithic (no metal bumps)
• SOI-CMOS (FETs fully isolated)
• Can choose* substrate of optimum resistivity (fully depleted CMOS sensors possible)
  *SOITEC SmartCut™
  
many excellent features
  
• Material budget
• S/N
• power dissipation
  
• speed
• cost
• Pixel size
  
• single event effects
• latch up
• Operation temp. (0.3K~570K)

IN SUMMARY...ALREADY

What is needed to realize (radhard) depleted CMOS pixels?

\[ d \sim \sqrt{\rho \cdot V} \]

1. “High” Voltage add-ons to apply 50 – 200 V bias
   - OK

2. “High” Resistivity Substrate Wafers (100 Ωcm – kΩ cm)
   - OK

3. Multiple (3-4) nested wells (for shielding and full CMOS)
   - Not needed

4. Backside Processing (for thinning and back bias contact)
   - OK

I. Peric, NIM A582 (2007) 876-885

from: www.xfab.com

I. Mandic et al., JINST 12 (2017) no.02, P02021

RAD-DAMAGE IN SOI

- strong against SEE*
  (thin active layer in SOI)
*SOI is a standard in space application

- affected by TID caused by accumulation of holes in insulator

Contribution from BOX is larger

Surrounded by insulator

40nm

~O(10)um
Hole accumulation

- smaller $V_{\text{gate}}$ required for turn-on

- $V_{BG}$ can null the $V_{\text{th}}$ shift

Fig. 11. Dose dependence of the threshold voltage shift for NMOS and PMOS transistors. The transistors are with the smallest gate length and body floating (see Table I). Open marks are the data obtained from proton irradiation.

- The threshold shifts are significant ($V_{CC} \sim 1.8V$)
- Proton-induced damage $\sim \gamma$ damage (TID)

Back-gate biasing is a clue to compensation but the detector back is for sensor biasing...
BPW (BURIED P-WELL)

- BPW(V=0) no effect for rad-damage
- BPW(V<0) should improve, but
  BPW tied to the pixel node … nested structure

Fig. 4. Radiation induced threshold shifts for NMOS and PMOS transistors vs. radiation fluence, without and BPW=0 V. $V_{BG}=0$ V. The first points refer to the pre-irradiation values.

Fig. 6. The $I_d-V_{gs}$ curves of NMOS transistor Tr4 irradiated to $1.3\times10^{12}$ 1-MeV $n_{eq}$ cm$^{-2}$ for (left) without BPW and (right) with BPW grounded. Curves are for different back-gate bias $V_{BG}$. $V_{ds}=2$ V.

~$10$ kGy

BPW suppresses the back-gate effect

DOUBLE SOI WAFER SINCE 2011

1st bonding

2nd bonding

SOI wafer

DSOI wafer

Negative View

The 1st metal layer

Gate

Top-SOI

Substrate

Middle-SOI

BOX1

BOX2

Si: 46.7 nm

SiO2: 158.7 nm

Si: 84 nm

SiO2: 156.0 nm

5.0 kV x 150k

0.3 μm

Courtesy of Lapis Semiconductor
DOUBLE SOI

Figure 1: I–V curves of (left) various $V_{SOI2}$ settings, compar... Vth Compensable by $V_{SOI2}$!
DOUBLE SOI

However...

Substantial reduction of $g_m$ for PMOS.... reason understood and solved
But, SOI works up to 100 kGy, good enough for ILC vertex
**DOUBLE SOI PIXEL**

Single VSOI2 control (INTPIXh2)

**Fig. 6.** Response to IR laser of a 100 kGy irradiated INTPIXh2: (left) \( V_{SOI2} = 0.0 \, \text{V} \), (right) \( V_{SOI2} = -10.0 \, \text{V} \) [12].

- Response after 100kGy observed
- \( V_{REST} \) response not fully recovered
- Proportional to depl. thick (IR laser)
The amplifier is not optimized for fast signal, but radiation-induced degradation in charge collection time seems small.
DOUBLE SOI – 3 $V_{\text{SOI2}}$ CONTROLS

$V_{\text{SOI2}} = (V_{\text{SOI2 IO}}, V_{\text{SOI2 pix}}, V_{\text{SOI2 dec}})$

**200 kGy**

$V_{\text{SOI2}}(-5 V, -10 V, -21 V)$

$V_{\text{SOI2}}(0 V, 0 V, 0 V)$

$V_{\text{SOI2}}$ response almost recovered

**500 kGy**

$V_{\text{SOI2}}(-12.5 V, -15 V, -29 V)$

$V_{\text{SOI2}}(0 V, 0 V, 0 V)$

$V_{\text{SOI2}}$ response partially recovered

TID most critical on:

- **PIXEL** … signal integration
- **DEC** … voltages for gain control
- **IO** … FET functioning for ESD

JPS (2016)

FNAL TEST BEAM

FTBF: 120GeV protons from Main Injector
4.2s beam spill every 1 minute

- Trigger generated by a SEABAS2 board using Scint.(5mm-sq) and ATLAS FE-I4 (2mmx1.75mm ROI)
- Data of 4 FPIX2 and 2 SOFIST sensors acquired per TLU request. All R/O boards (SEABAS2) implemented with same TimeStamp firmware
- Last FPIX2 made accessible for exchanging to irradiated DSOI

SEABAS2 (Soi EvAluation BoArd with Sitcp): 16ch 12bit 40MHz ADCs, Giga-bit Ethernet

R. Nishimura et al. “high speed DAQ system...”
5x5 cluster charge about the maximum charge pixel in an event

5x5 cluster charge [ADC]

TID DAMAGE COMPENSATION

FNAL TB : FPIX2 100kGy

Innovative double-SOI allows operation of SOI devices @ 100kGy

Noise: $1.8 \pm 0.1 \pm 5.4 \pm 0.5@RT$

MORE COMPENSATION...

PMOS TID in sidewall: LDD loses control (LDD: lightly doped drain)

- increasing LDD by x10 (FPIX2->FPIX3)

Trans-conductance recovered significantly

Vth shift compensable by applying negative volts to SOI2: optimum volts differ for n/p as dose ~1MGy

✓ Separate n/p SOI2 controls in FPIX3
COMPENSATION TUNING

STEP-1 tune IO
IO outputs are clipped due to always “ON” ESD

STEP-2 tune DECODER
Wide range of VSOI2_IO

STEP-3 tune PIX to maximize the dynamic range and linearity

ESD protection

Vreset response (non-irrad)
For $V_{\text{RESET}} = 100\text{mV}$, tune to minimize the output

Typical $V_{\text{RESET}}$ range

ADC

VSOI2-DECN = 0V

-16V

VSOI2-DECP = -16V

-15V
Response to pulsed IR-laser

FPIX2: 500kGy

V(IO) = -12.5 V
V(Dec) = -26 V
V(Pix) = -15 V

FPIX3: 500kGy

V(IO) = -6
V(Dec N/P) = -20/-30
V(Pix N/P) = -9/-11

FPIX3: 1MGy

V(IO) = -6
V(Dec N/P) = -26/-30
V(Pix N/P) = -10/-11

✓ Response fully recovered at 500kGy
✓ Expect linear response at 1MGy
FPIX3 PIXEL LAYOUT

PIXEL NMOS FETs (N1+N2) located at a corner
One VPIX_n for a group of 2×2 pixels
Rolling shutter R/O resets the signals in next row...

No response from odd-row
OK w/ singleSOI

Pre-irrad
CONCLUSIONS

- TID identified as main concern for SOI applications in high-radiation environment

- Innovative Double SOI solved many issues including TID. LDD profile revisited to enhance radiation tolerance

- TID tolerance up to 500 kGy is achieved and good performance is expected also at 1 MGy (FPIX3)

- SOI pixel (SOFIST) is being developed for the ILC. SOI applications to wider area are encouraged.
SPARES
**FINE-PIXEL DETECTOR: FPIX2**

- **Pixel size:** 8μm
- **#Pixels:** 128 × 128
- **Handle wafers:**
  - >single SOI
    - 25kΩ·cm p, 500 um
  - >double SOI
    - 1kΩ·cm p, 300 um
- **Rolling shutter RO**
  - 8 parallel outputs

**In Development:**
- to demonstrate excellent spatial resolution achievable with SOI technology (=>tracker for SOFIST TB)
- as demonstrator of TID tolerance (FPIX2 equipped with three middle-SOI regions)

**On-pixel circuit**

TID: hole accumulation in BOX/GOX
Middle-SOI: compensate TID effects by applied negative voltages

Analog signals are digitized (2ms) by external SEABAS2 12-b ADCs (8 parallel)