Radiation Hardness of Silicon-on-Insulator Pixel Devices

- Ten years of struggle -

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SOIPIX
Silicon-On-Insulator Pixel Detector Project

Project supported by
JSPS Grant-in-Aid for Scientific Research on Innovative Areas

筑波大学
University of Tsukuba

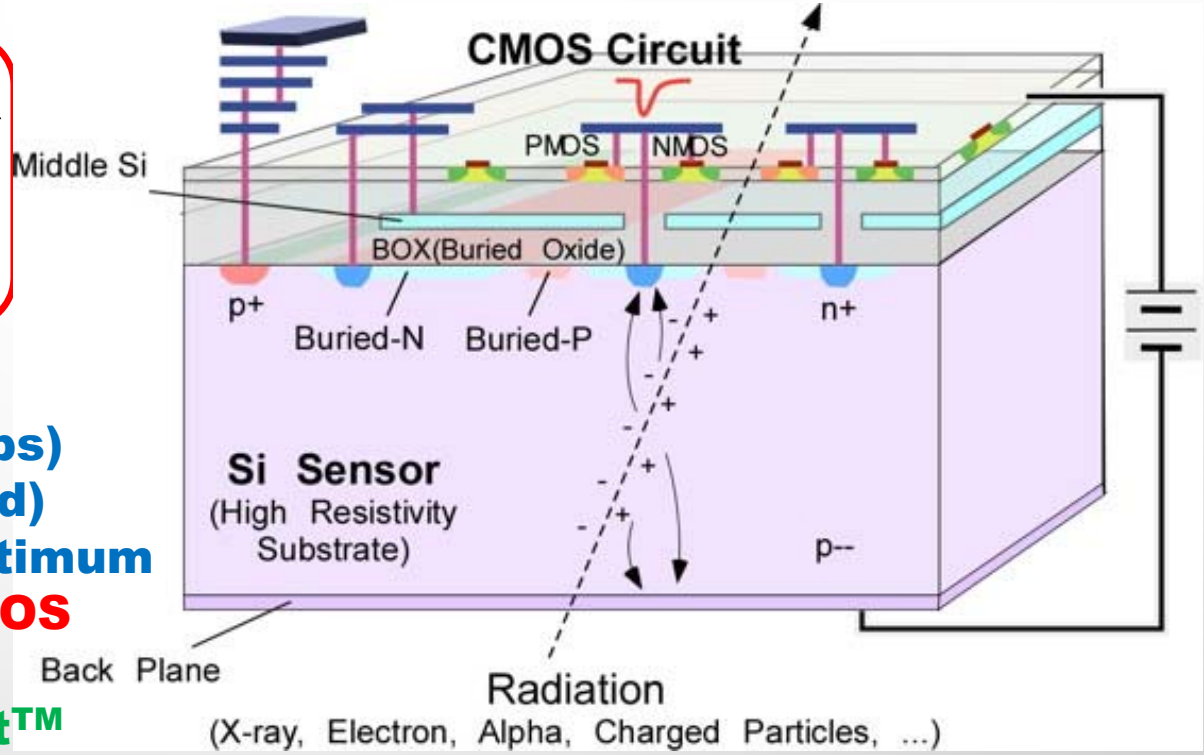
OUTLINE

- SOI Pixel and Radiation Damage
- TID Damage and Compensation
  - First Results
  - BPW
  - Double SOI
    - TrTEGs
    - INTPIXh2
    - FPIX2
    - FPIX3
- Conclusions

SOI PIXEL

SOI: SILICON-ON-INSULATOR

CMOS circuitry fabricated on buried oxide(BOX)
LAPIS 0.2um FD-SOI



Features:

- **monolithic (no metal bumps)**
- **SOI-CMOS (FETs fully isolated)**
- **Can choose* substrate of optimum resistivity (fully depleted CMOS sensors possible)**

***SOITEC SmartCut™**

many excellent features

- **Material budget**
- **S/N**
- **power dissipation**
- **speed**
- **cost**
- **Pixel size**
- **single event effects**
- **latch up**
- **Operation temp. (0.3K~570K)**

IN SUMMARY…ALREADY

What is needed to realize (radhard) depleted CMOS pixels?

universitätbonn

$$d \sim \sqrt{\rho \cdot V}$$

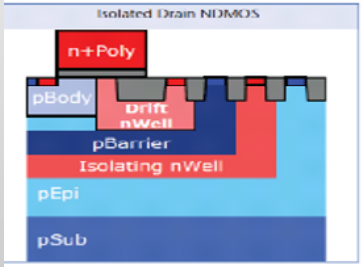
I. Peric, NIM A582 (2007) 876-885

1 **"High" Voltage add-ons to apply 50 – 200 V bias**

OK

2 **"High" Resistivity Substrate Wafers (100 Ωcm – kΩ cm)**

OK



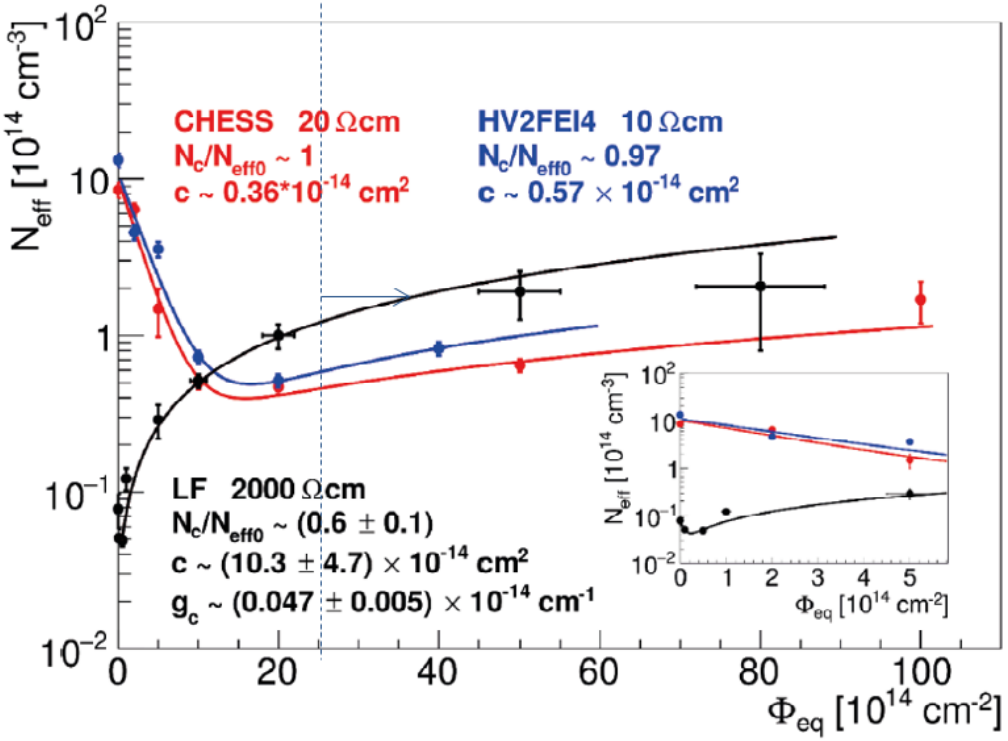
from: www.xfab.com

3 **Multiple (3-4) nested wells (for shielding and full CMOS)**

Not needed

4 **Backside Processing (for thinning and back bias contact)**

OK



I. Mandic et al., JINST 12 (2017) no.02, P02021

N. Wermes, FCC-2017 Berlin, 6/2017

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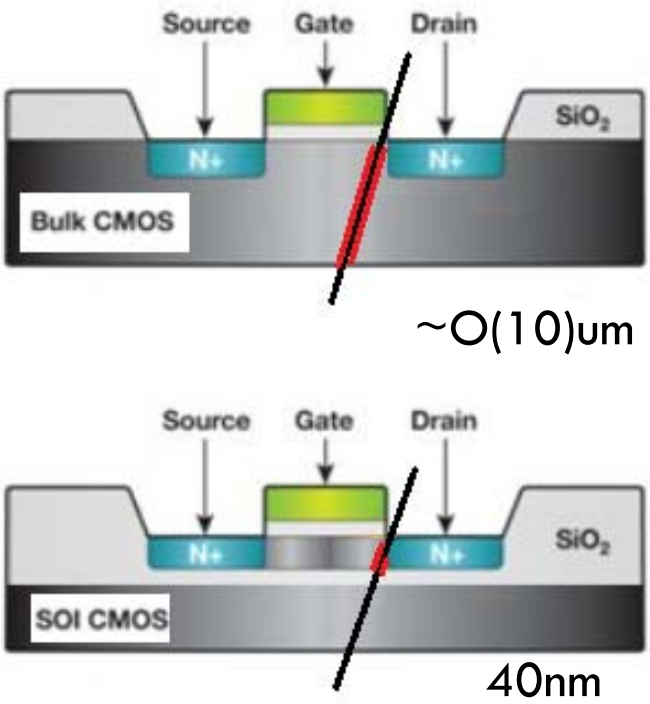
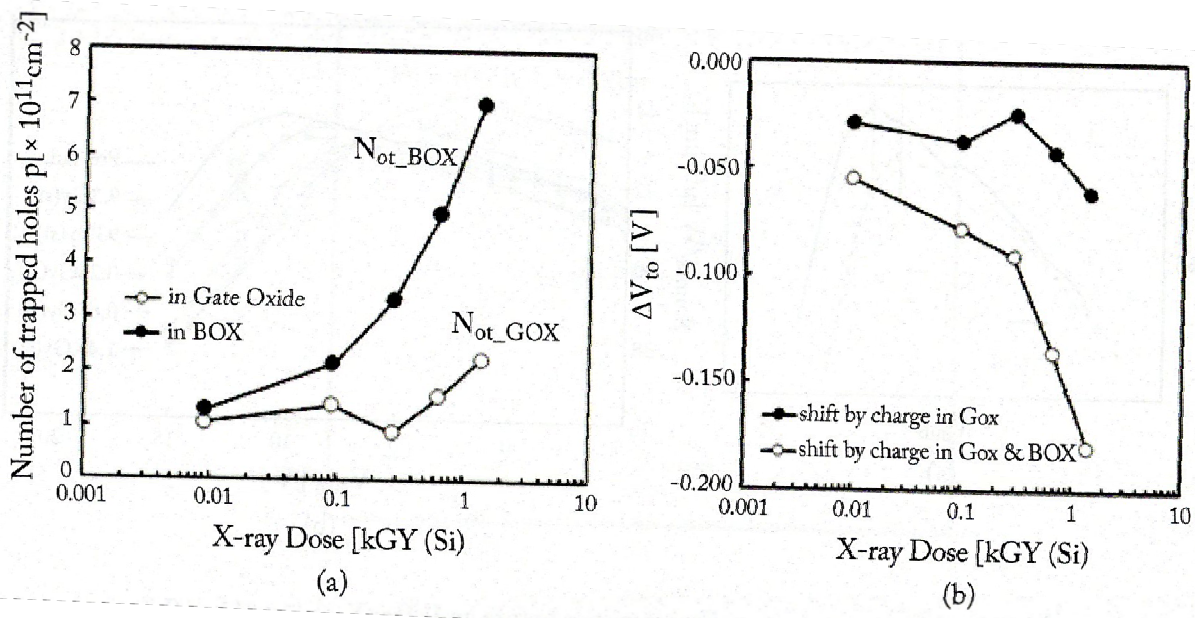
RAD-DAMAGE IN SOI

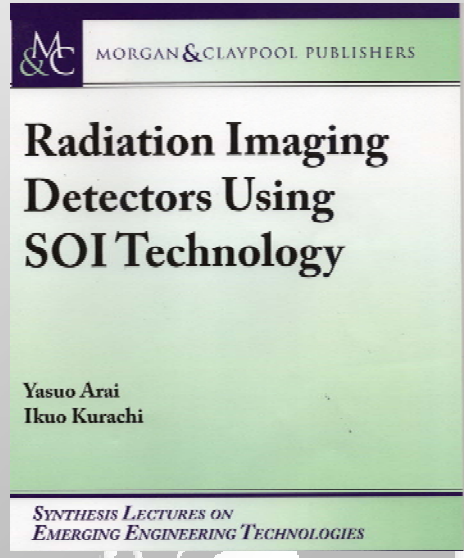




Surrounded by insulator

- strong against SEE*
  (thin active layer in SOI)
  *SOI is a standard in space application

- affected by TID caused by accumulation of holes in insulator
  Contribution from BOX is larger



2008 IEEE Nuclear Science Symposium Conference Record N04-5

IEEE2008

Radiation Resistance of SOI Pixel Devices Fabricated with OKI 0.15μm FD-SOI Technology

K. Hara, M. Kochiyama, A. Mochizuki, T. Sega, Y. Arai, K. Fukuda, H. Hayashi, M. Hirose, J. Ida, H. Ikeda, Y. Ikegami, Y. Ikemoto, H. Ishino, Y. Kawai, T. Kohriki, H. Komatsubara, H. Miyake, T. Miyoshi, M. Ohno, M. Okihara, S. Terada, T. Tsuboyama and Y. Unno

Hole accumulation

⇒smaller Vgate required for turn-on

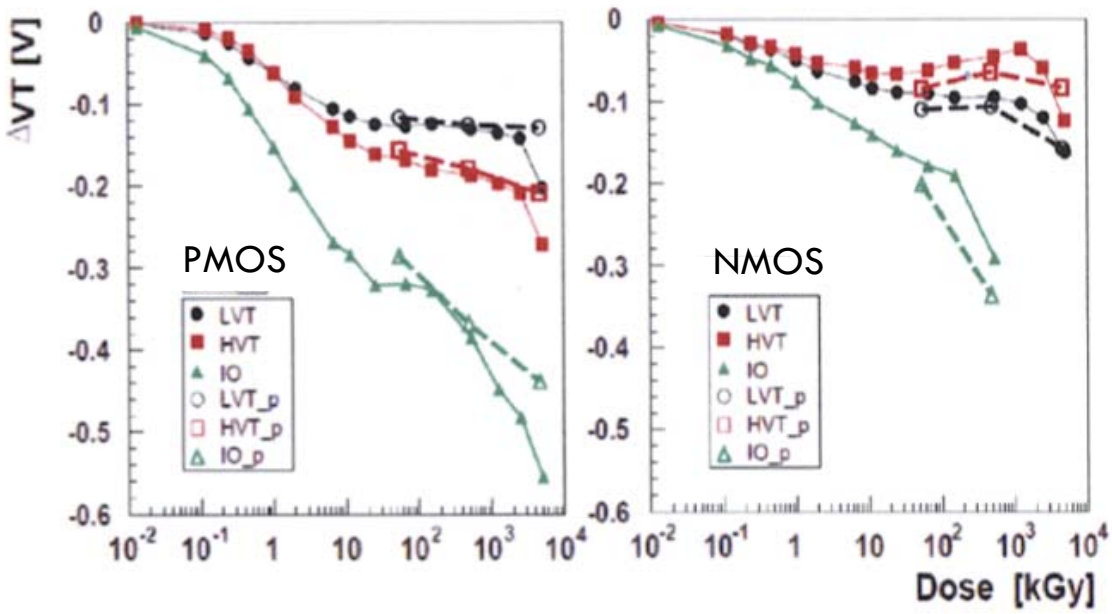
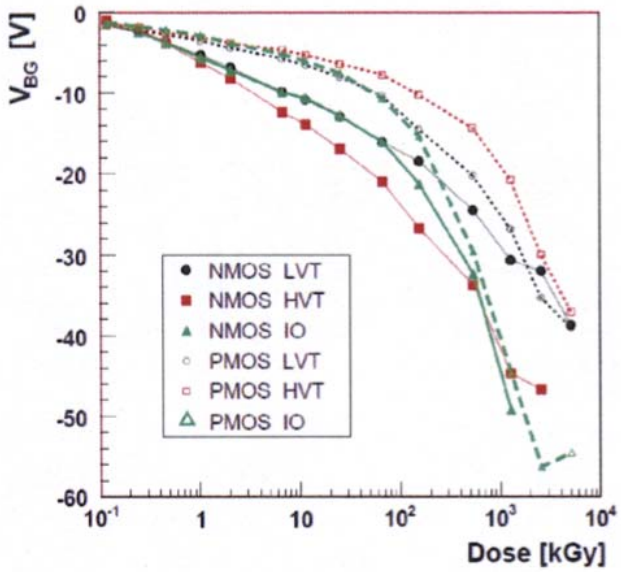
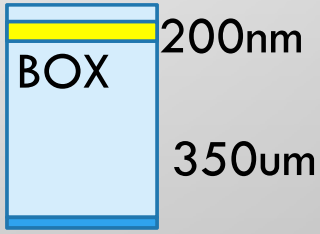


Fig. 11. Dose dependence of the threshold voltage shift for NMOS and PMOS transistors. The transistors are with the smallest gate length and body floating (see Table I). Open marks are the data obtained from proton irradiation.

⇒V_{BG} can null the Vth shift



ig. 12. Optimum Vback voltages for the transistors with shortest gate ths to compensate the threshold voltage shifts.



Back-gate biasing is a clue to compensation

but the detector back is for sensor biasing…

- The threshold shifts are significant (Vcc~1.8V)
- Proton-induced damage ~ γ damage (TID)

HSTD9(2010)

BPW (BURIED P-WELL)

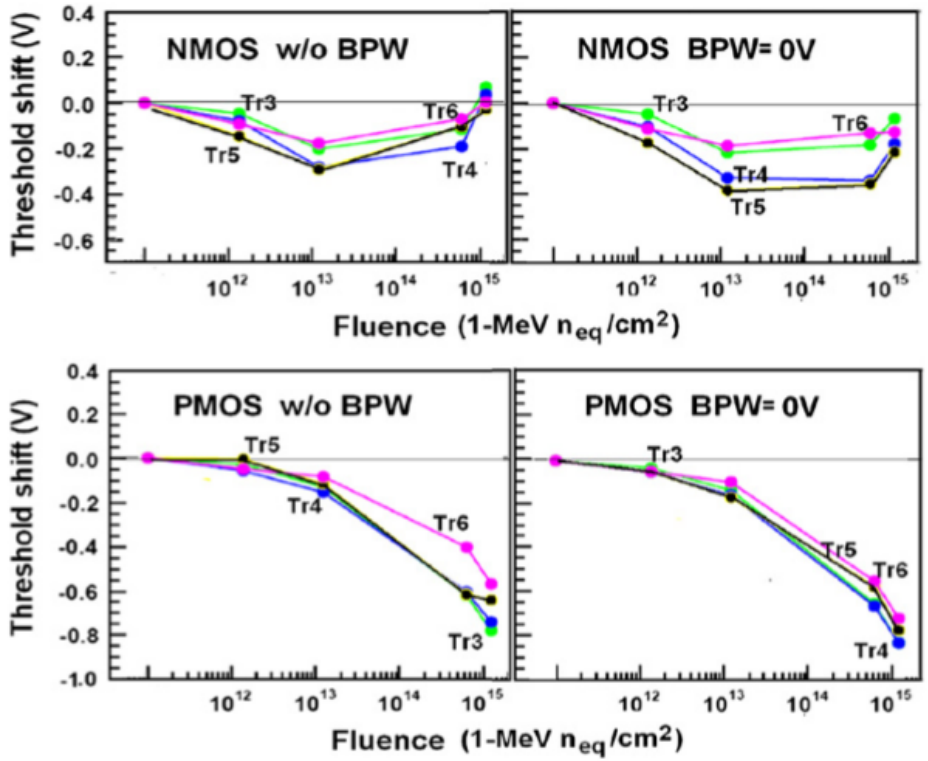
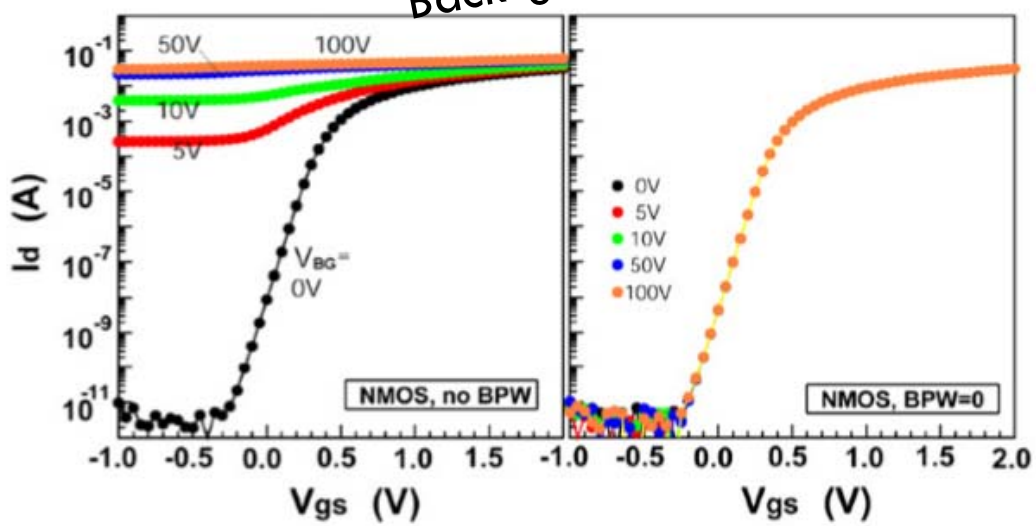


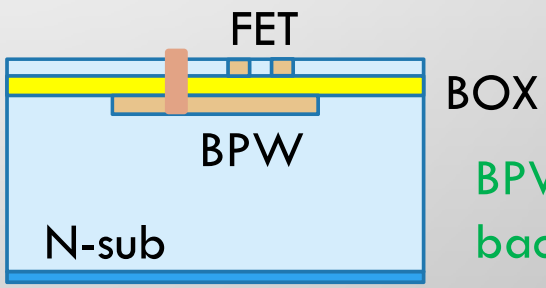
Fig. 4. Radiation induced threshold shifts for NMOS and PMOS transistors vs. radiation fluence, without and BPW=0 V. V_{BG}=0 V. The first points refer to the pre-irradiation values.

Back-gate effect suppressed



~10kGy

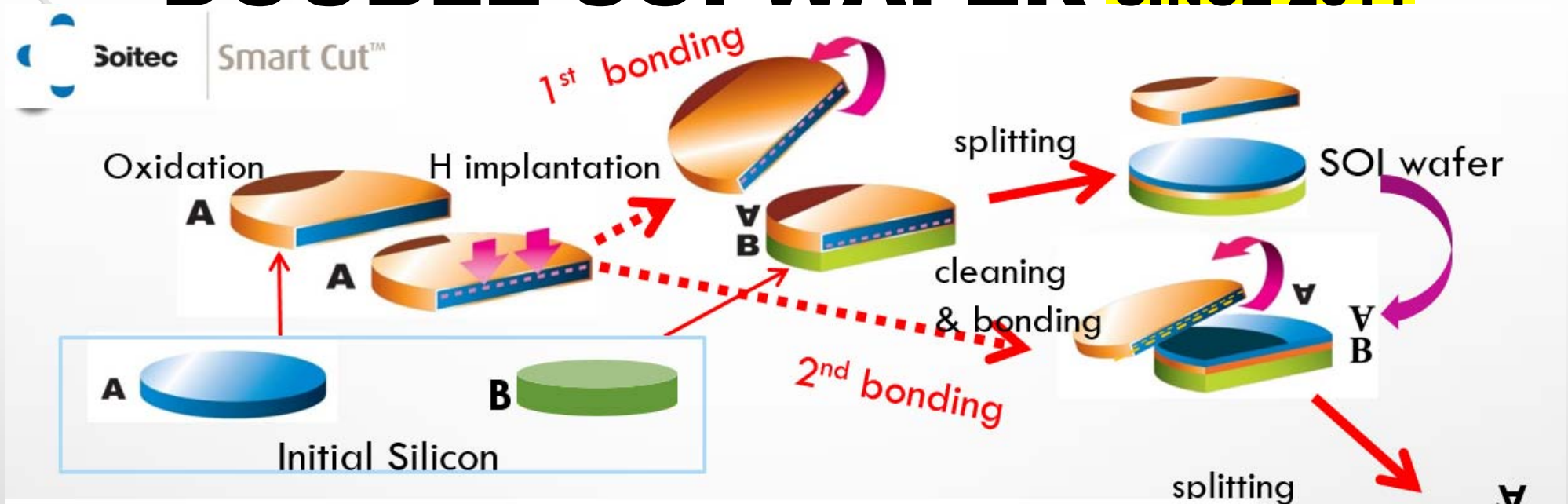
Fig. 6. The I_d–V_{gs} curves of NMOS transistor Tr4 irradiated to 1.3×10^{12} 1-MeV n_{eq} cm^{-2} for (left) without BPW and (right) with BPW grounded. Curves are for different back-gate bias V_{BG}. V_{ds}=2 V.

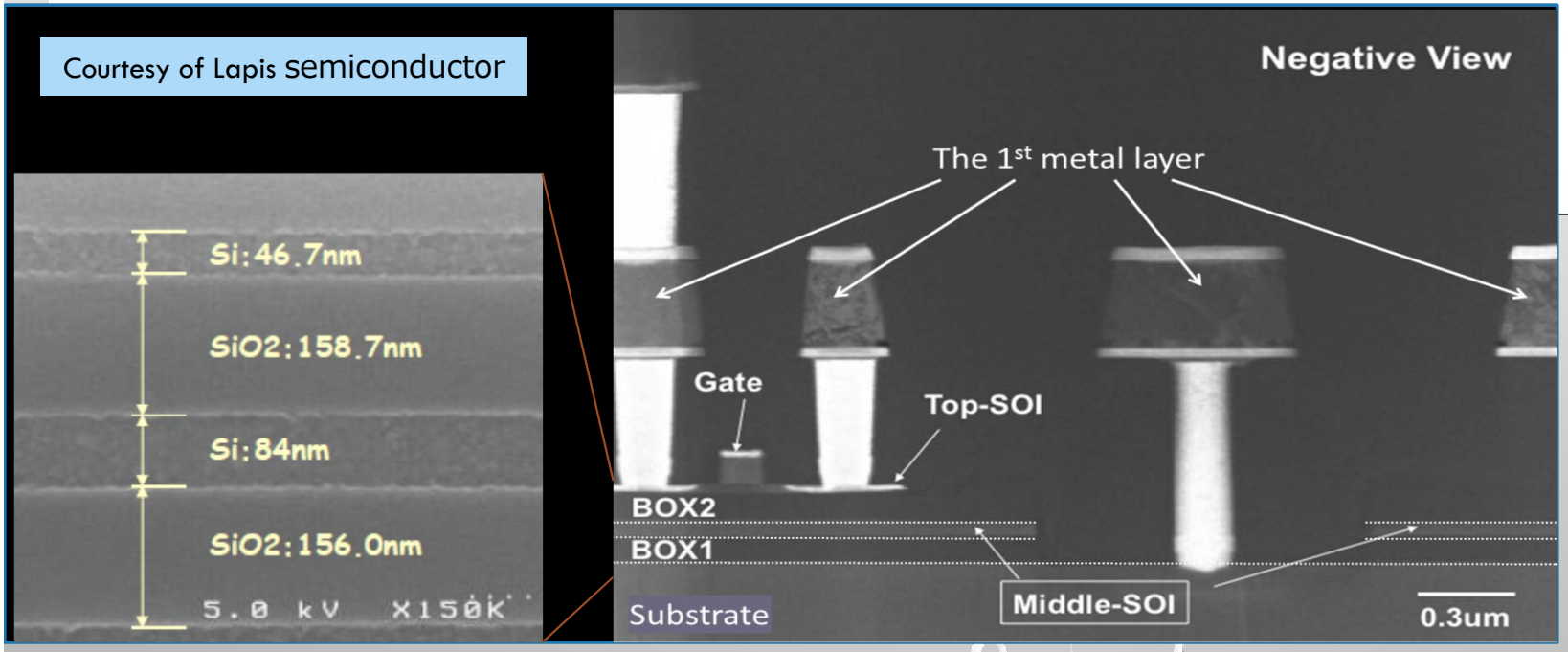


BPW suppresses the back-gate effect

- BPW(V=0) no effect for rad-damage
- BPW(V<0) should improve, but
  BPW tied to the pixel node … ⇒ nested structure

DOUBLE SOI WAFER SINCE 2011

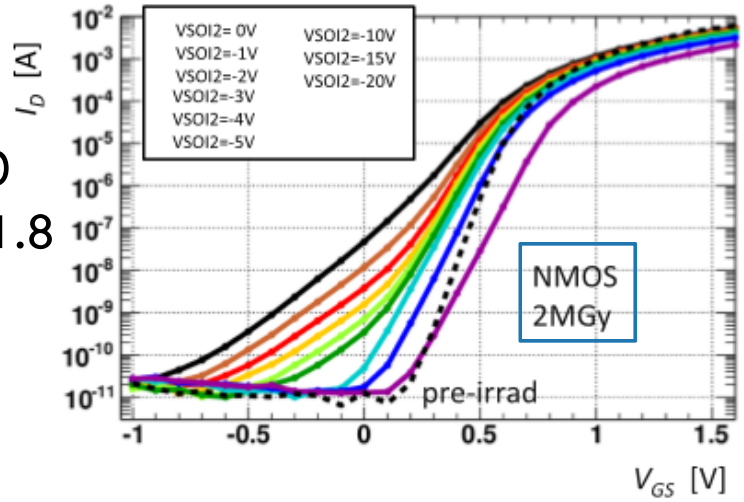


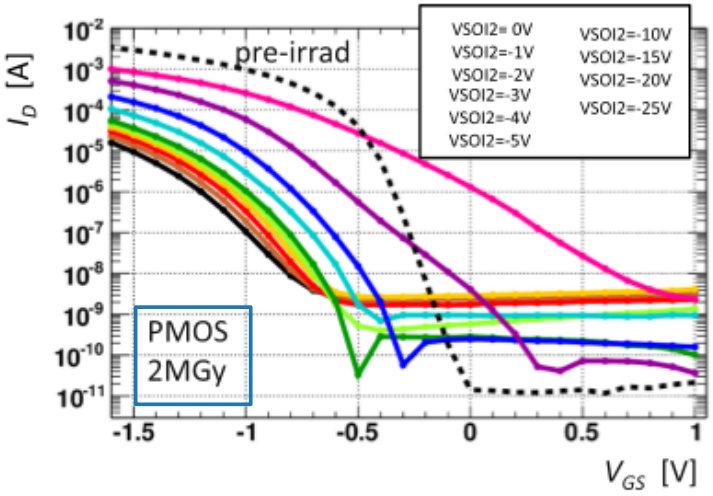


IEEE2013

DOUBLE SOI

V_S=0
V_D=1.8

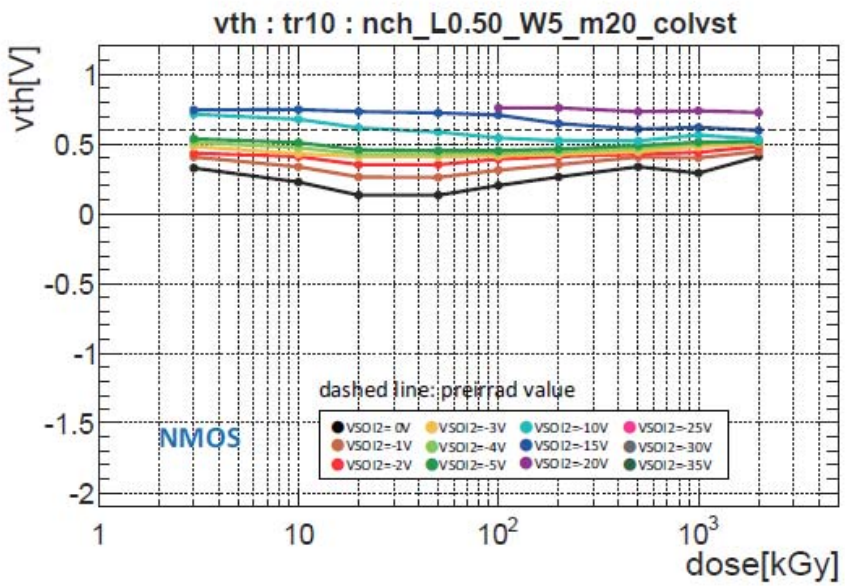


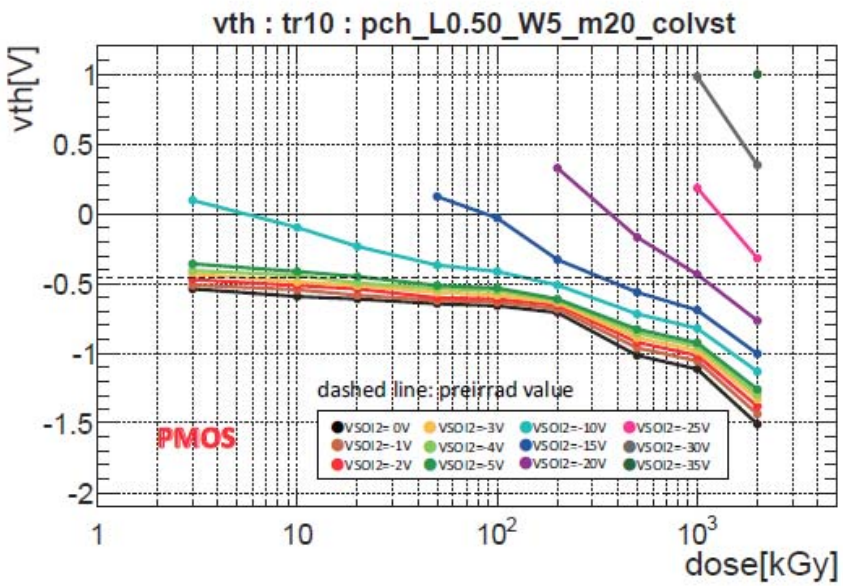


V_S=-1.8
V_D=0

Figure 1: I–V curves of (left) curves are for various V_{SOI2} settings, compar

Vth Compensable by VSOI2 !

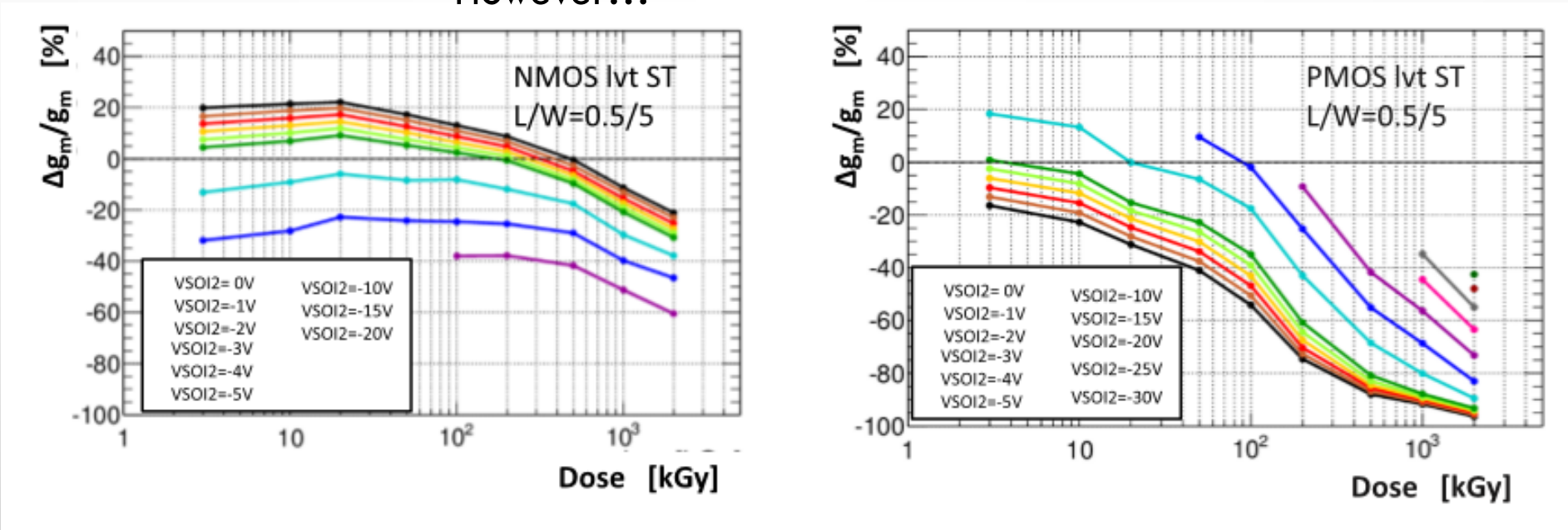




IEEE2013

DOUBLE SOI

However…



Substantial reduction of gm for PMOS…. ⇔ reason understood and solved

But, SOI works up to 100 kGy, good enough for ILC vertex

HSTD10(2015)

DOUBLE SOI PIXEL

Single VSOI2 control (INTPIXh2)

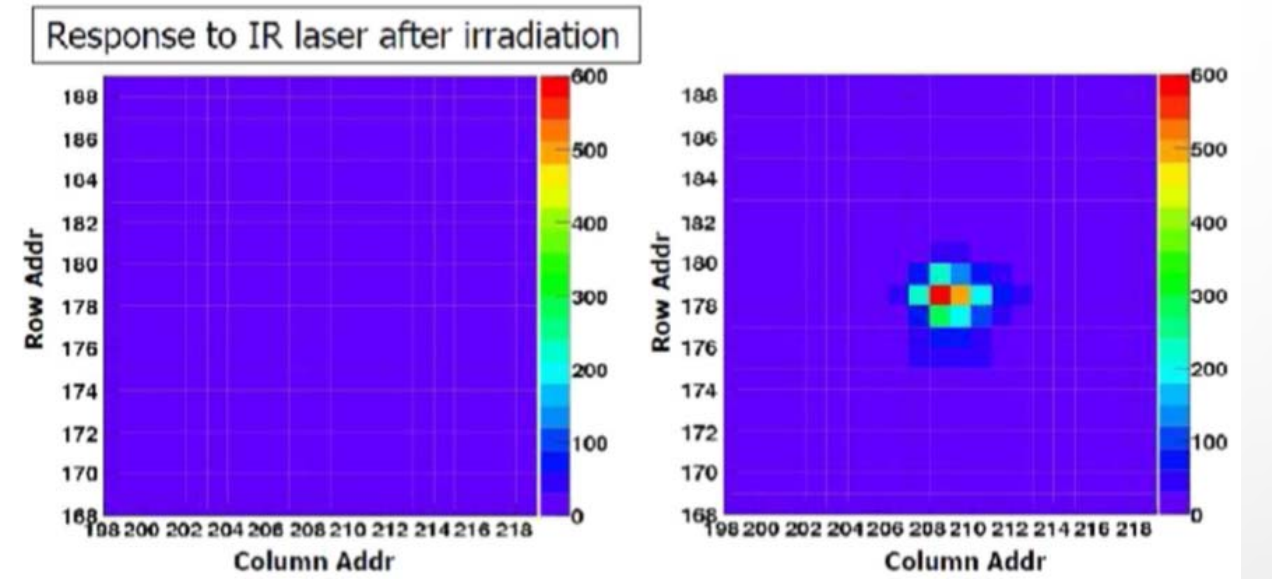
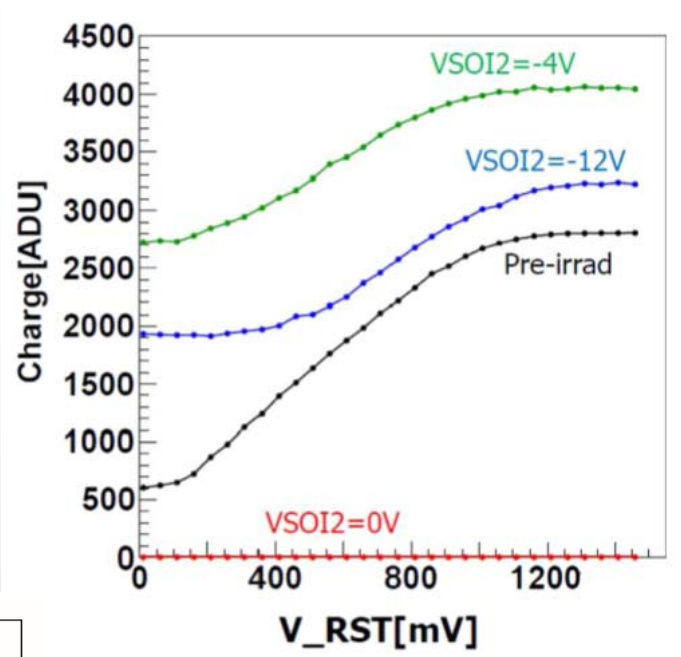


Fig. 6. Response to IR laser of a 100 kGy irradiated INTPIXh2: (left) $V_{SOI2} = 0.0$ V, (right) $V_{SOI2} = -10.0$ V [12].

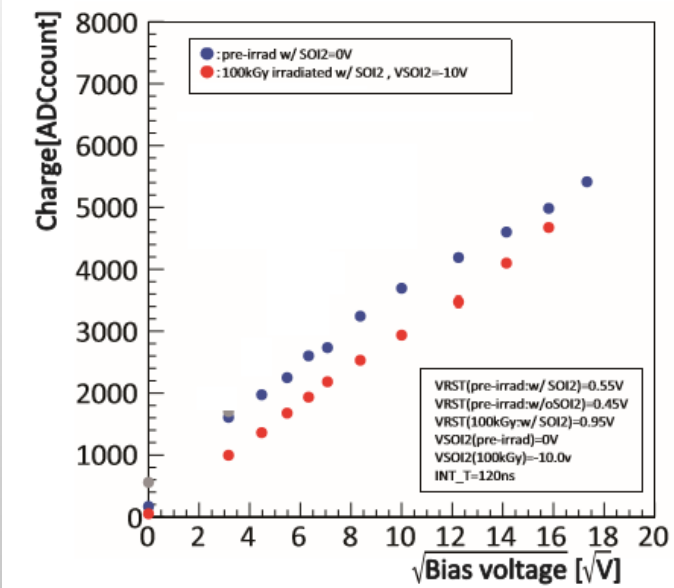


7. Response to V_{RST} before and after 100 kGy irradiation with V_{SOI2} of 0 V, /, and −12 V [12].

Response after 100kGy observed though

V_{REST} response not fully recovered

Proportional to depl. thick (IR laser)



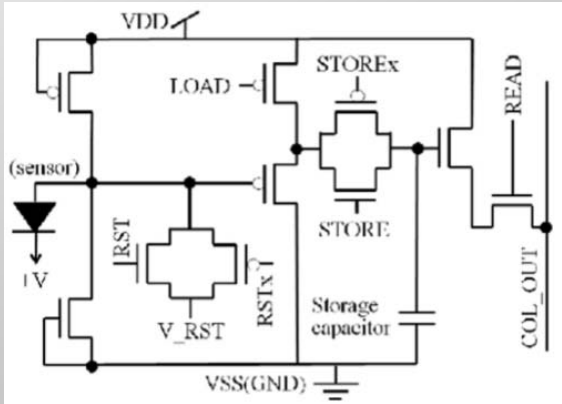


Fig. 3. On-pixel circuit of INTPIXh2 [11].

HSTD10(2015)

DOUBLE SOI PIXEL

Signal Shape (INTPIXh2)

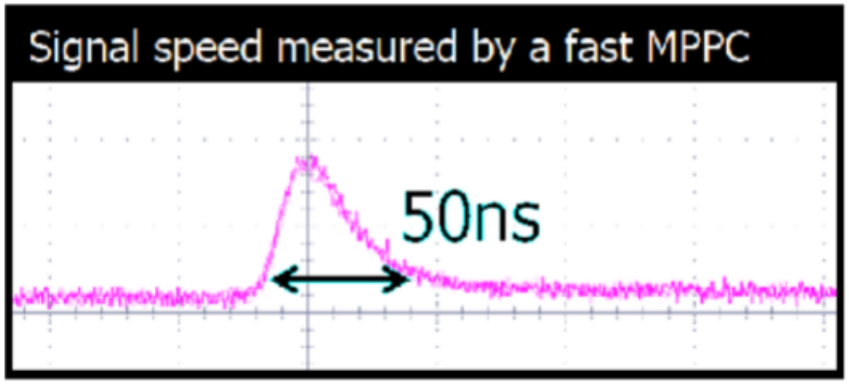
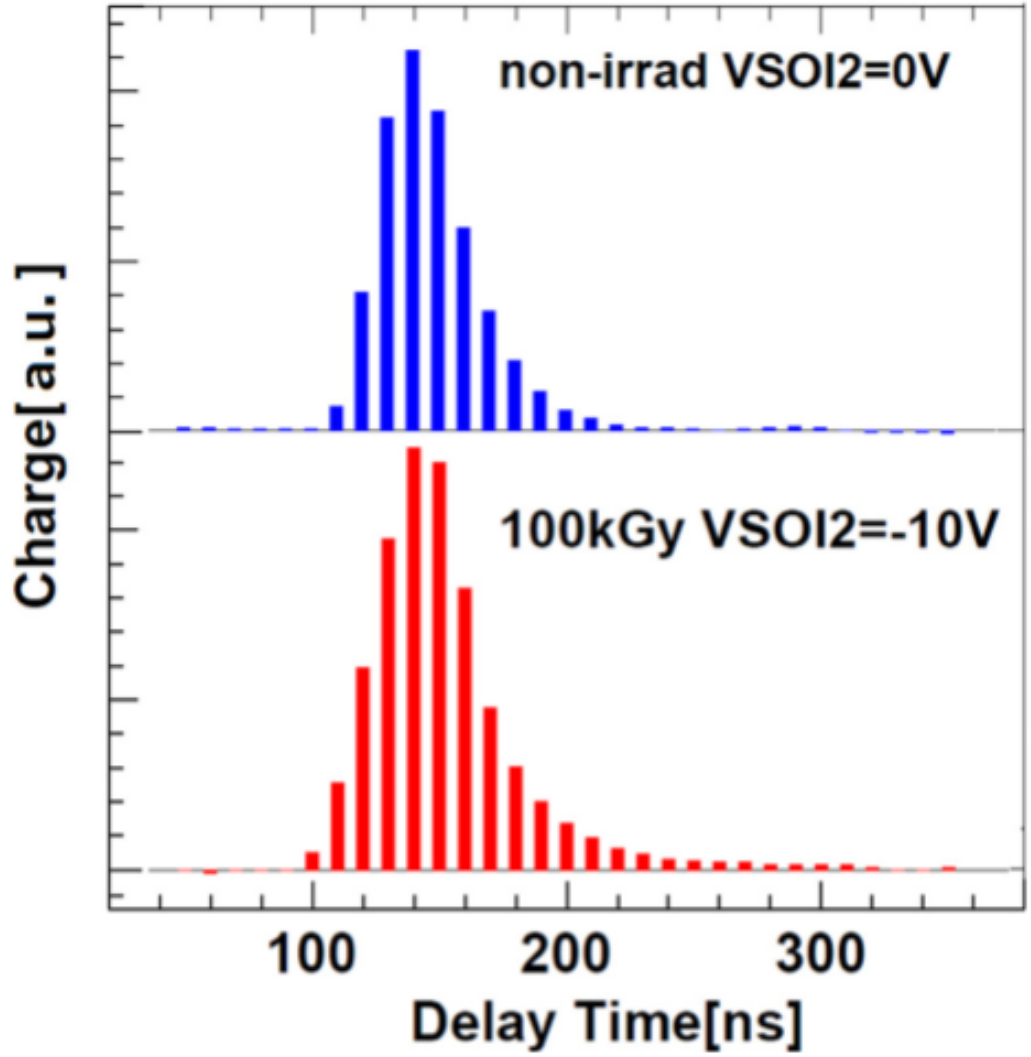


Fig. 8. Signal shape of IR-laser pulse measured with MPPC.

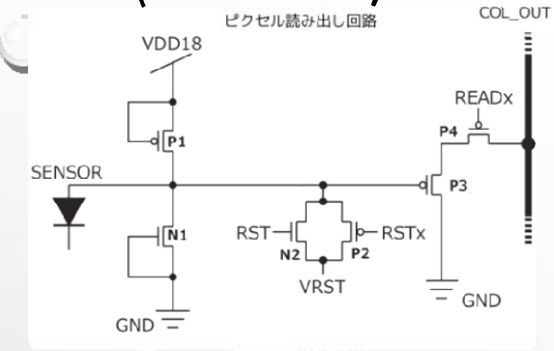
The amplifier is not optimized for fast signal, but radiation-induced degradation in charge collection time seems small.



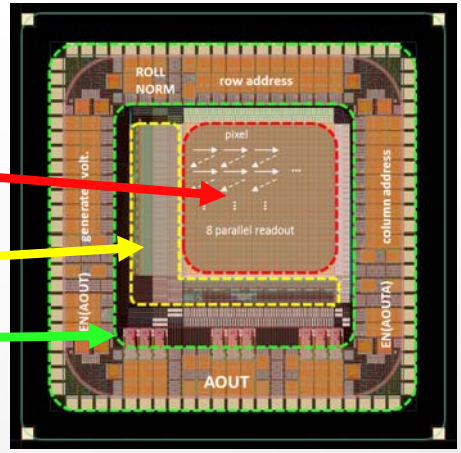
JPS (2016)

DOUBLE SOI – 3 V_{SOI2} CONTROLS

VSOI2=(VSOI2 IO ,VSOI2 pix , VSOI2 dec)



FPIX2



SOI2 PIXEL

SOI2 DECORDER

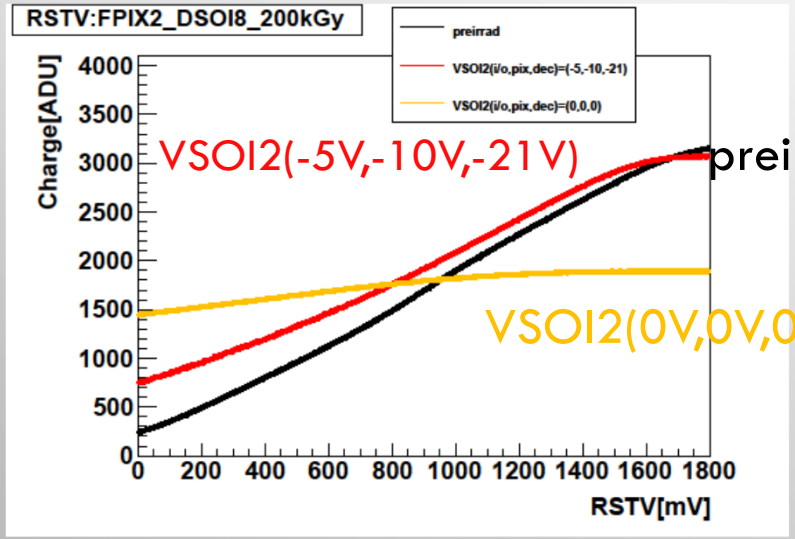
SOI2 I/O

TID most critical on : PIXEL … signal integration

DEC … voltages for gain control

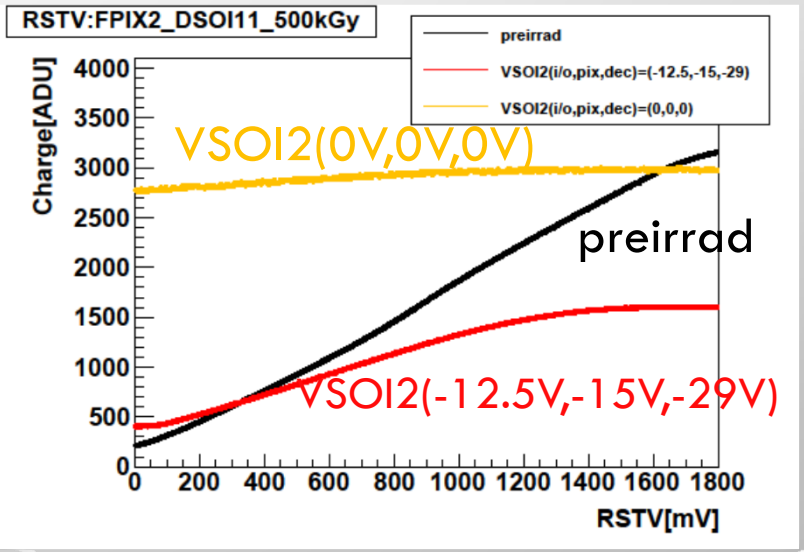
IO … FET functioning for ESD

200kGy



V_{RESET} response almost recovered

500kGy



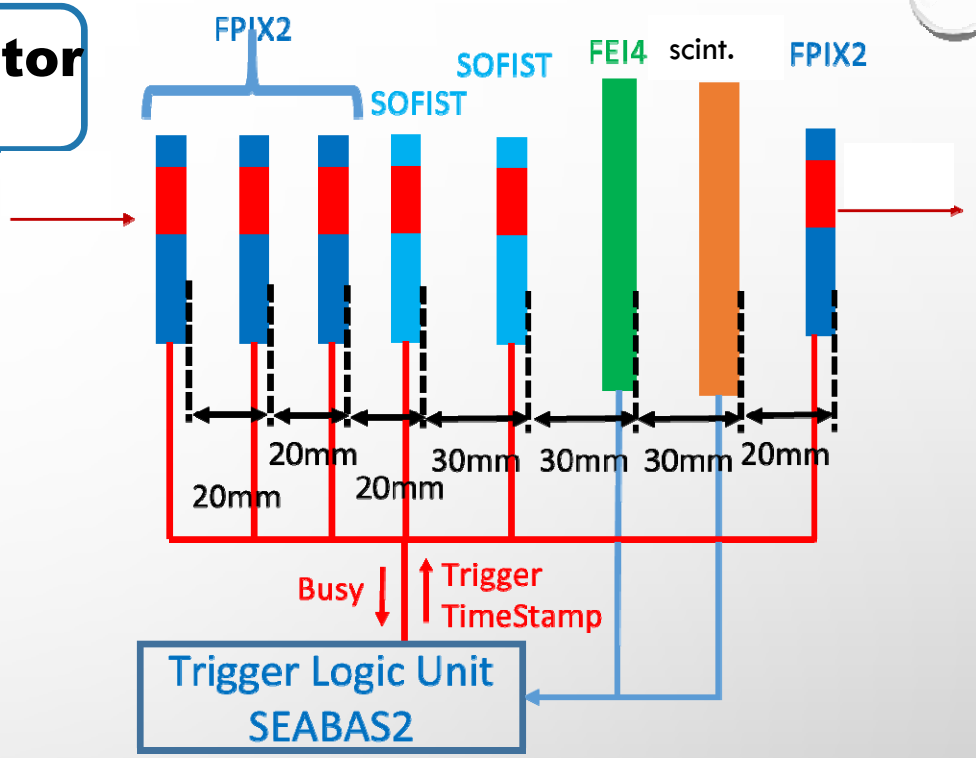
V_{RESET} response partially recovered

Jan (2017)

FNAL TEST BEAM

FTBF: 120GeV protons from Main Injector

4.2s beam spill every 1 minute



R.Nishimura et al. "high speed DAQ system…"

- **Trigger generated by a SEABAS2 board using Scint.(5mm-sq) and ATLAS FE-I4 (2mmx1.75mm ROI)**
- **Data of 4 FPIX2 and 2 SOFIST sensors acquired per TLU request.** DAQ~1.2k/spill
  All R/O boards (SEABAS2) implemented with same TimeStamp firmware
- **Last FPIX2 made accessible for exchanging to irradiated DSOI**

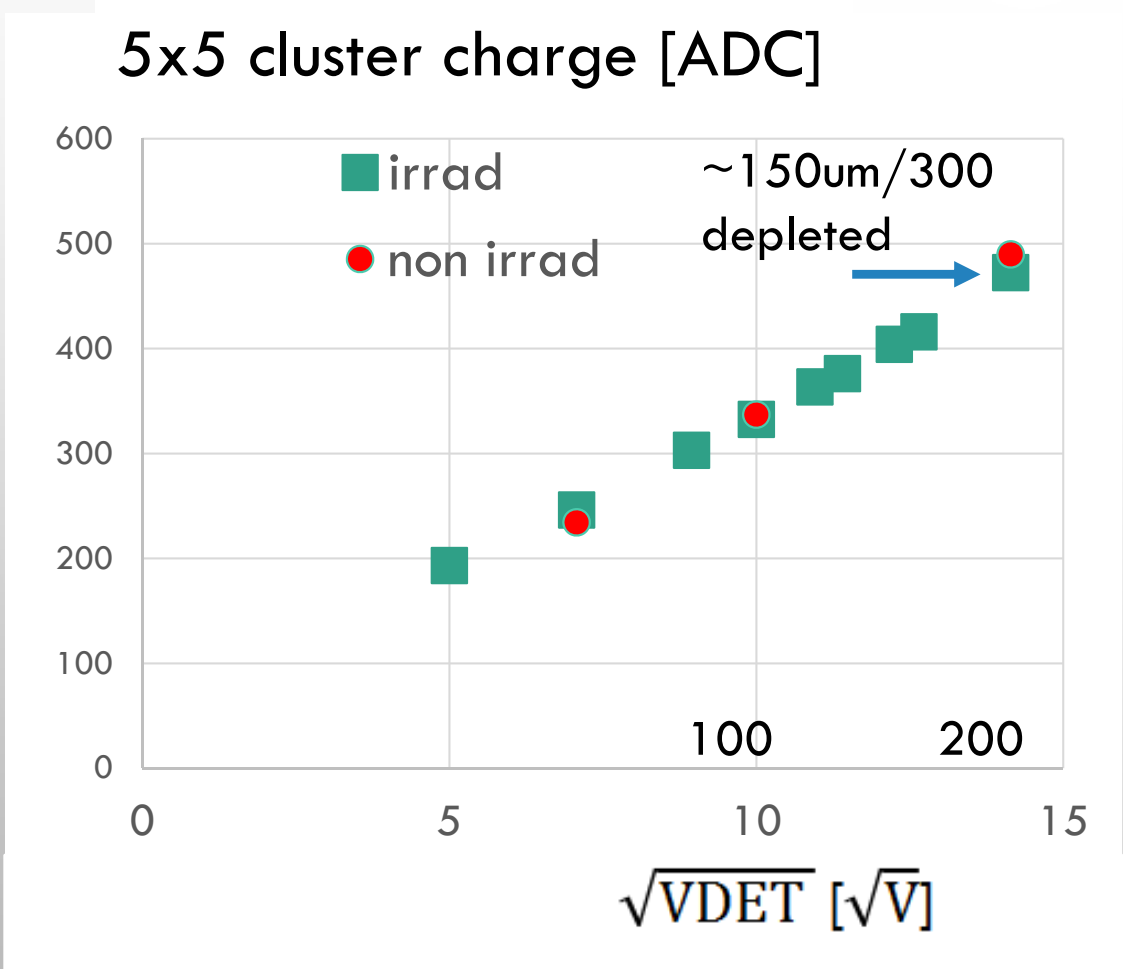
SEABAS2(Soi EvAluation BoArd with Sitcp): 16ch 12bit 40MHz ADCs, Giga-bit Ethernet

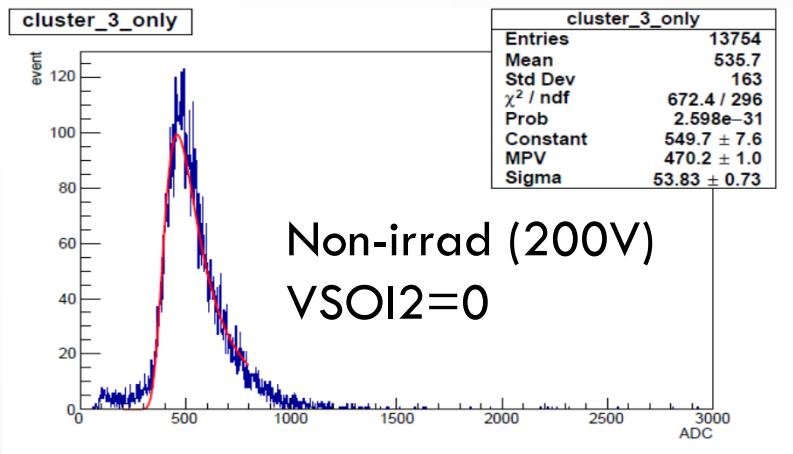
TIPP (2017)

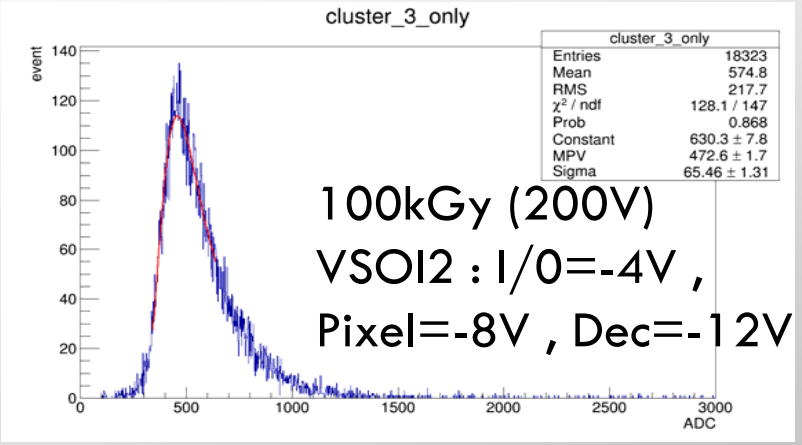
TID DAMAGE COMPENSATION

FNAL TB : FPIX2 100kGy

5x5 cluster charge about the maximum charge pixel in an event



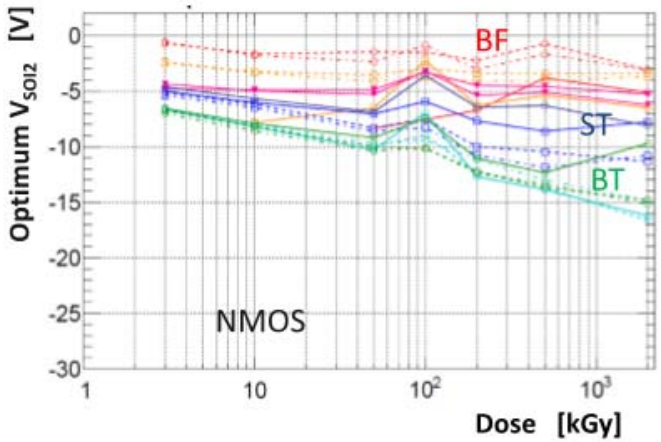


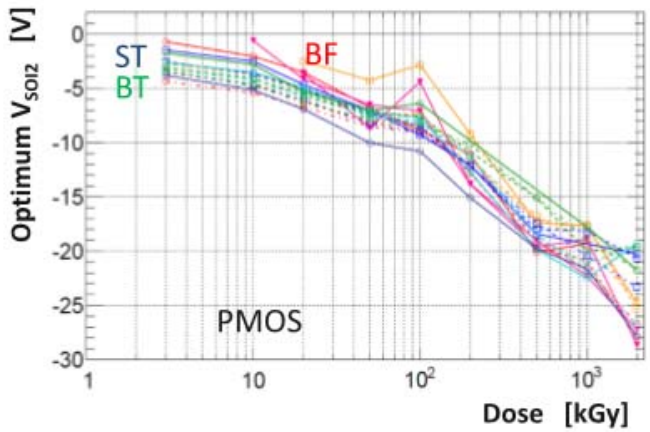


Innovative double-SOI allows operation of SOI devices @ 100kGy

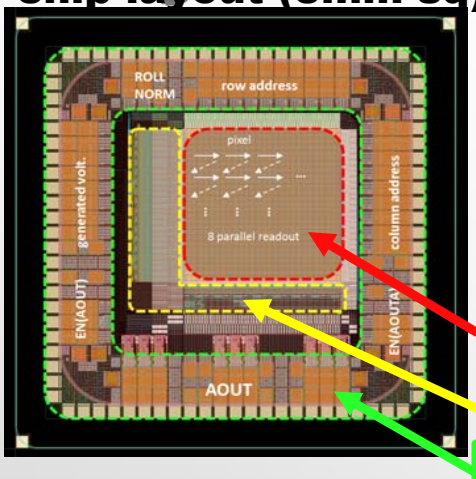
Noise:1.8±0.1 ⇒5.4±0.5@RT

MORE COMPENSATION…





chip layout (3mm-sq)

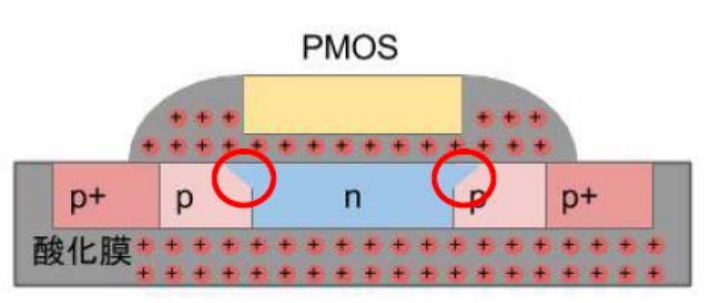


FPIX2
PIXEL
DECODER
I/O

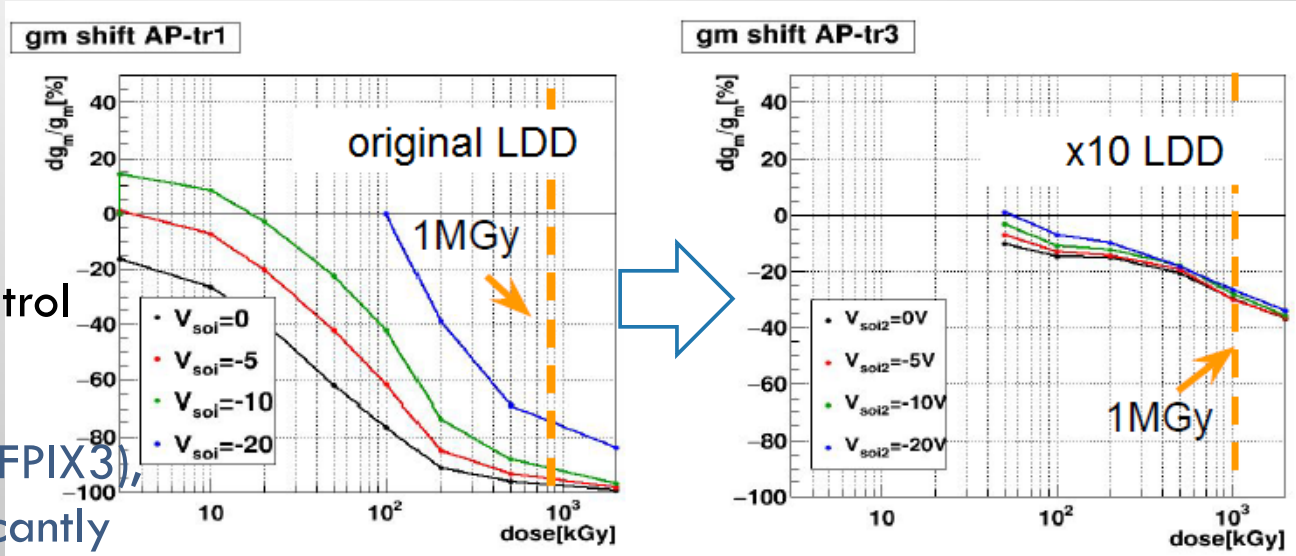
FPIX3
p/n
p/n

Vth shift compensable by applying negative volts to SOI2: optimum volts differ for n/p as dose ~1MGy

✓ Separate n/p SOI2 controls in FPIX3

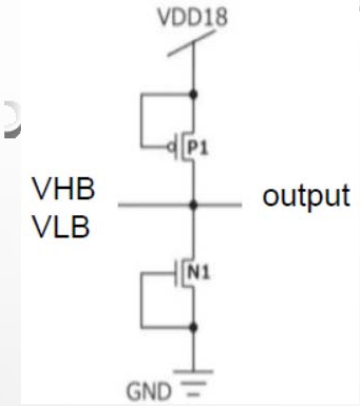


PMOS TID in sidewall: LDD loses control
(LDD: lightly doped drain)

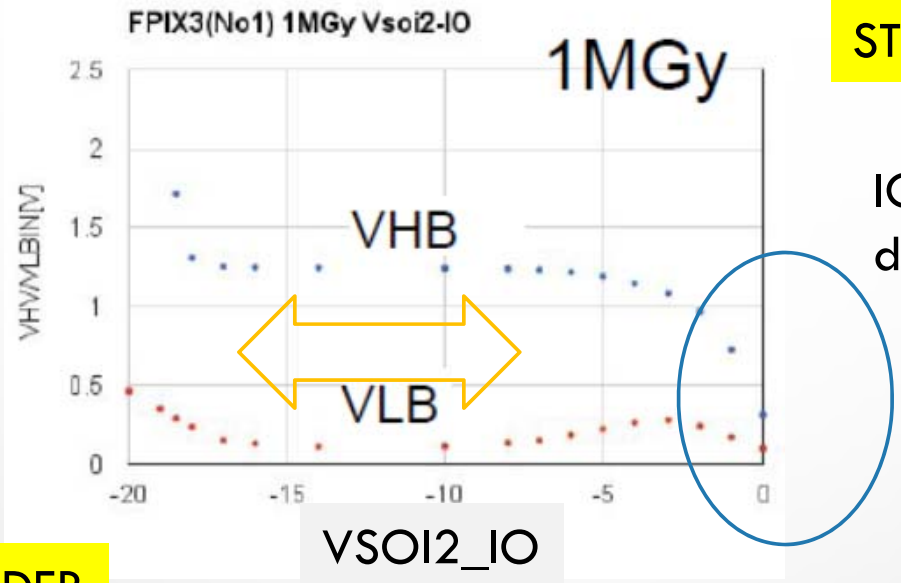


✓ increasing LDD by x10 (FPIX2-.>FPIX3),
Trans-conductance recovered significantly

COMPENSATION TUNING



ESD protection



VSOI2_IO

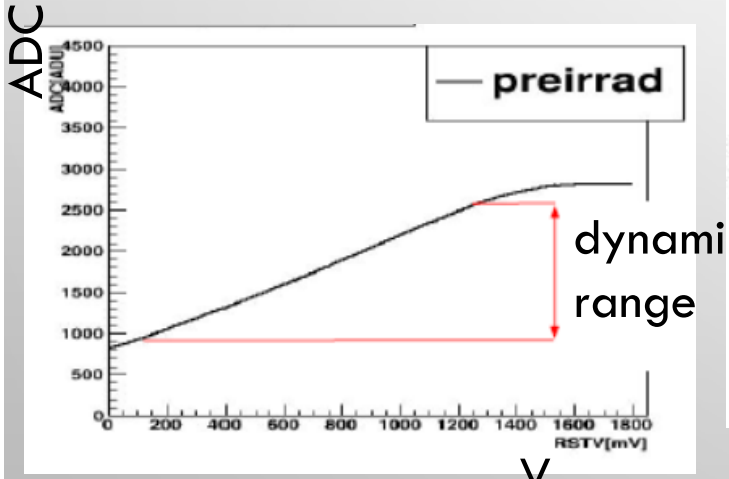
STEP-1 tune IO

IO outputs are clipped due to always "ON" ESD

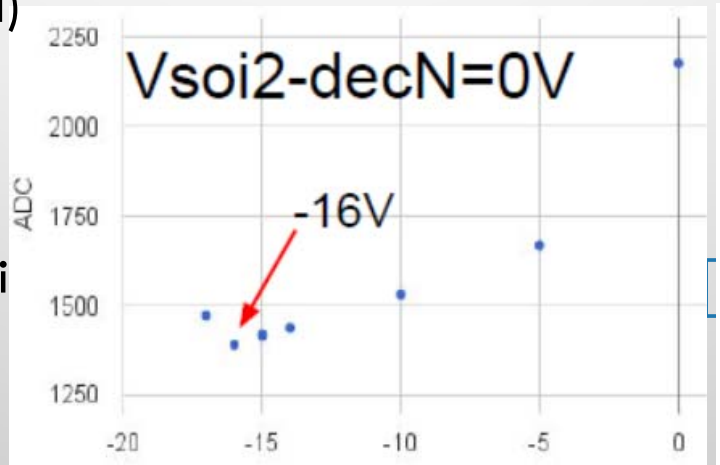
Wide range of VSOI2_IO

STEP-2 tune DECODER

Typical V_{RESET} response (non-irrad)

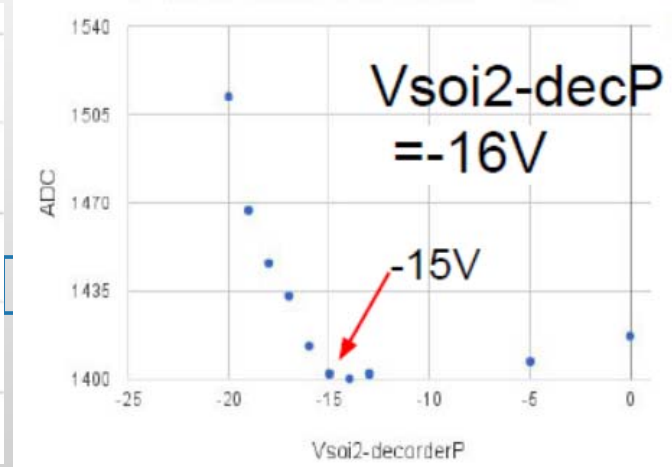


For V_{RESET}=100mV, tune to minimize the output



VSOI2_decP

200kGy

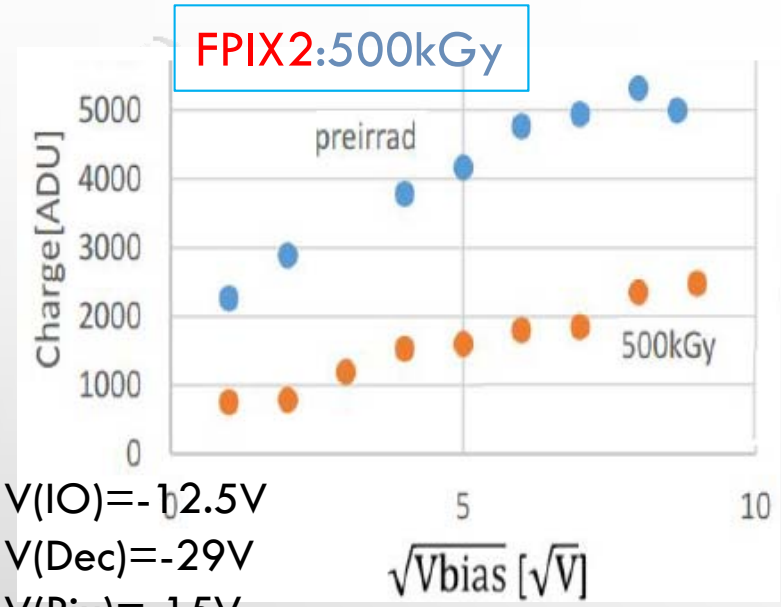


VSOI2_decN

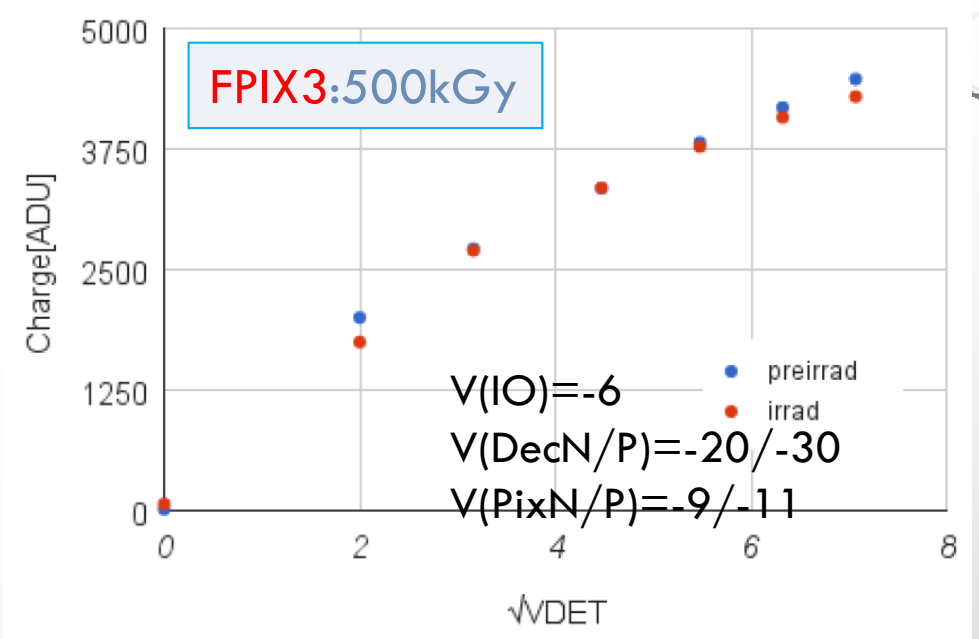
STEP-3 tune PIX to maximize the dynamic range and linearity

TID DAMAGE COMPENSATION

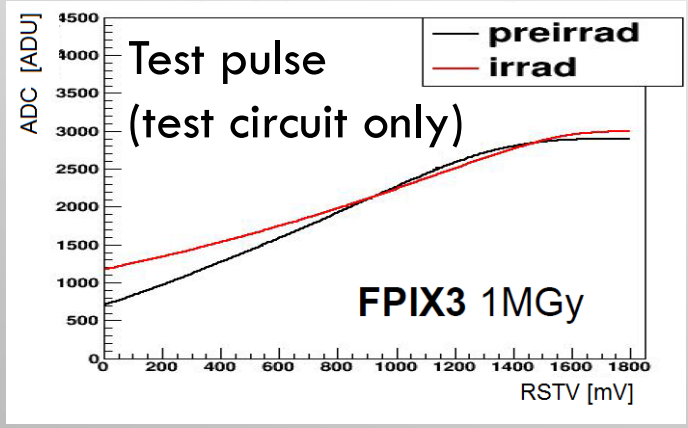
Response to pulsed IR-laser

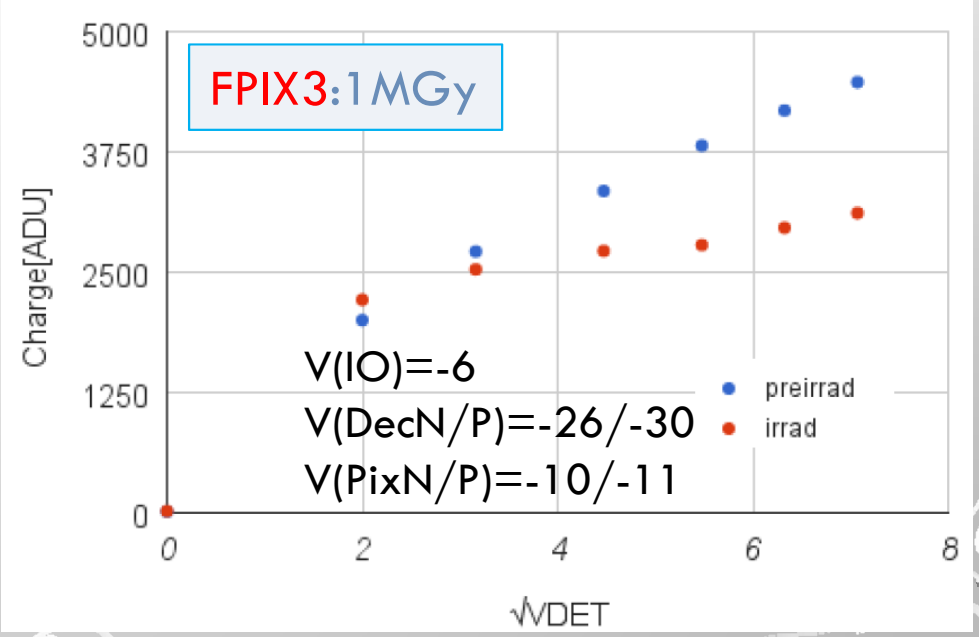


V(IO)=-12.5V
V(Dec)=-29V
V(Pix)=-15V



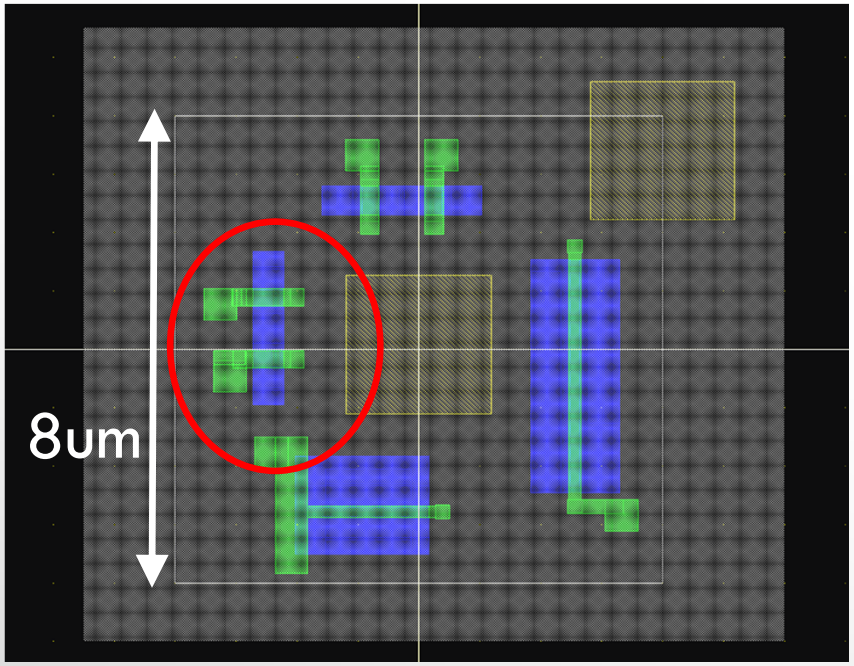
- ✓ Response fully recovered at 500kGy
- ✓ Expect linear response at 1MGy



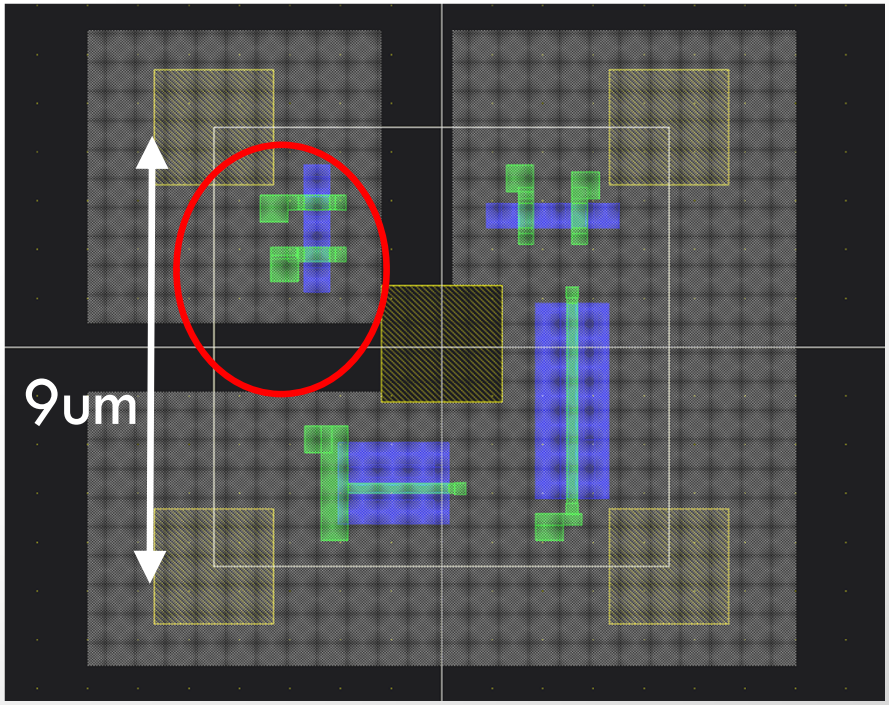


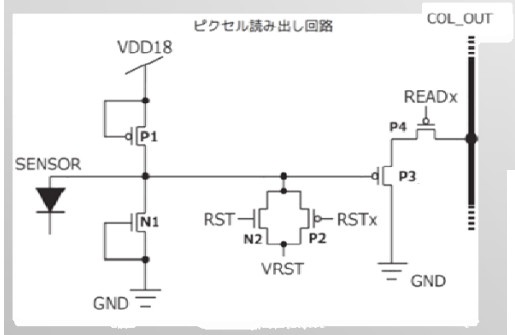
FPIX3 PIXEL LAYOUT

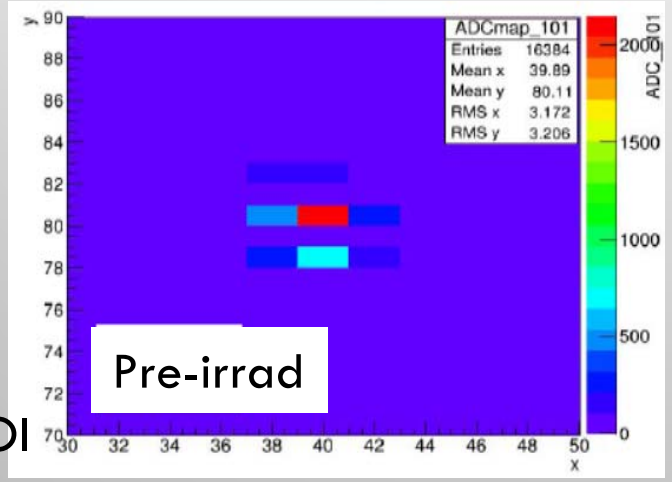
FPIX2

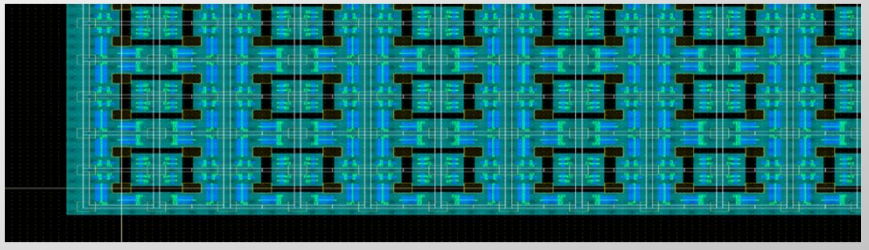


FPIX3









No response from odd-row
OK w/ singleSOI

PIXEL NMOS FETs (N1+N2) located at a corner
One VPIX_n for a group of 2×2 pixels
Rolling shutter R/O resets the signals in next row…

CONCLUSIONS

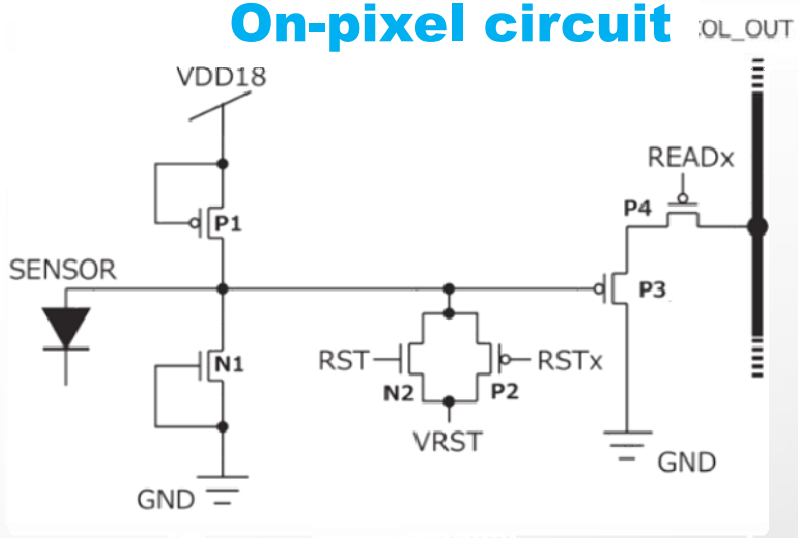
- **TID identified as main concern for SOI applications in high-radiation environment**
- **Innovative Double SOI solved many issues including TID. LDD profile revisited to enhance radiation tolerance**
- **TID tolerance up to 500 kGy is achieved and good performance is expected also at 1 MGy (FPIX3)**
- **SOI pixel (SOFIST) is being developed for the ILC. SOI applications to wider area are encouraged.**

SPARES

FINE-PIXEL DETECTOR: FPIX2

- **Pixel size: 8μm□**
- **#Pixels: 128×128**
- **Handle wafers:**
  >single SOI
  25kΩ·cm p, 500 umt
  >double SOI
  1kΩ·cm p, 300 umt
- **Rolling shutter RO**
  8 parallel outputs

On-pixel circuit

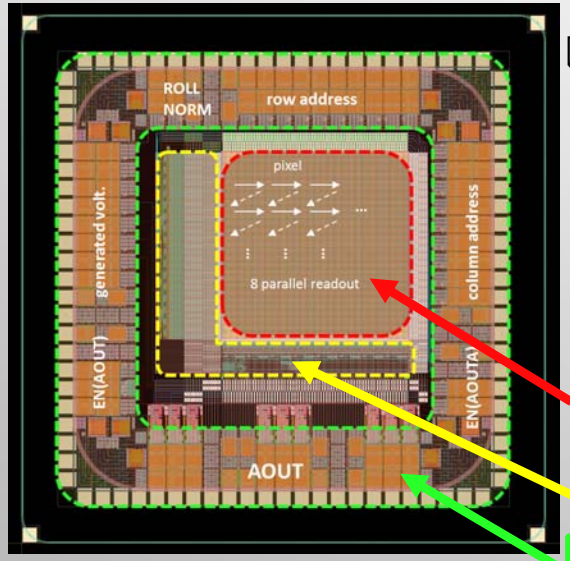


In Development:

- ❑ **to demonstrate excellent spatial resolution achievable with SOI technology (=>tracker for SOFIST TB)**
- ❑ **as demonstrator of TID tolerance (FPIX2 equipped with three middle-SOI regions)**

TID: hole accumulation in BOX/GOX
Middle-SOI: compensate TID effects by applied negative voltages

chip layout (3mm-sq)



PIXEL

DECODER

I/O

Analog signals are digitized (2ms) by external SEABAS2 12-b ADCs (8 parallel)

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