中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

# A prototype SOI pixel sensor for CEPC vertex

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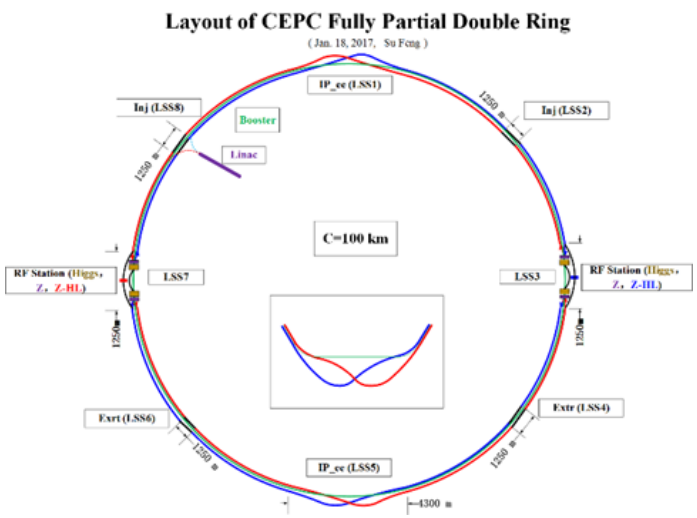
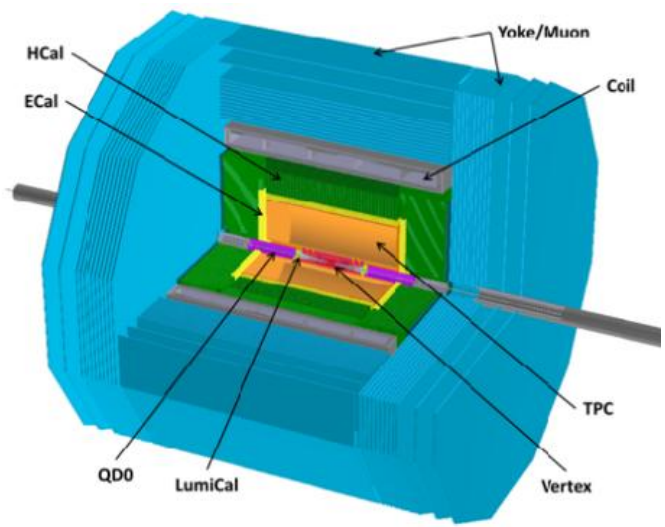
# outline

- Introduction for CEPC vertex
  - Physics driven requirements
  - Technical challenges
  - Advantages of SOI technology for tracking
- Concept of CPV2 chip
- Basic characterization
  - Sensor test
  - calibration
  - noise test
- Single point resolution measurement
  - Infrared laser test setup
  - Laser beam response
  - Measurement results
- Conclusion and outlook

# Introduction

- High Energy Circular Electron Positron Collider (CEPC)
  - $e^+ e^-$ Higgs and Z factory
  - $E_{cm} \approx 240$GeV, luminosity $\approx 2 \times 10^{34}$ $cm^{-2}s^{-1}$ @Higgs
  - Higgs precision 1% or better



# Physics driven requirements

**Table 6.1** Required performance of the CEPC sub-detectors for critical benchmark Higgs processes.

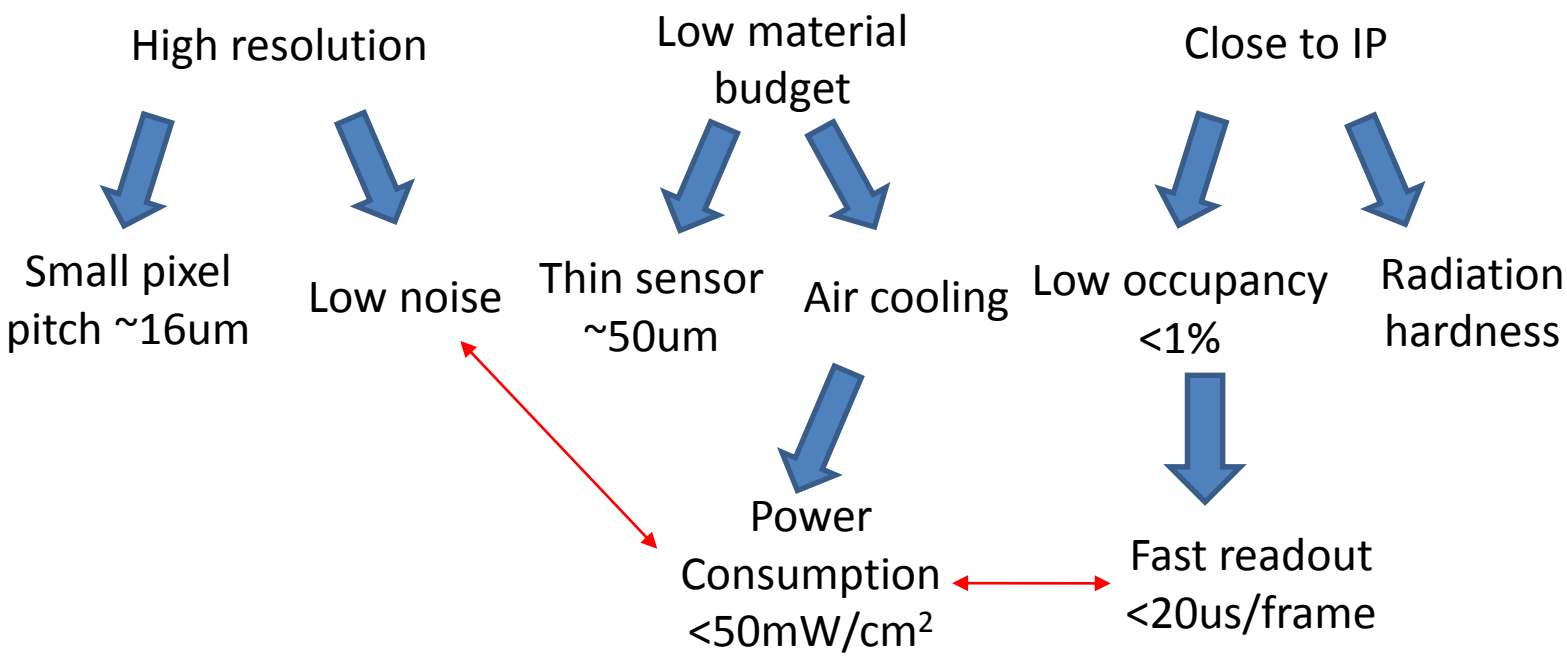
| Physics Process | Measured Quantity | Critical Detector | Required Performance |
|---|---|---|---|
| $ZH \to \ell^+\ell^- X$ | Higgs mass, cross section | Tracker | $\Delta(1/p_{\mathrm{T}}) \sim 2 \times 10^{-5}$ |
| $H \to \mu^+\mu^-$ | $\mathrm{BR}(H \to \mu^+\mu^-)$ | | $\oplus 1 \times 10^{-3}/(p_{\mathrm{T}} \sin\theta)$ |
| $H \to b\bar{b},\ c\bar{c},\ gg$ | $\mathrm{BR}(H \to b\bar{b},\ c\bar{c},\ gg)$ | Vertex | $\sigma_{r\phi} \sim 5 \oplus 10/(p \sin^{3/2}\theta)\ \mu\mathrm{m}$ |
| $H \to q\bar{q},\ VV$ | $\mathrm{BR}(H \to q\bar{q},\ VV)$ | ECAL, HCAL | $\sigma_E^{\mathrm{jet}}/E \sim 3-4\%$ |
| $H \to \gamma\gamma$ | $\mathrm{BR}(H \to \gamma\gamma)$ | ECAL | $\sigma_E \sim 16\%/\sqrt{E} \oplus 1\%$ (GeV) |

- excellent tagging capability of b-/c-quark jets and τ-lepton
  - Impact parameter resolution, $\sigma(r\phi) = a \oplus \frac{b}{p(\mathrm{GeV})\sin^{3/2}\theta}\ \mu\mathrm{m}$ a=5, b=10
- Design requirements on vertex:
  - Single point resolution near the IP: ≤ 3 μm
  - Material budget: ≤ 0.15% $X_0$/layer
  - Very close to IP (<16mm)

Continuous operation with ~500ns bunch spacing for Higgs

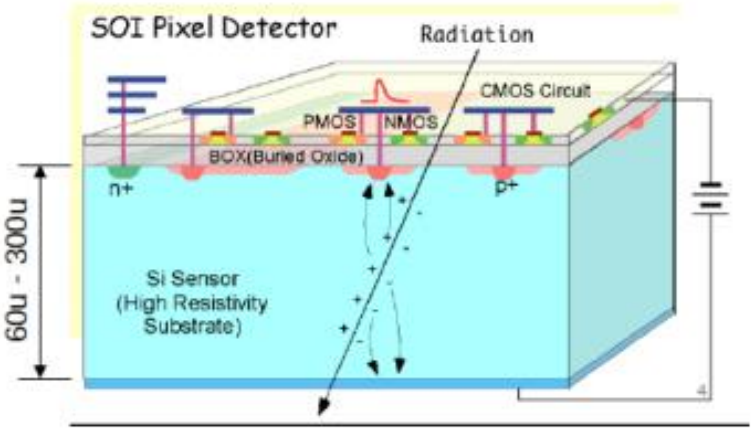
# Technical challenges

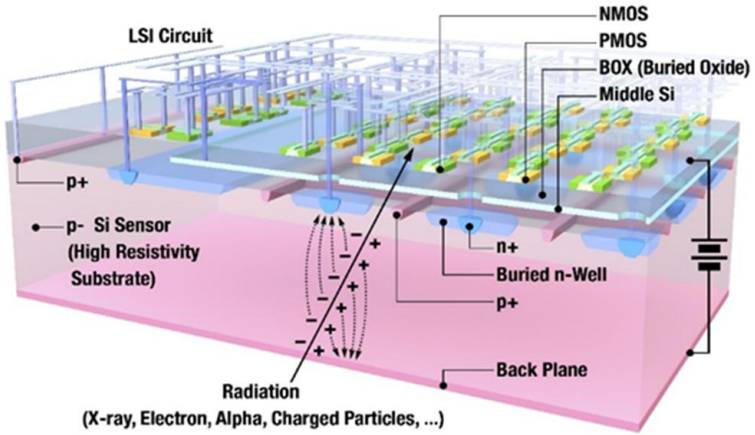
- vertex design requirement leads to technical challenges
  - Technical target is a compromise of all design details



# SOI for tracking

- Features of SOI technology for tracking
  - Full CMOS circuit at 0.2um process node
  - High resistive (up to >10kΩcm) substrate, full depletion/over depletion(large signal and fast charge collection)
  - Pixel pitch below 10um possible
  - Sensor can be thinned to ~50um
  - Double SOI wafer and process available

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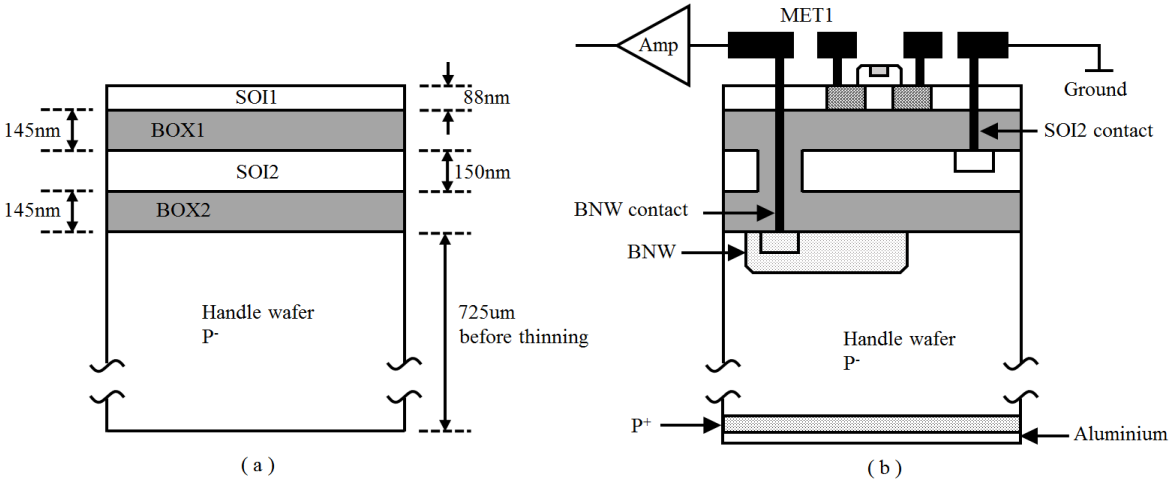
# CPV2 chip concept

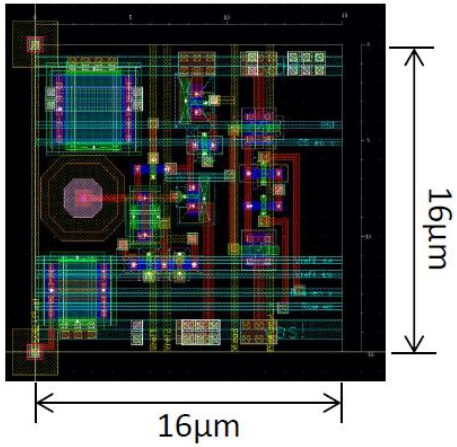
- Double-SOI wafer
  - Second SOI layer as shielding between Front-end and sensing diodes
  - Compensation voltage can be applied to mitigate TID effect
  - High resistive substrate: FZ(p) ~1kΩcm
  - Thinning the sensor down to 75um(usually 300um)



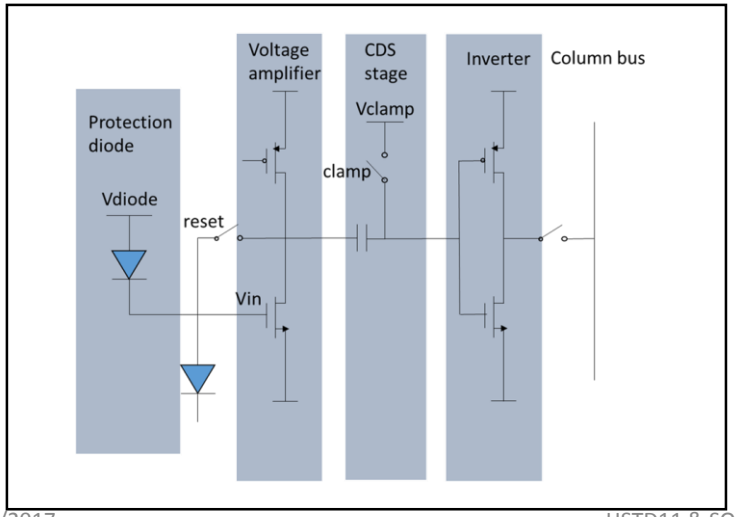
# CPV2 chip concept

- Fine pitch matrix with in-pixel discriminator
  - 16um pitch and digital readout to achieve single point resolution < 3um
  - In-pixel discriminator to enable a low power operation in a continuously colliding mode
  - Sensing diode, amplifier, CDS stage, discriminator
  - Half of matrix are analog readout for calibration

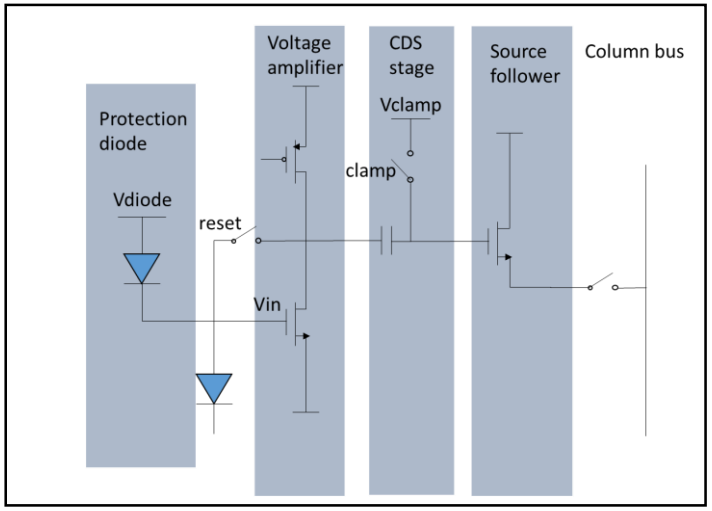
CPV2 pixel layout




CPV2 digital blocks




CPV2 analog blocks



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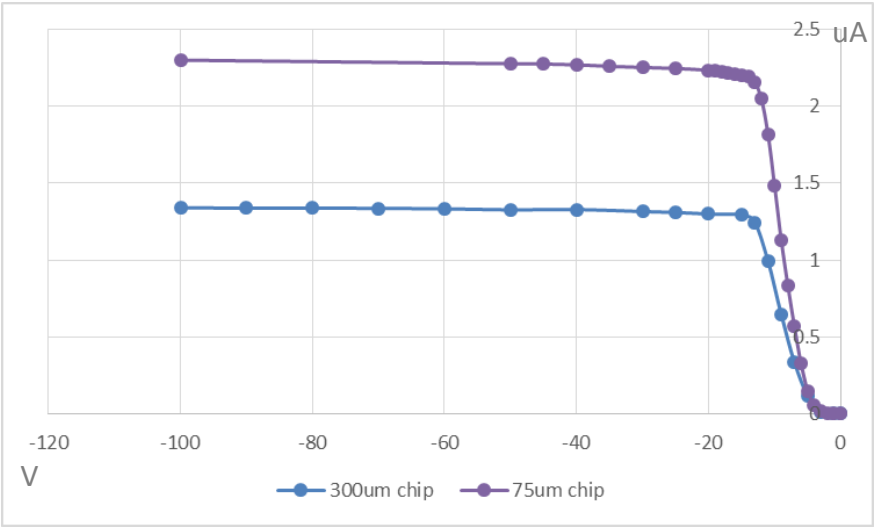
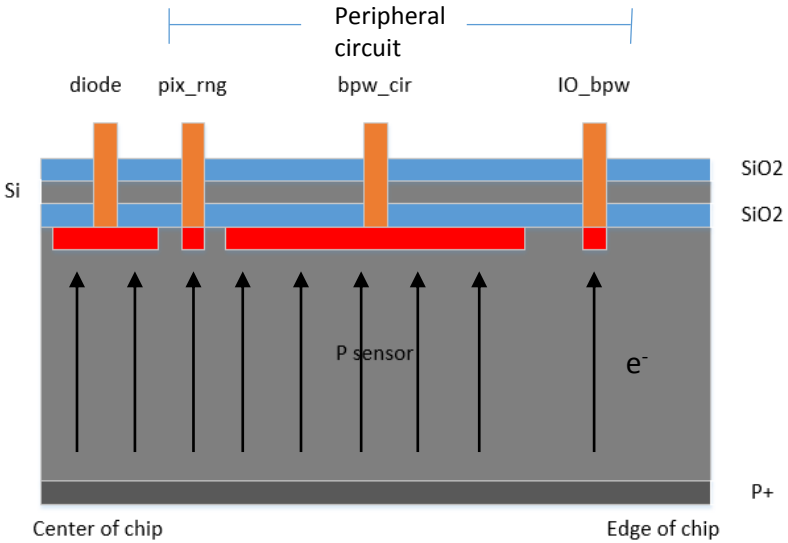
# Sensor test

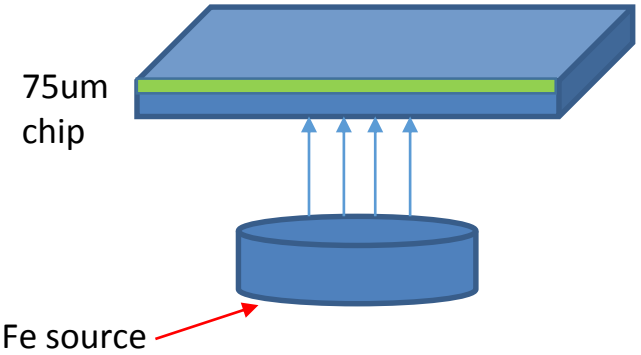
- I-V curve
  - Total Leakage current reaches the plateau when bias voltage is -15V
  - No breakdown at high voltage
  - Thinning chip has larger leakage current
  - Diode current is very small both (~nA/total pixel array), below the accuracy of current meter

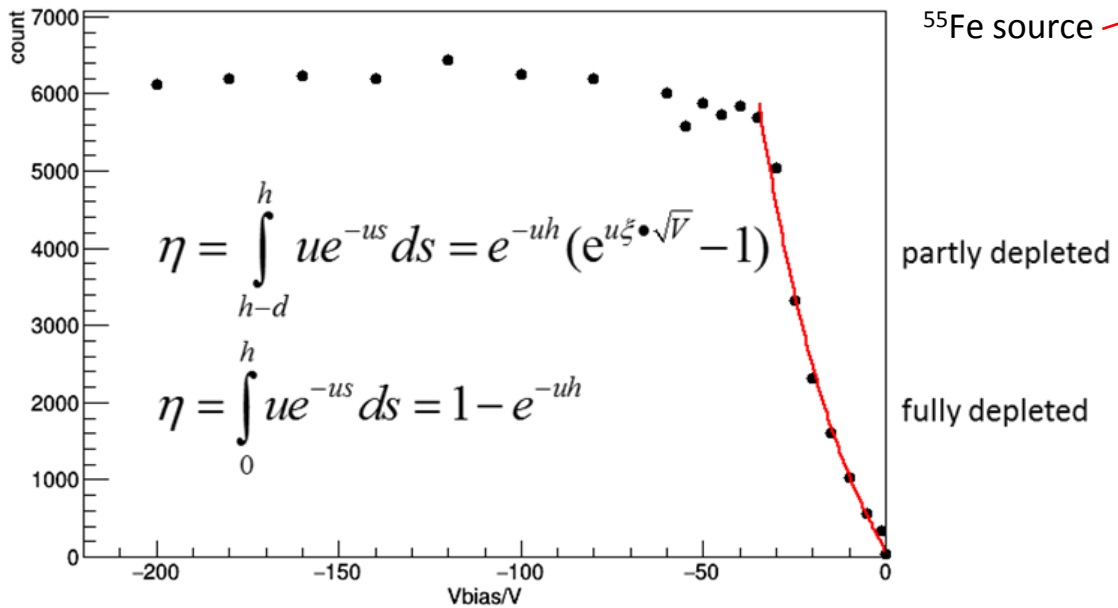


# Sensor test

- $^{55}$Fe signal Efficiency versus bias voltage
  - x-ray illuminates the sensor from backside
  - plateau reached @$V_{bias}$ = -30V
  - An evidence of fully-depleted sensor



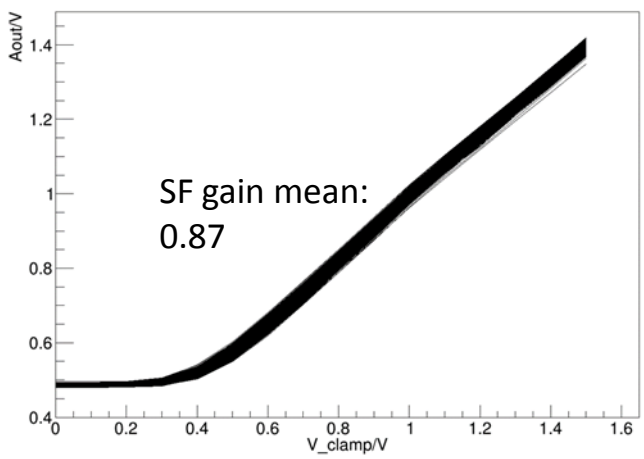



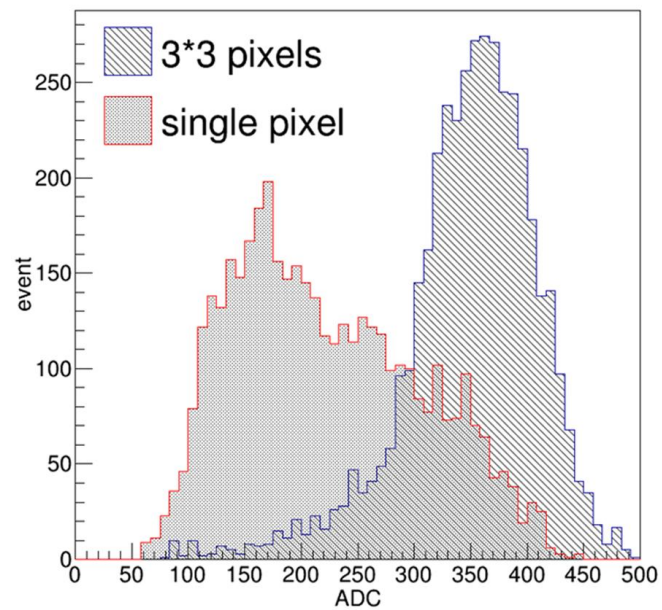

$$\eta = \int_{h-d}^{h} u e^{-us} ds = e^{-uh}(e^{u\xi \bullet \sqrt{V}} - 1)$$

$$\eta = \int_{0}^{h} u e^{-us} ds = 1 - e^{-uh}$$

# Calibration

- Charge voltage factor (CVF)
  - $^{55}Fe$ 5.9KeV X-ray@1640$e^-$
  - SF gain measured 0.87
  - Most probable signal amplitude around 180ADC in single pixel mode
  - A peak at 360ADC in 3×3 pixel cluster mode
  - CVF: 123.3uV/$e^-$ @source follower input

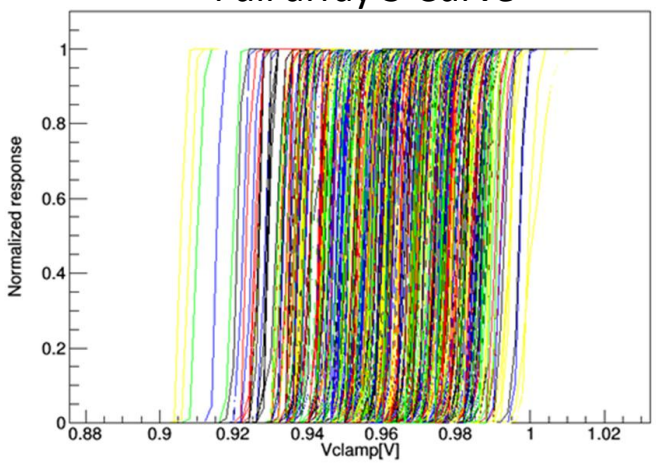


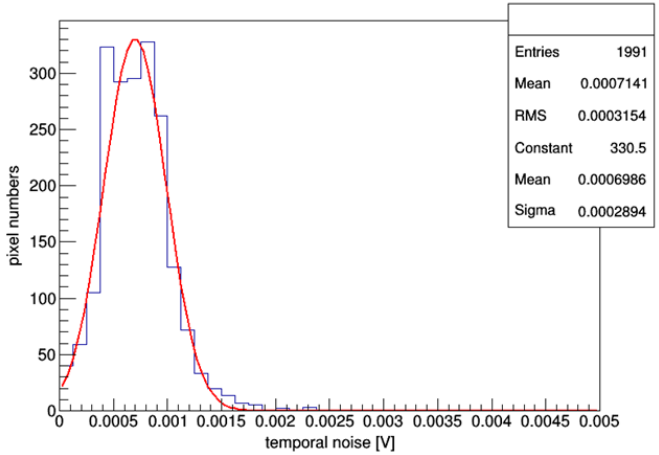



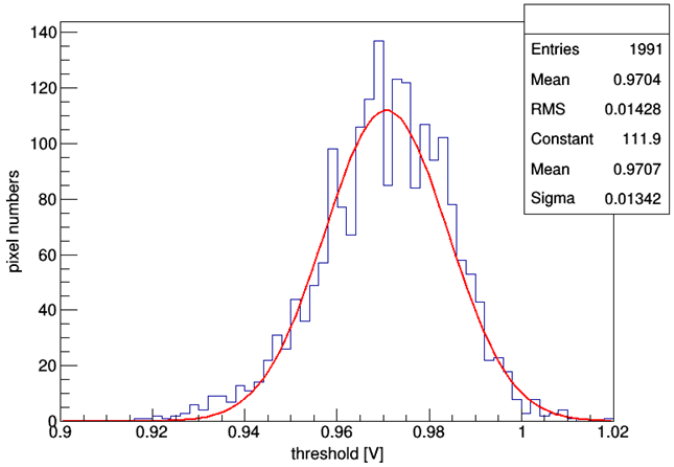
# Noise

- Temporal noise and FPN
  - S-curve measured on full pixel array
  - TN ~6e$^-$
  - Threshold dispersion (FPN) ~114e$^-$
  - Offset cancellation is needed

Full array S-Curve



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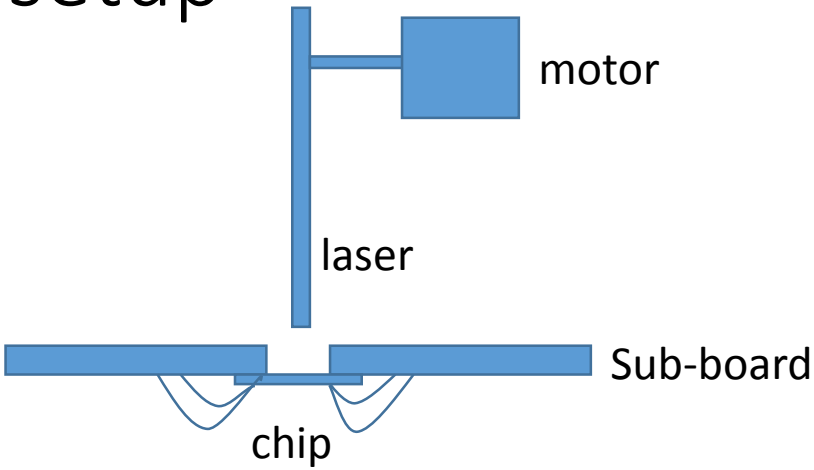
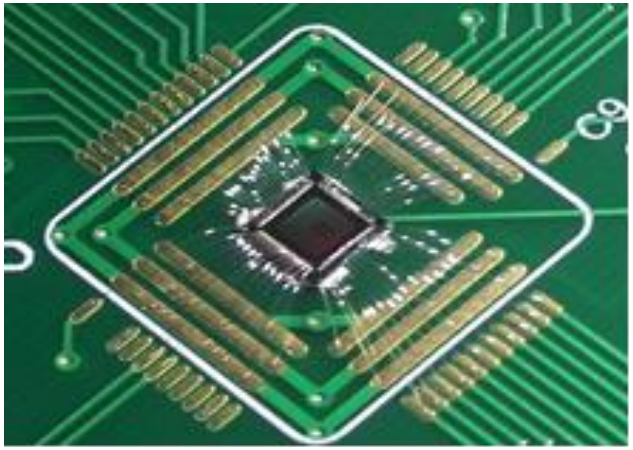
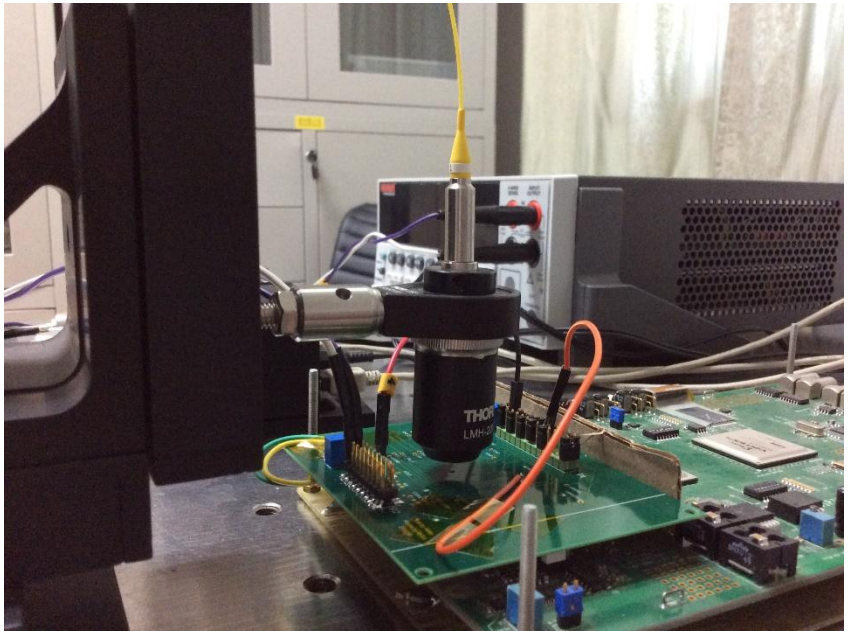
# Experiment setup



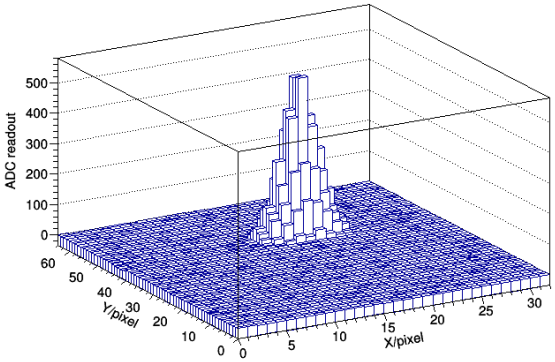

- 1064nm laser beam
  - optical lens to focus laser
- 3-dimensional stepping motor
  - accuracy: 0.1um
- Thinning chip
  - wire-bonding on sub-board
  - illuminate from backside (no aluminum)



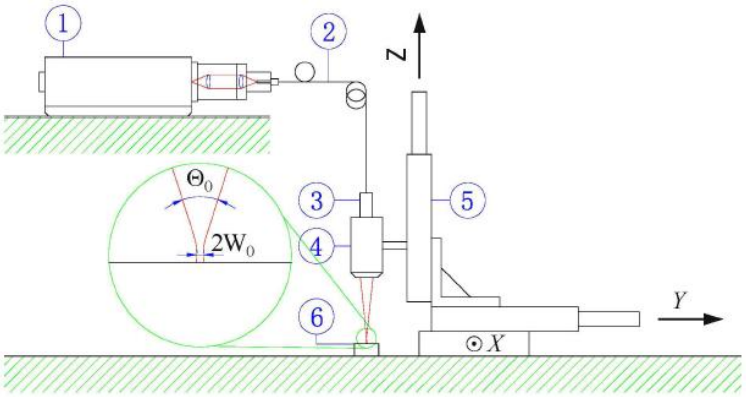


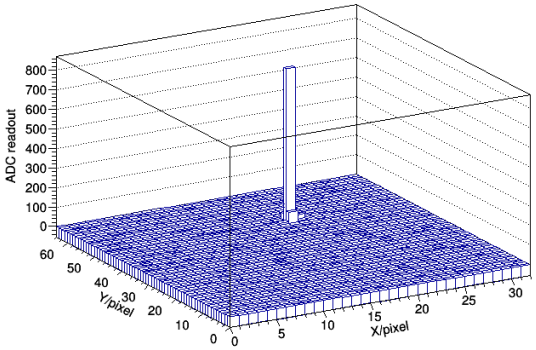
# Laser beam

- Timing
  - Triggered by the frame start signal
  - Synchronized with rolling shutter readout
- Focusing with analog pixel as a monitor
  - Achieve the smallest beam cluster
  - Calibrate the equivalent electron number of laser energy
- beam waist diameter
  - 3.4um




before focusing

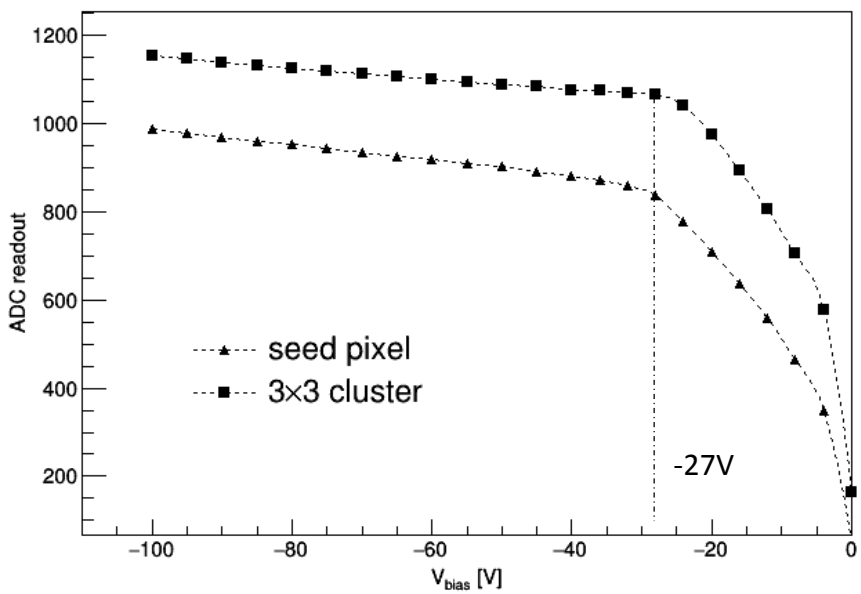



after focusing

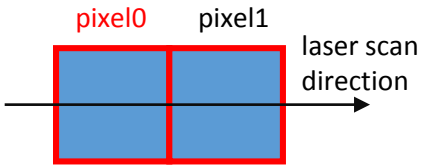
# sensor test by laser

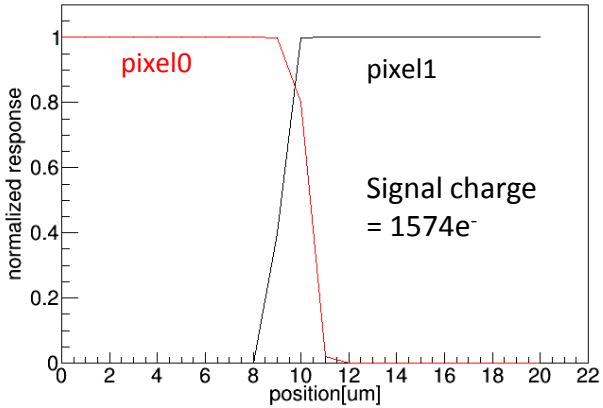
- Laser signal versus bias voltage
  - Inflection point @$V_{bias}$ = -27V
  - An evidence of fully-depleted sensor
  - Slow increasing maybe caused by signal collection efficiency
  - Choosing $V_{bias}$ = -100V in the following laser scan test

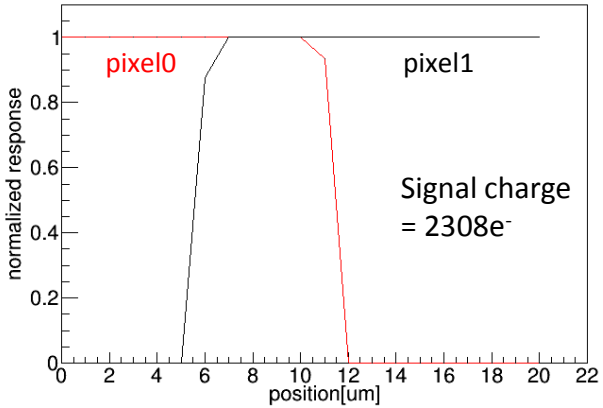


# Laser scan with different laser intensity

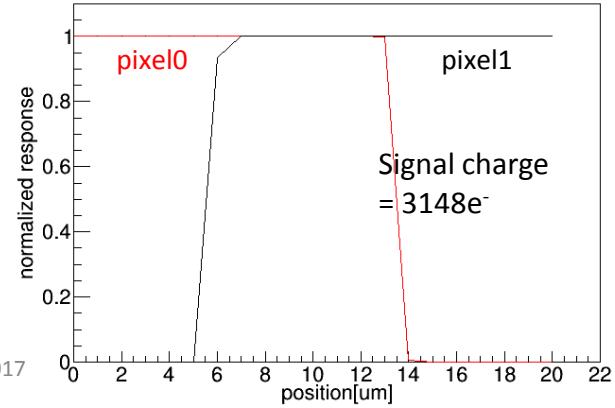
- Scan two adjacent digital pixels
  - Step size of 1um
  - Threshold is fixed (no noise hits)

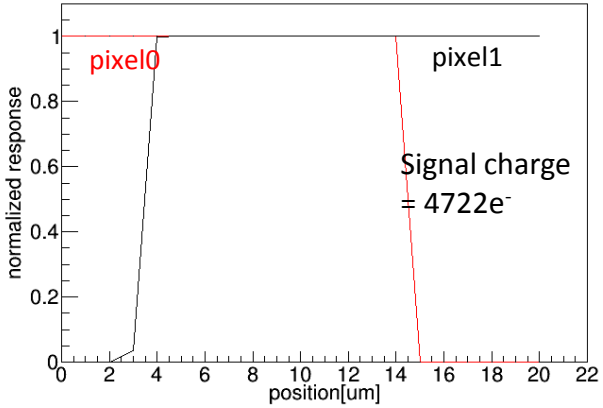


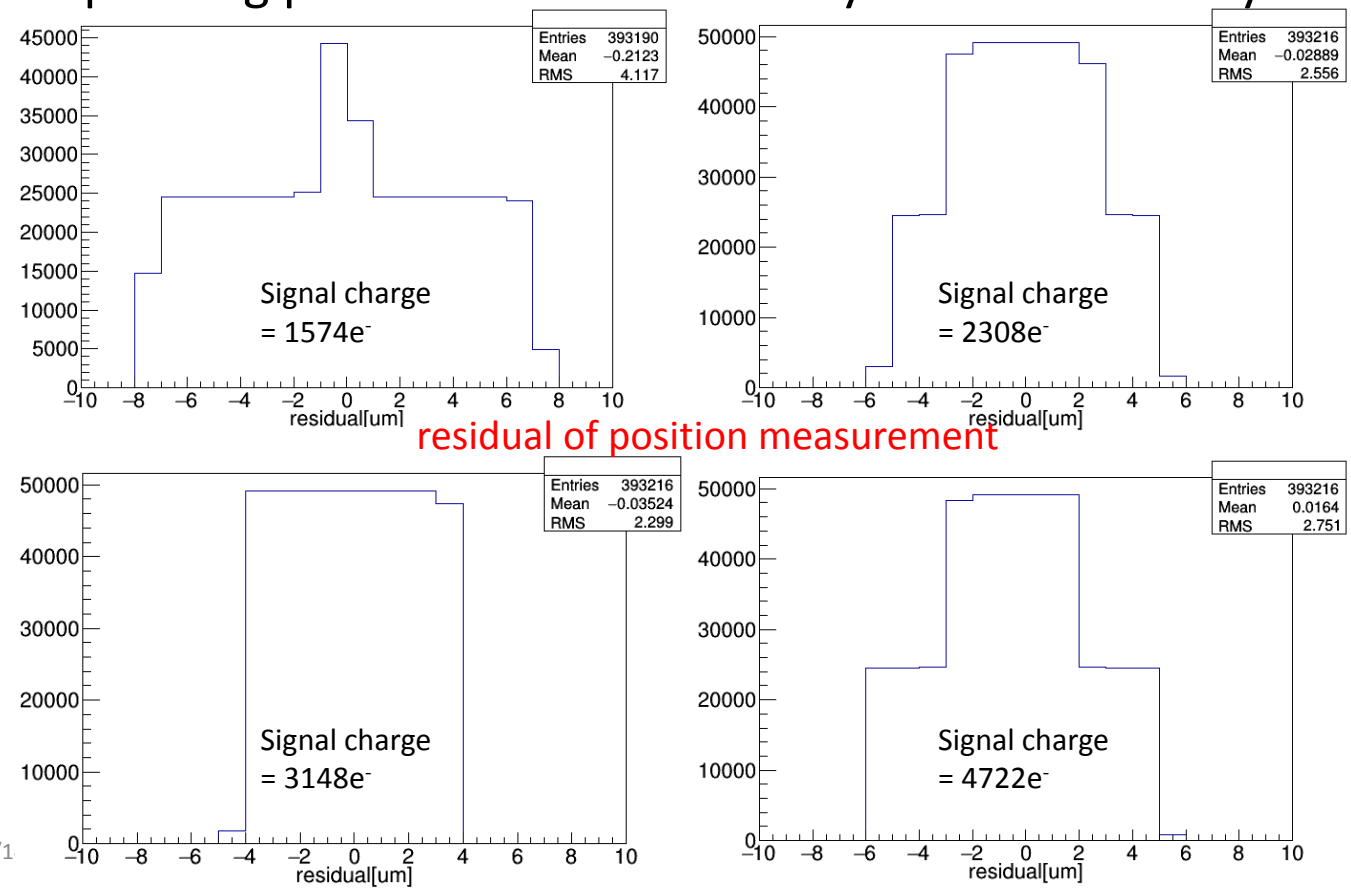

Normalized response =number of hit/number of pulse



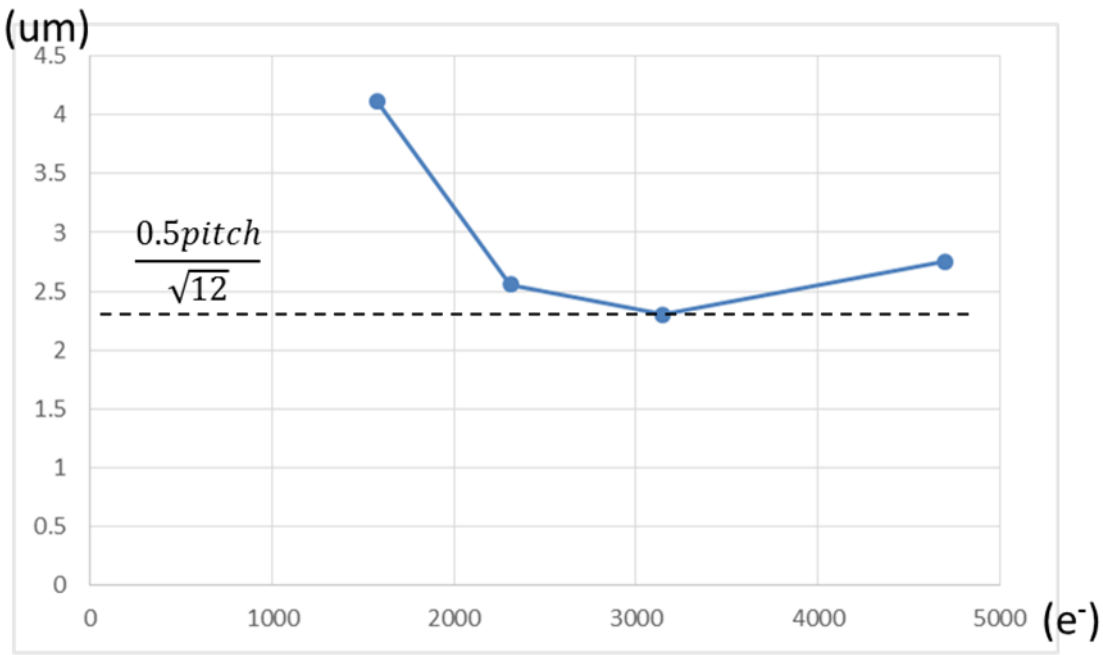
# Spatial resolution by laser

- Actual position decided by motor
- Responding position reconstructed by Center of Gravity



# Spatial resolution by laser

- Spatial resolution versus signal level
  - Get the best resolution of 2.3um at around 3000e$^-$ signal level



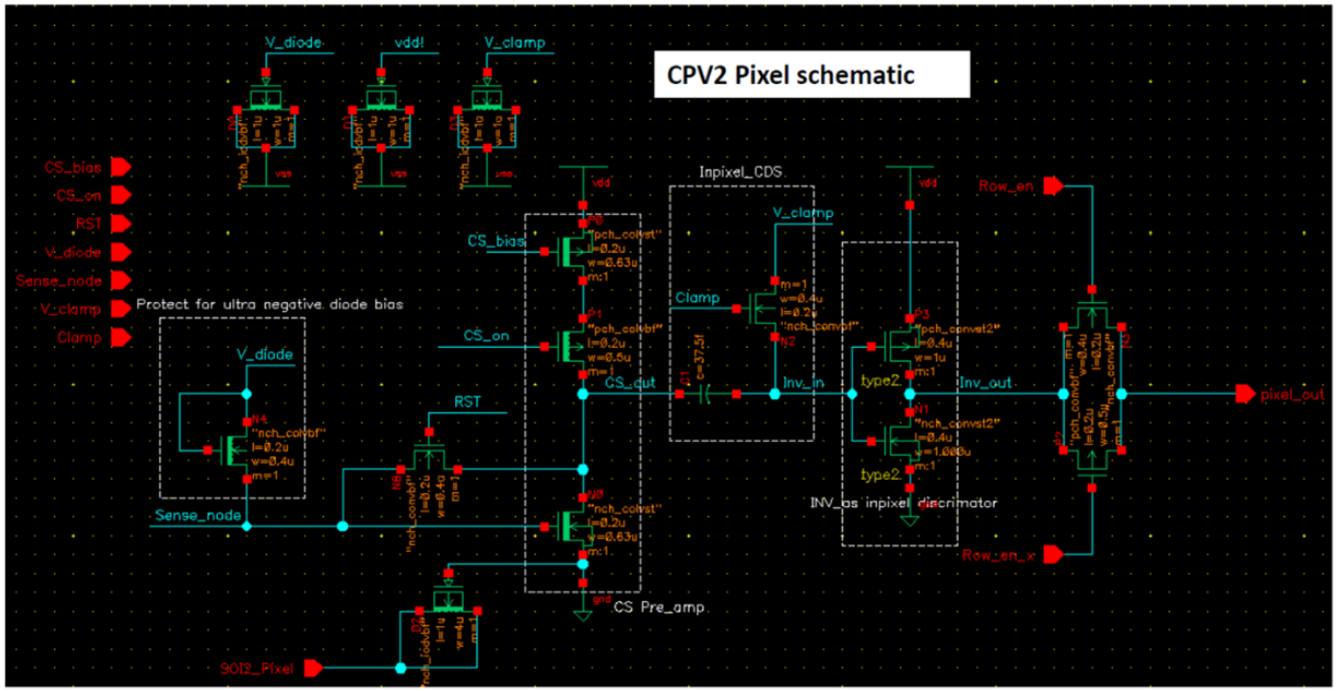
# Conclusion and outlook

- A prototype SOI pixel sensor for CEPC vertex
  - 16um pitch and 75um thickness D-SOI chip
  - Validate the feasibility of thinning process
  - Fully depleted sensor @$V_{bias}$ = -30V
  - Low noise ($6e^-$) of single pixel is achieved
  - The demonstration of a single point resolution below 3um
- CPV3 will follow up
  - Fix the problems in CPV2
  - Reduce the threshold distribution
  - Compatible with 3D integration
  - Characterized by particle beam test

# Thanks for your attention!

# Backup

- CPV2 pixel schematic



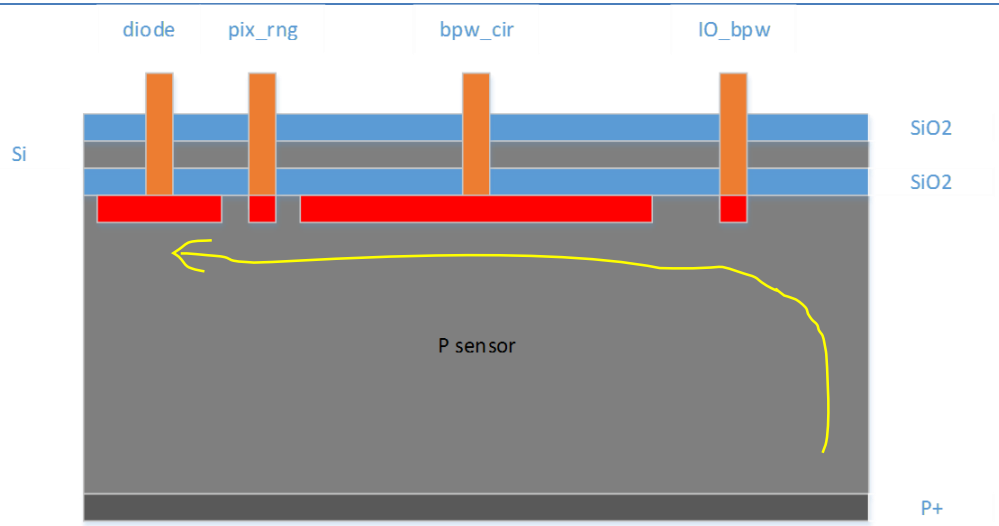

Sensing node | Pre_amp stage | Offset cancellation | INV stage | Switch for row select

3

# Backup

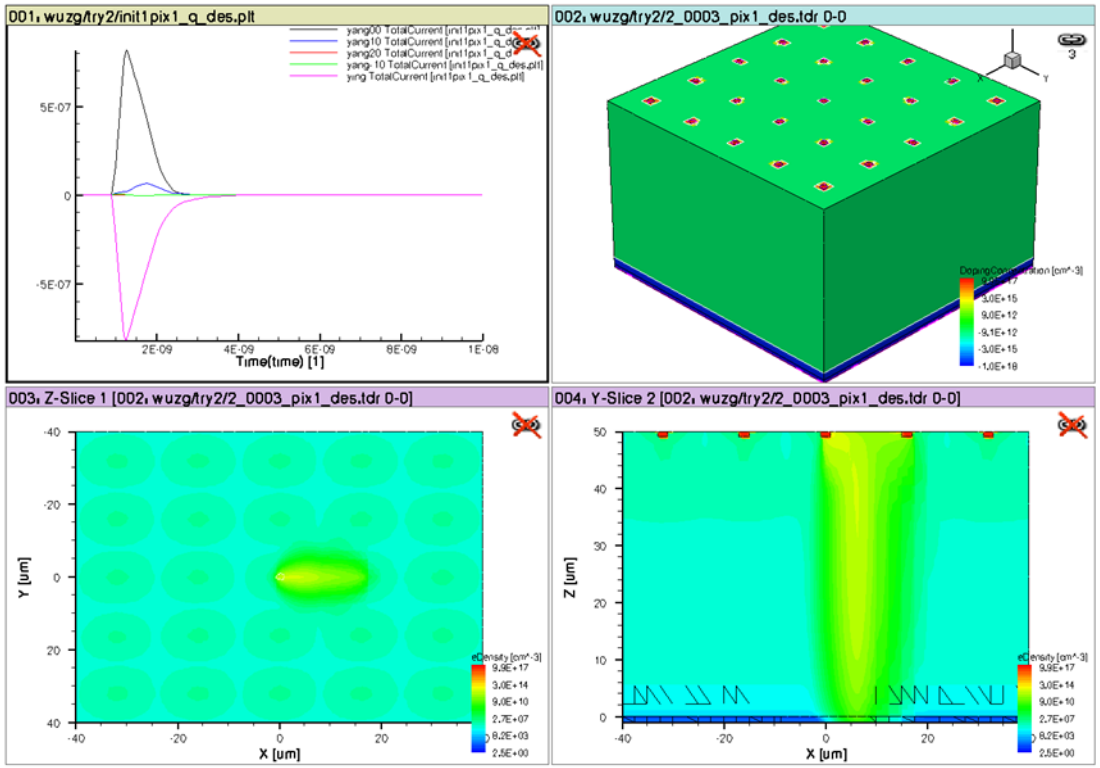
- I-V curve measurement

| | diode | Pix_rng | Bpw_cir | IO_bpw | I_all |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | m | m |
| 2 | 0 | 0 | m | × | m |
| 3 | 0 | m | × | × | m |



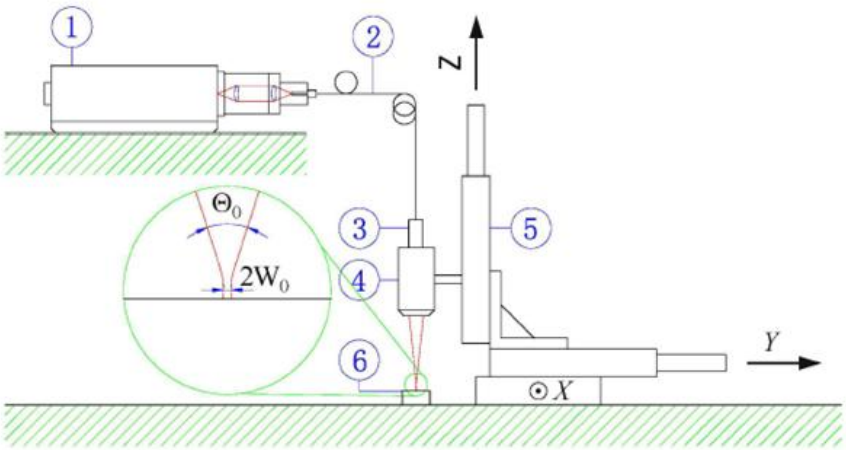
# Backup

- TCAD simulation for charge sharing in SOI sensor



# Backup

- Calculation for beam waist diameter




$$\tan\frac{\theta_0}{2}=\frac{D}{2F}. \qquad 2\omega_0=\frac{4\lambda}{\pi\theta_0}\approx\frac{4\lambda}{\pi}\frac{F}{D}.$$