



Performance evaluation of an SOI pixel sensor with in-pixel binary counters

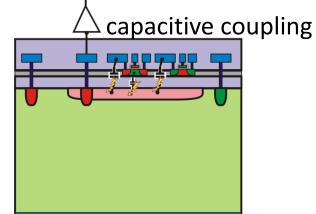
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- Introduction
- Chip concepts
- Noise performance
- Point spread function
- X-ray sensitivity
- Summary and outlook

Introduction

- Merits of SOI pixel detector
 - Monolithic process
 - Full in-pixel CMOS circuitry
 - Small parasitic capacitance
 - High resistive handle wafer with full depletion thickness up to several hundred microns
- Digital pickup in SOI sensor
- Motivation of prototype CPIXTEG3b
 - Double-SOI process to solve the pickup issue
 - High resolution low noise detector for X-ray imaging



G. DEPTUCH, SOIPIX 2010

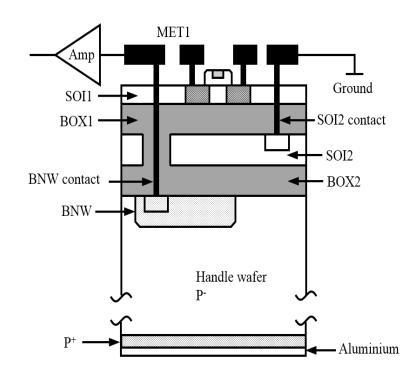
Introduction

- Design optimization and single pixel test results can be found in
 - Y. Lu et al., Nucl. Instrum. Methods Phys. Res. A 831 44-48 (2016).
- This report mainly focuses on
 - The noise performance of the full matrix
 - Detection of X-ray photons measured on a synchrotron X-ray beam

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Double-SOI pixel sensor

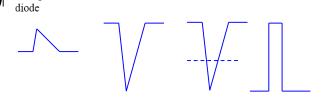
- 50 μm pixel pitch
- High resistive sensitive layer
 - P type substrate > $1k\Omega$ -cm
 - 300 μm full depletion thickness
- Charge collection electrode
 - Defined by buried n-well (BNW)
 - Octagon with size of 16 μm



- Middle silicon layer (SOI2)
 - Connected to shielding ground, dedicated shielding layer
 - Compensate the trapped charge caused by TID

Pixel circuit

- Charge sensitive preamplifier
 - Cf = 4fF
 - Constant current feedback (0.5 10nA adjustable)
- Shaper with inverse polarity
 - AC coupled
 - Voltage gain = 5



Signal processing chain in pixel

Shaper

Discrominator

4-bit DAC

Counter

Amplifier

capacitor

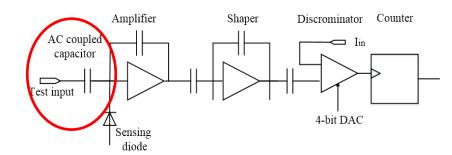
Test input

- Diode-biased inverter as the discriminator
 - AC coupled
 - 4-bit local DAC dedicated for threshold tuning
- 6-bit ripple counter
 - Register the X-ray photon number
 - Needs further optimization to incorporate more bits
- 6-bit shift register
 - For control of each individual pixel
 - DAC setting, Pixel mask, Calibration enable

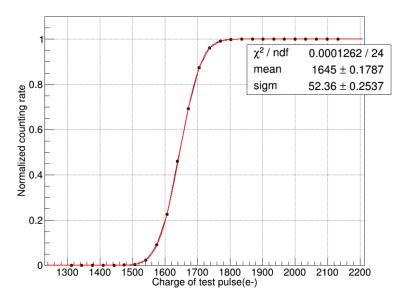
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TN and FPN

- Test pulse amplitude scan
 - Based on an AC coupled capacitor



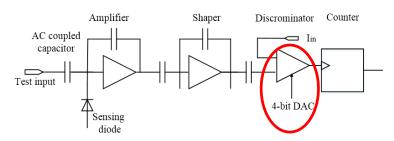
- S-curve fitting
 - Accumulative Gaussian fitting
 - TN, input-referred-threshold → sigma, mean



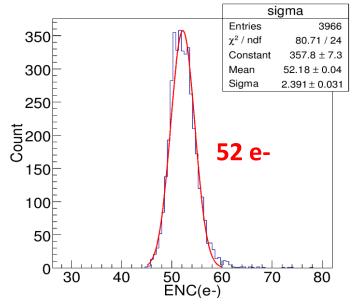
Typical S-curve fitting

TN and FPN

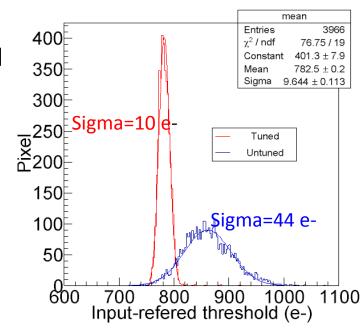
- Temporal noise (TN): 52 e⁻
 - 3966 pixels (special pixels masked)
- Fixed-pattern noise (FPN): 44 e-
 - 3966 pixels (special pixels masked)
- Threshold tuning
 - Target threshold = 780e⁻ (2.8keV)
 - The DAC value was added to the global threshold level



- Excellent threshold distribution
 - FPN = 10e- after tuning

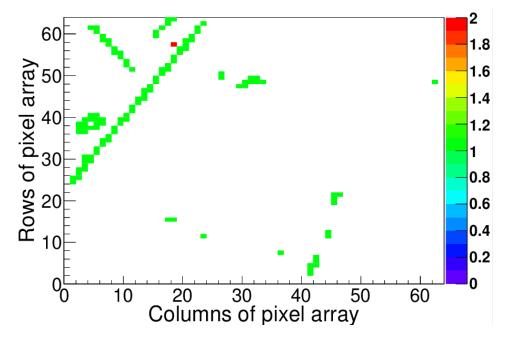


Noise distribution



Noise count measurement

- Zero noise hits
 - set in dark room, perpendicular to horizon
 - Threshold = $830e^{-}$ (3keV)
 - 10s \times 360 frames (for long exposure time and small data set)
 - Only a few events recorded from environmental radiation

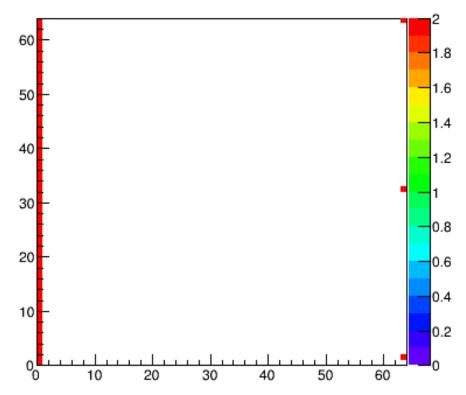


Environmental events accumulated in 1 hour

Noise count measurement



10s/frame



Environmental events replay

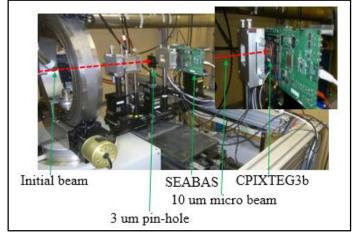
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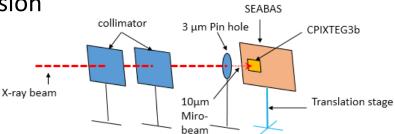
Point spread function

- Micro beam test setup
 - KEK PF BL-14A,
 - Pin hole with 3um in diameter
 - Micro beam with less than 10 μm in diameter
 - Chip and SEABAS mounted on high precision translation stage



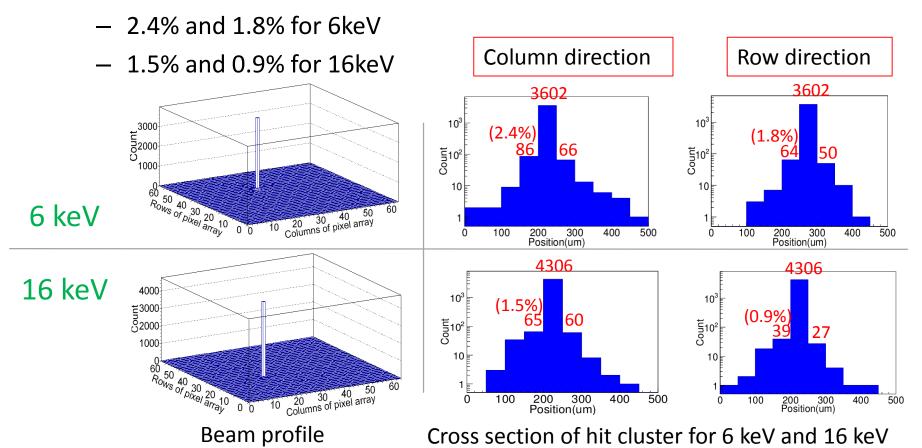
- For two different energy 6keV and 16 keV
- Impinged at the center of targeted pixel





Point spread function

- Micro beam measurement
 - Target pixel dominated almost all of the counts
- The counting ratio of neighboring pixels to the center one is



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 - Sensor depletion
 - Charge sharing
 - Flat field response
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Sensor depletion

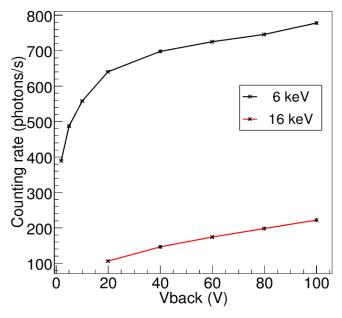
- Measurement
 - Micro beam illuminate from the topside
 - Impinged at the pixel center
 - Bias voltage increasing to -100 V
- Relative quantum efficiency (RQE)
 - Eliminate the effects of various inactive absorption medium

$$RQE = \frac{N(-20V)}{N(-80V)} = \frac{\eta(-20V)}{\eta(-80V)}$$

$$\eta = 1 - e^{-\mu d}$$

$$d = \xi \sqrt{V}$$

N:counting rate
η:quantum efficiency
μ:attenuation coefficient
d:depletion thickness.
ξ:process-related constant

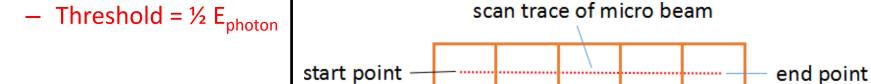


- The depletion thickness
 - ~117 µm at 100 V bias voltage
- High bias voltage leads to significant leakage current in phriphery
 - guard ring need optimization

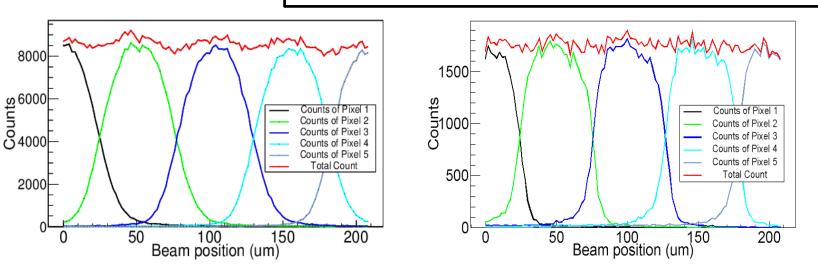
Beam energy (keV)	Bias voltage (V)	Depletion thickness (um)
6	-100	116.9±1.7
16	-100	136.0±21.5

Charge sharing at pixel edge

- Scan across 5 pixels from center to center
 - Step size = $2 \mu m$
- Uniform efficiency can be achieved at pixel edge



pixel 1

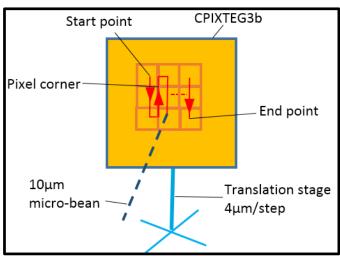


Charge sharing at pixel edge for 6 keV (left) and 16 keV (right) X-ray

pixel 5

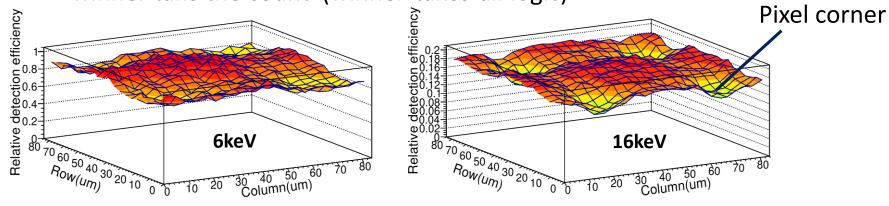
Charge sharing at pixel corner

- Across 3×3 pixel-square
 - Step = $4 \mu m$ for two direction
- Inevitable loss of efficiency at the corner
 - Threshold = $\frac{1}{2}$ E_{photon}
 - Charge shared by 4 pixels adjoined



Considerable effects on pixel sensor with small pixel size

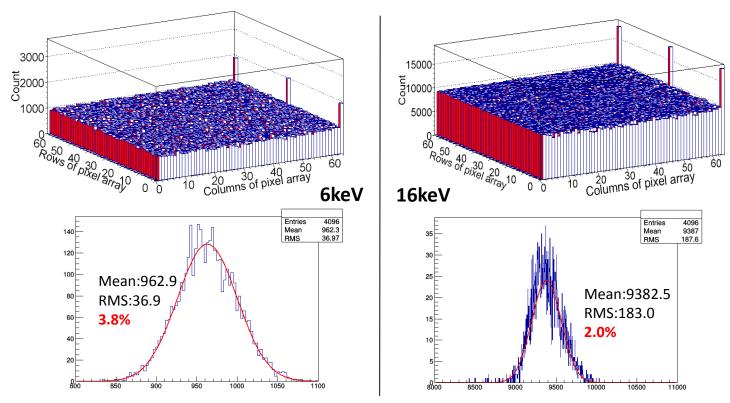
 Solution: to compare the charge between adjoining pixels and make the winner take the count (winner-takes-all logic)



Charge sharing at pixel corner for 6 keV (left) and 16 keV (right) X-ray

Flat field response

- Beam scattered by glassy carbon
 - Sensor placed in 90° with respect to the beam line
- Full pixel array illuminated.
 - inhomogeneity: 3.8% and 2.0%



Count distribution under flat field

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Summary and outlook

- The prototype CPIXTEG3b led to the development of SOI pixel sensors of low noise and high resolution for X-ray imaging.
 - The TN is 52 e⁻ and FPN is 10 e⁻ over the full matrix
 - A small pitch of 50μm manifests good PSF as expected
- The depletion of sensor and the impact of charge sharing have been characterized, and provides the insights for further development.
- The uniformity of response to X-ray photons has been obtained in the flat field test.
- Further improvements have been made
 - Charge sharing decision logic equipped in each pixel
 - Compact layout of counter to accommodate 19 bits

Thanks for your attention!

