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Performance evaluation of an SOI pixel sensor with in-pixel binary counters

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Digital pickup is a critical issue to pixel detectors. SOI technology suffered much from it due to the capacitive coupling between sensing electrode and pixel circuit, insulated by a thin layer of SiO₂. In order to tackle this issue, an advanced process called Double-SOI has been developed and many prototype chips have been submitted to this process. Among them, the design of CPIXTEG3b is dedicated to the study of the digital pickup issue. For this reason, a conventional architecture of single photon counting pixel is chosen and the in-pixel binary counter acts as an active source of pickup. The design optimization concerning Double-SOI and test results from single pixel have been summarized and presented in a separate publication. This talk will focus on the noise performance of the full matrix and detection efficiency measured on a synchrotron X-ray beam. The typical ENC is 52 e⁻ and the sigma of threshold dispersion is 10 e⁻ after threshold tuning. The detailed study of detection efficiency has demonstrated a homogeneous response to a flat field of illumination and revealed the impact of charge sharing at a pitch of 50 μm. This work has verified the solution of digital pickup explicitly and led to the development of SOI pixel sensors of low noise and high resolution for X-ray imaging.

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