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OIST, Okinawa, Japan

Investigation of Radiation Hardness Improvement by Applying Back-gate Bias for FD-SOI MOSFETs

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SOIPIX
Silicon-On-Insulator Pixel Detector Project

Outline

1. Introduction
2. Experimental Procedure
3. Concept for recovering by using back-gate bias
4. Gate length dependence improvement and recovering by back-gate bias
5. Back-gate bias windows covering wide L range and N/P MOSFETs
6. Summary

Introduction

Structure of FD-SOI pixel X-ray sensor
- pn photo-diode in handle wafer
- circuits in SOI layer
- via connects between sensor and circuit

Merits of FD-SOI pixel X-ray sensor
- monolithic and small pixel
- SOI CMOS process compatible
- full depletion of photo-diode

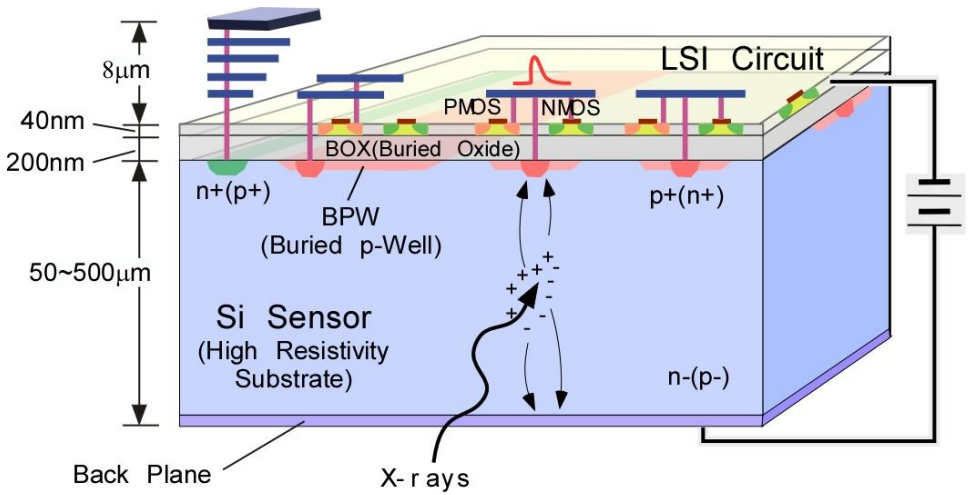
One of major issues is TID weakness of FD-SOI MOSFET.

Cause of radiation degradation of SOI MOSFET

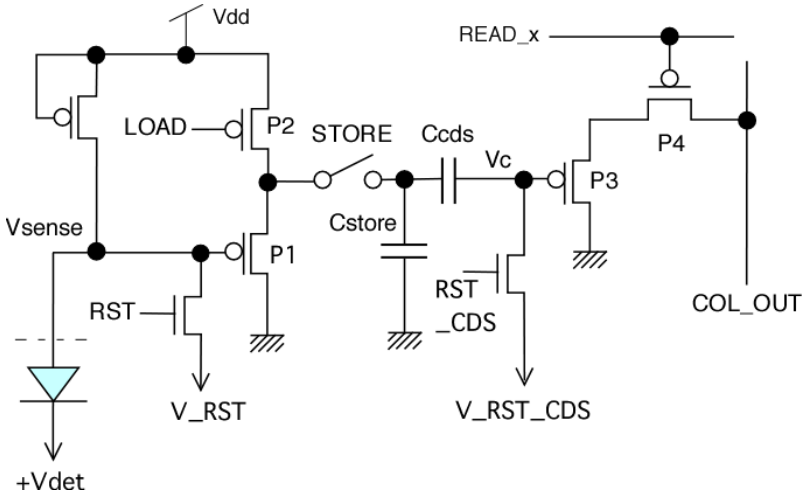
Positive charge generation in BOX

Is there any possibility to compensate the charge? --- back-gate bias

Can back gate bias compensate uniformly for different gate length or channel (Nch/Pch) ?



Schematic cross-section of sensor



Integration type pixel circuit

Experimental Procedure

1. Sample Process
   - Fabrication Process : 0.2 μm FD-SOI CMOS Process with 5 metal layers (Lapis Semiconductor Co., Ltd.)
   - MOSFET : salicide and Lightly Doped Drain (LDD):ULP-LDD/RH-LDD
   - SOI layer thickness : around 40 nm
   - Buried Oxide (BOX) Thickness : 200 nm
   - Gate Oxide (Gox) Thickness : 4.5 nm
2. Measured Test Keys
   - Floating body Nch & Pch FD-SOI MOSFETs
   - W=10μm, L=0.2/0.3/0.5/1.0/10 μm
3. X-ray Radiation (by RIKEN SPring-8)
   - Dose Rate : 3 Gy(Si)/s
   - All terminals of MOSFETs (S/D/G) are grounded during irradiation
     (For detail, refer to : T. Kudo et.al., IEEE Trans. Nuclear Science, 61, pp.1444-pp1450 , 2014)
4. Measurement
   - I_{ds}-V_{gs} with $|V_{ds}|$=0.1 V, $V_{back\text{-}gate}$=-18 to +2 V
   - I_{d_lin} : I_{ds} @ $|V_{ds}|$=0.1 V, $|V_{gs}|$=1.8 V
   - Vt : extrapolated from I_{ds}-V_{gs} around g_{mmax}

Concept for Recovering by Back Gate Bias

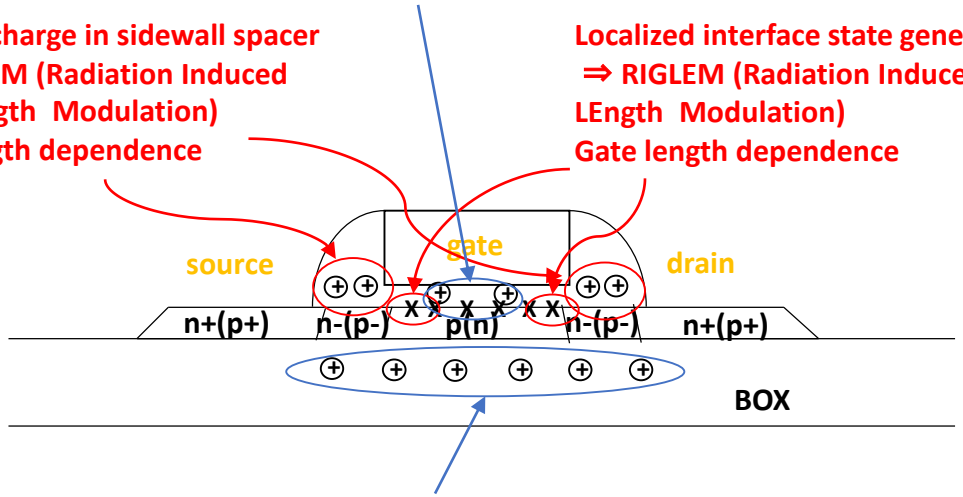
■ Assuming that generated positive charge in oxide and interface states at Si-SiO_2 by X-ray irradiation causes of MOSFET characteristic change.
■ Reduce degradation factor of gate length dependence (RIGLEM) ⇒ RH-LDD.
■ Compensate uniformly distributed charge by back gate bias.

Possible causes of MOSFET characteristic change

Positive charge and interface state in channel
⇒ Uniformly distributed underneath gate
No or less gate length dependence

Positive charge in sidewall spacer
⇒ RIGLEM (Radiation Induced Gate LEngth Modulation)
Gate length dependence

Localized interface state generation
⇒ RIGLEM (Radiation Induced Gate LEngth Modulation)
Gate length dependence

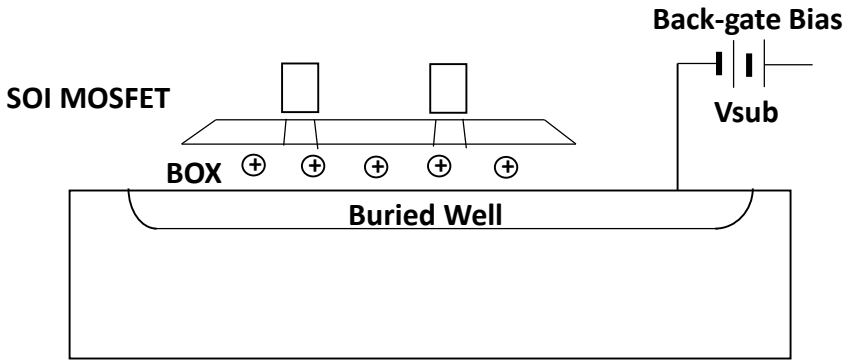


Positive charge in BOX
⇒ Uniformly distributed over BOX
No or less gate length dependence

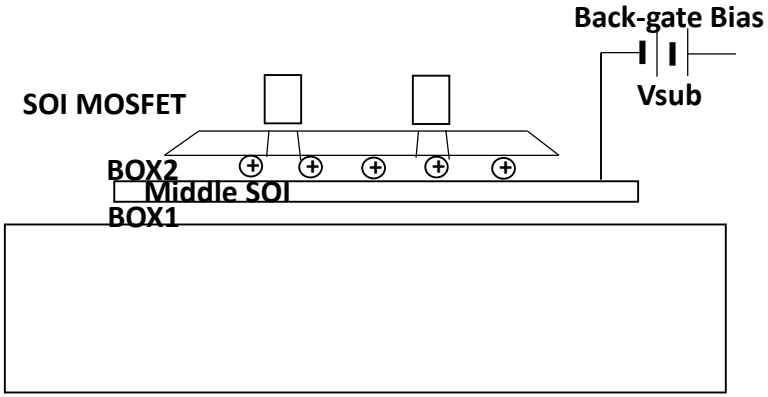
① gate length dependent degradation improvement
② improvement by back-gate bias with Nch/Pch and wide gate length range.

BOX Charge Compensation by Applying Back-Gate Bias

If major cause of characteristic change is positive charge in BOX, then the charge can be compensated by applying back-gate bias through Buried Well (S-SOI) or Middle SOI (D-SOI).



Single SOI

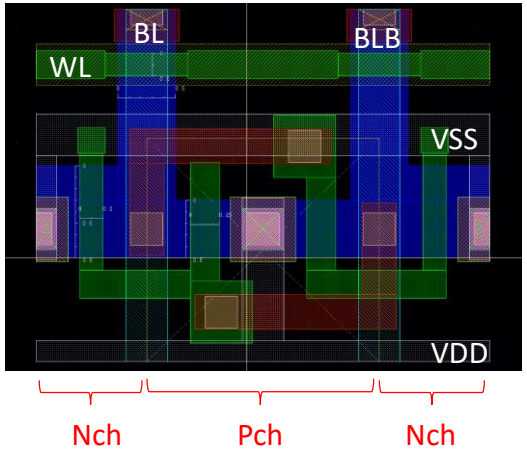


Double SOI

Back-gate electrode (Buried Well and Middle SOI) should cover multiple MOSFETs including Nch/Pch because of their rough DR.

Need to evaluate one back-gate electrode can cover

- **wide range of gate length (0.2-10 μm)**
- **Nch and Pch**

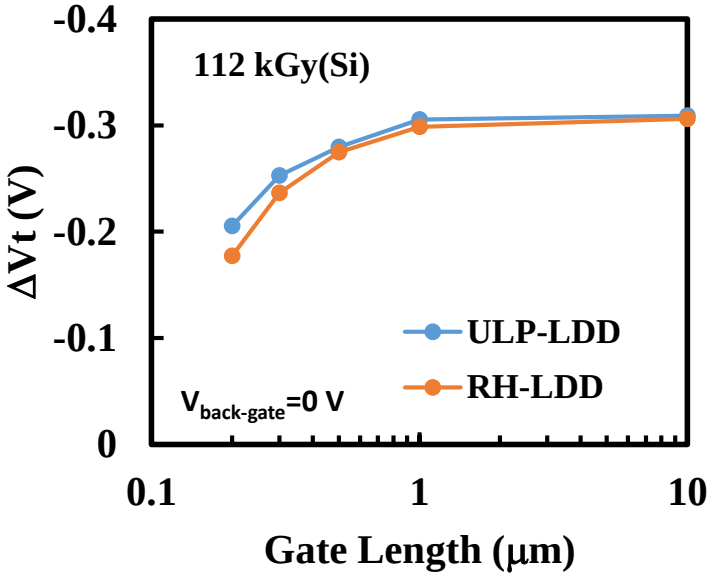


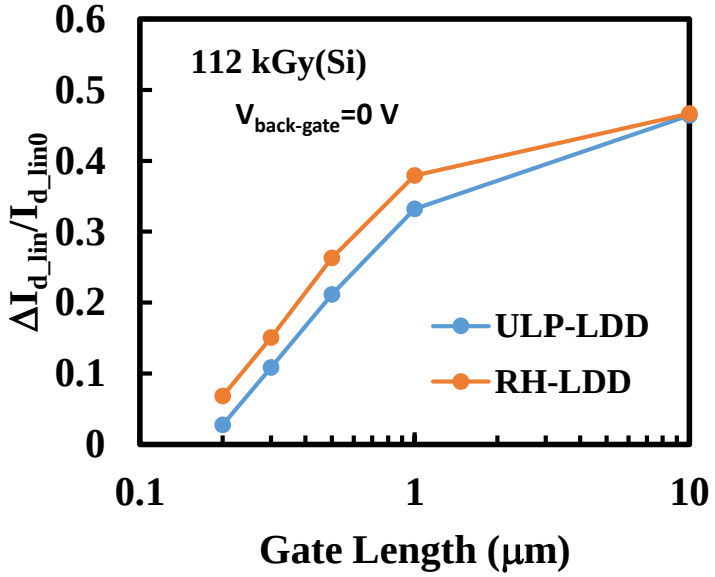
SRAM Bit Cell

In SOI, active merge technique can be used to shrink area such as SRAM bit cell. Therefore, Nch and Pch embedded back gate electrode must be needed.

Nch MOSFET RIGLEM Improvement by RH-LDD

- Gate length dependence can be slightly improved by applying RH-LDD.
- Much higher LDD dose may improve RIGLEM but short channel effect occurs.



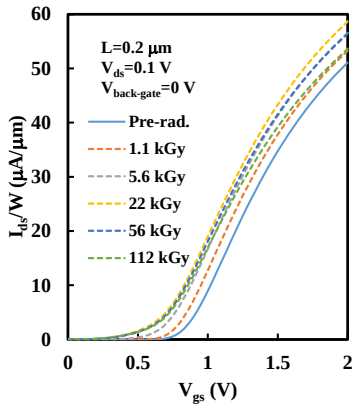


Presented in ETCMOS 2017
I. Kurachi et al., "Analysis of Radiation Induced Gate Length Modulation Mechanism in FD-SOI MOSFETs"

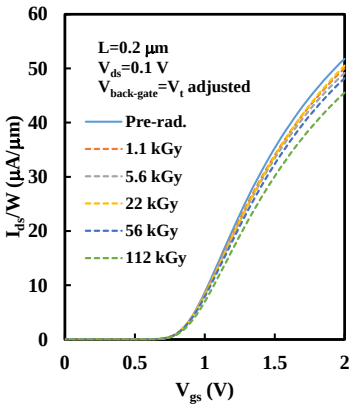
Nch MOSFET Recovering by Applying Back-Gate Bias

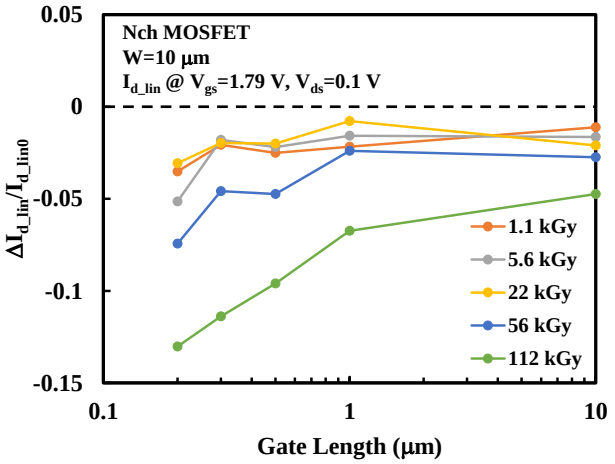
- Drain current change can be reduced by applying correct back-gate bias to align Vt.
- In low dose (<22 kGy(Si)), drain current change can be controlled within 5%.
- In high dose (100 kGy(Si)), around 13% change for L=0.2 μm and 5% for L=10 μm even though Vt aligns to Pre-rad. because of RIGLEM.

L=0.2 μm

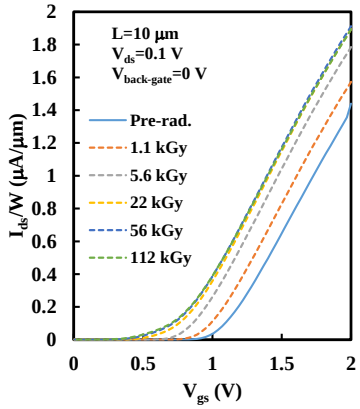


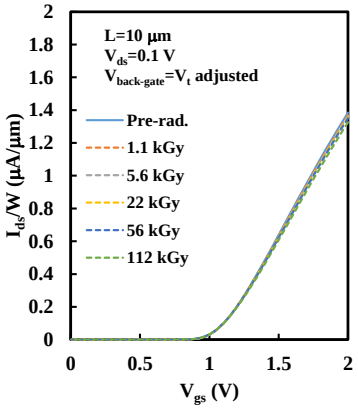
Vt adjustment by applying $V_{back-gate}$

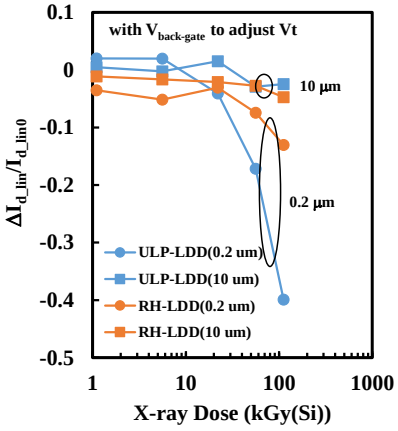




L=10 μm

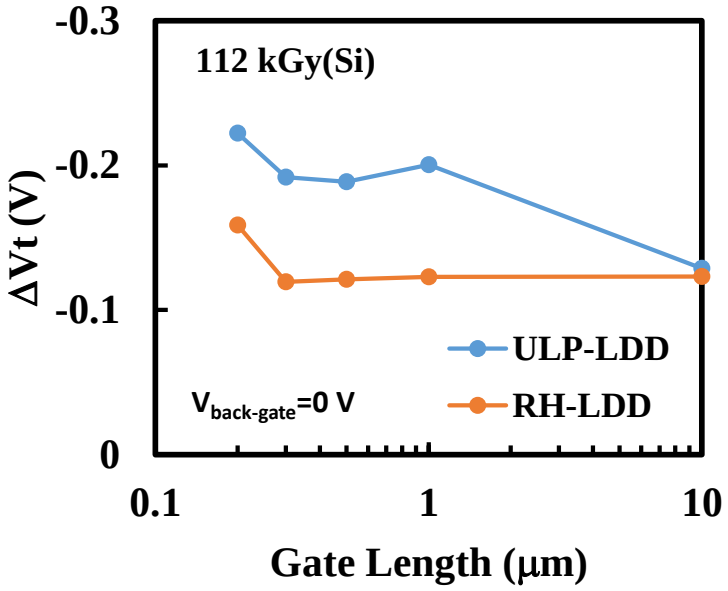


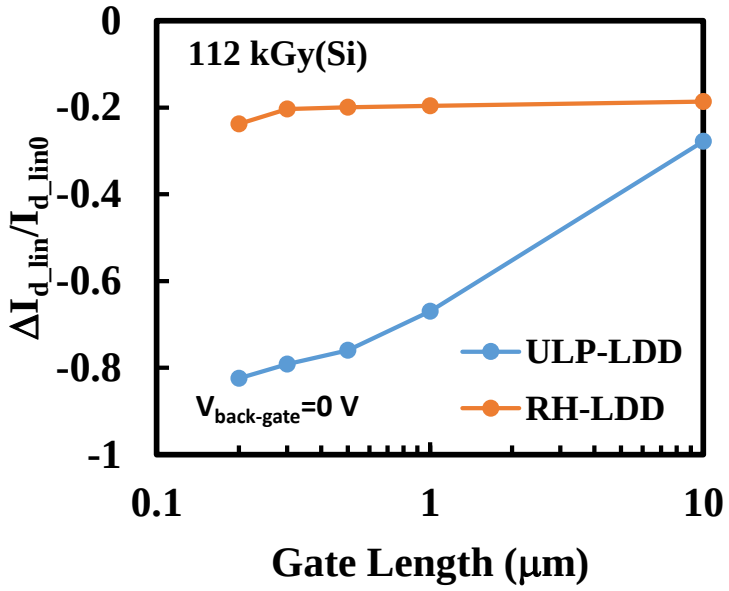




Pch MOSFET RIGLEM Improvement by RH-LDD

- Gate length dependence is dramatically improved by RH-LDD.
- ΔVt and $\Delta I_{d\_lin}/I_{d\_lin0}$ are almost constant in gate length even after 100 kGy(Si) irradiation.
- Major degradation of RH-LDD MOSFET may be caused by generated positive charge in BOX. This means back gate bias can work well to compensate degradation.





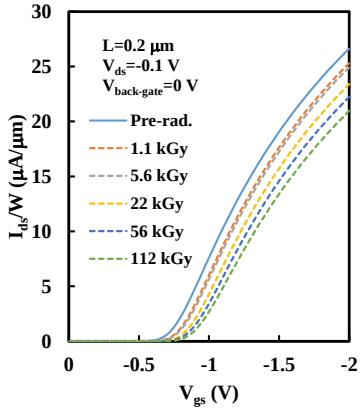
I. Kurachi et al., IEEE Trans. Electron Devices, vol. 62, pp. 2371-2376, 2015.

I. Kurachi et al., IEEE Trans. Electron Devices, vol. 63, pp. 2293-2298, 2016.

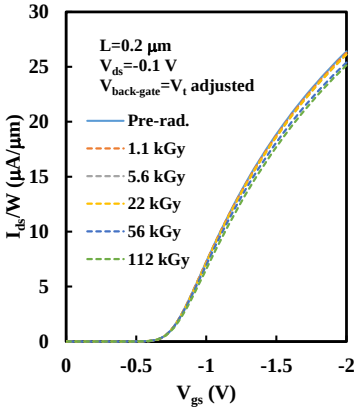
Pch MOSFET Recovering by Applying Back-Gate Bias

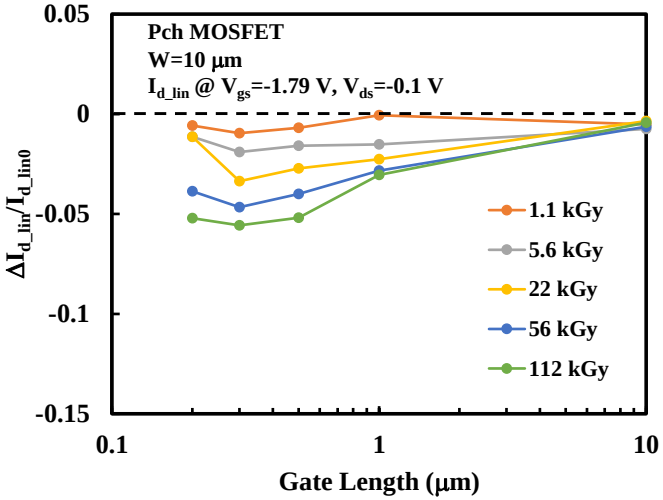
- Drain current change can be reduced by applying back-gate bias to align Vt.
- When L=10 μm, drain currents are almost identical up to 100 kGy(Si) irradiation.
- Overall drain current change is less than around 5% up to 100 kGy(Si) irradiation.

L=0.2 μm

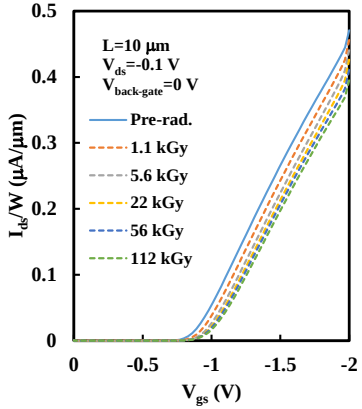


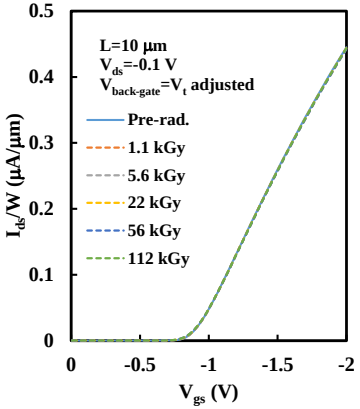
Vt adjustment by applying $V_{back-gate}$





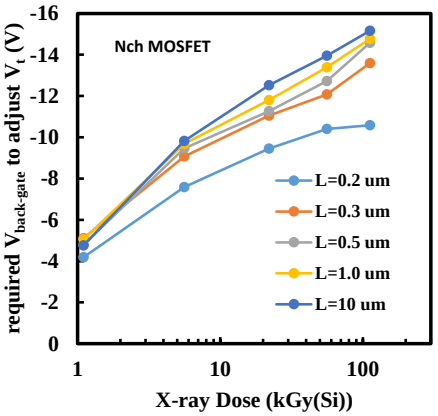
L=10 μm

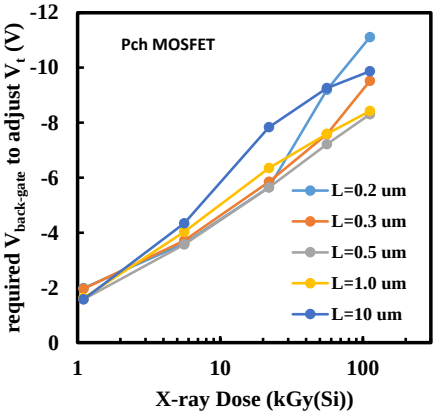


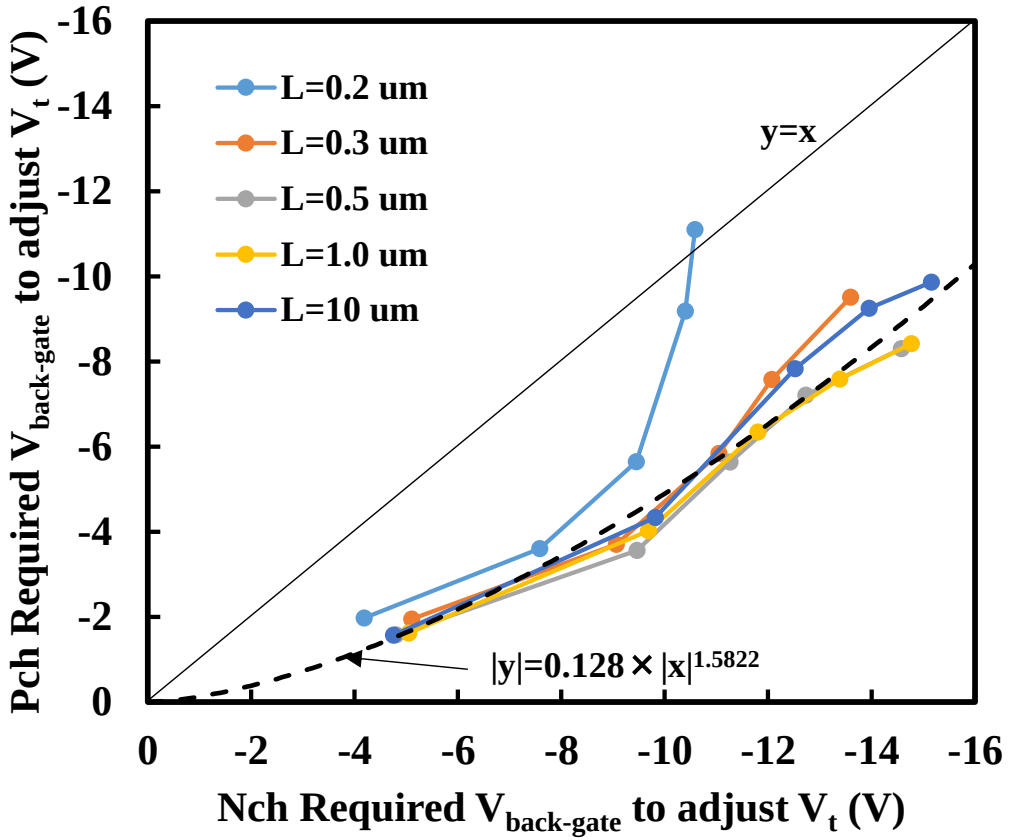


Required Back-Gate Bias of N & Pch MOSFETs

- Required back gate biases to adjust Vt for Nch MOSFETs are different from those for Pch MOSFETs.
- The relation between both biases shows power low relation.
- For shorter L (0.2 μm), relation is not follow the trend because of RIGLEM of Nch MOSFET.

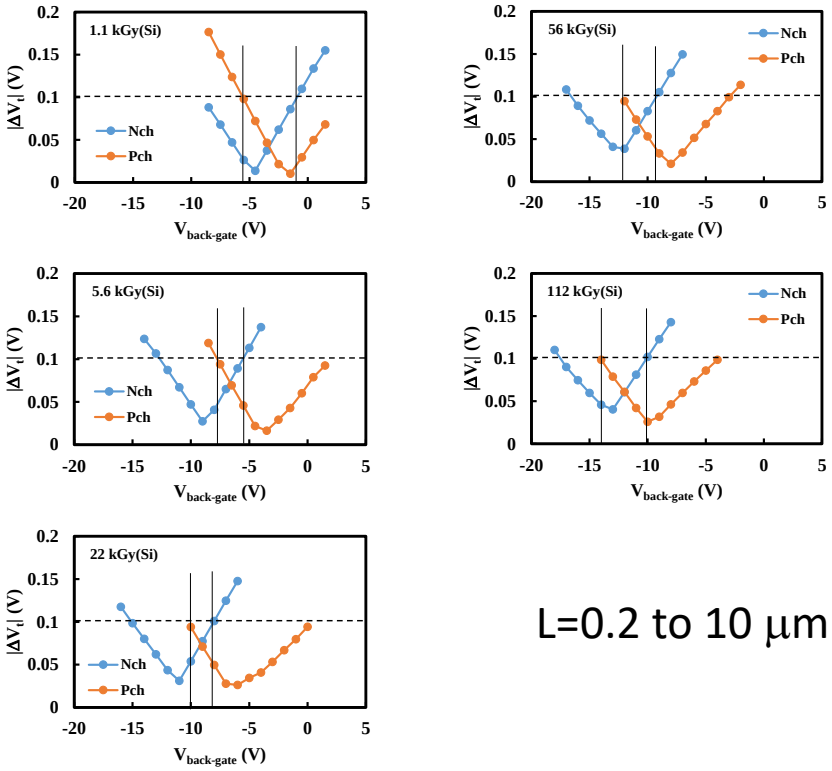




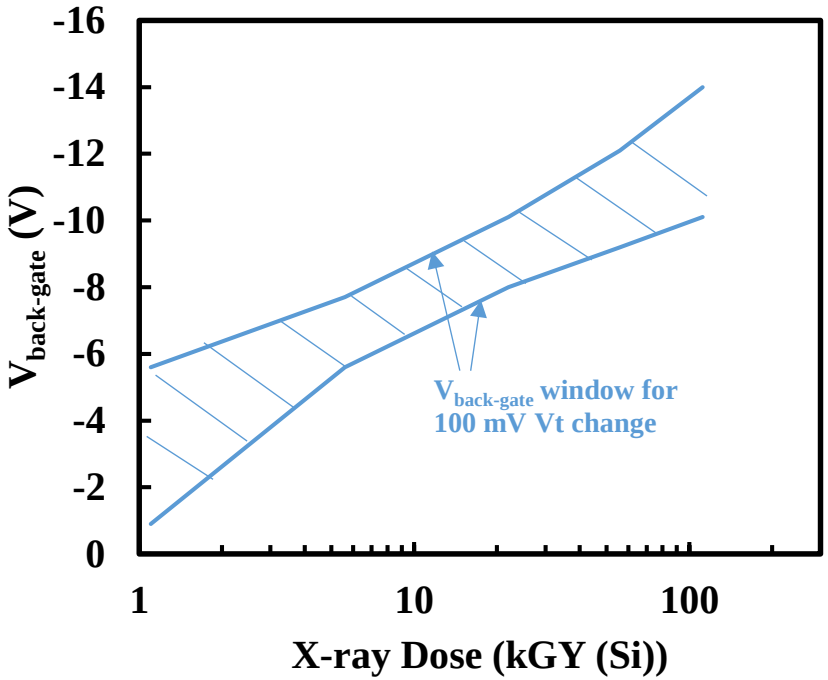


Threshold Voltage Correction by Applying Back-Gate Bias

- $V_{back\text{-}gate}$ windows up to 100 kGy(Si) irradiation for N & Pch of L=0.2-10 μm are investigated in terms of Vt change.
- No windows for |ΔVt|<75 mV.
- If 100 mV of |ΔVt| is allowable, there are $V_{back\text{-}gate}$ windows up to 100 kGy(Si).

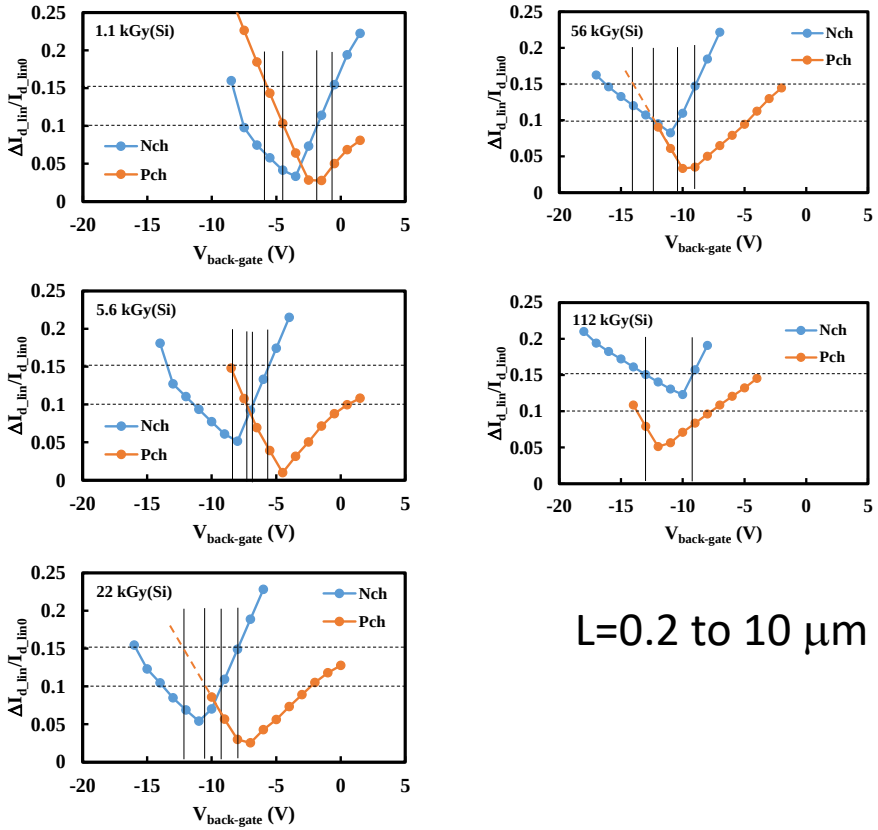


L=0.2 to 10 μm

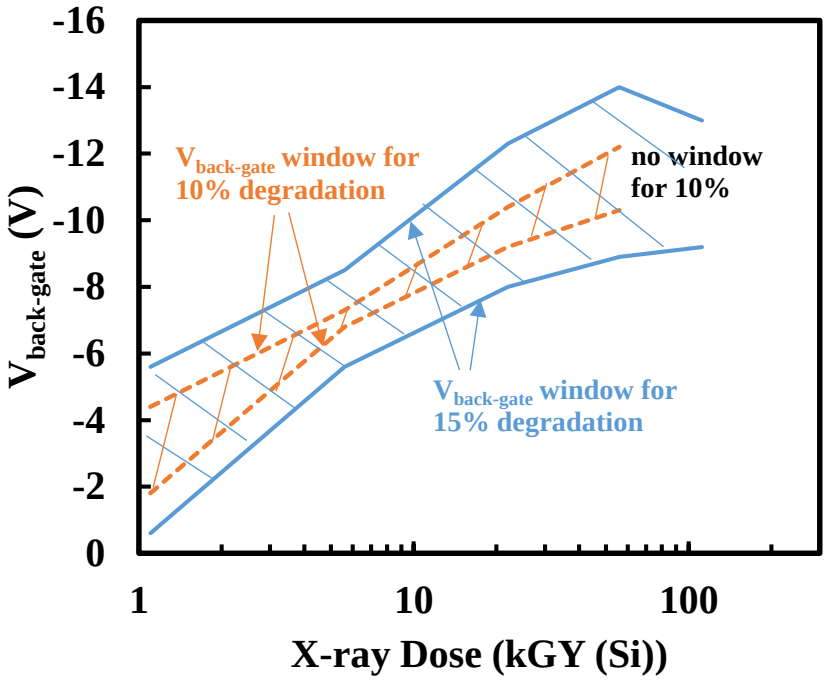


Linear Drain Current Correction by Applying Back-Gate Bias

- $V_{back\text{-}gate}$ windows up to 100 kGy(Si) irradiation for N & Pch of L=0.2-10 μm are investigated in terms of drain current cahnge.
- No windows up to 100 kGy(Si) exists if allowable change is 10%.
- If allowable change is 15%, there are $V_{back\text{-}gate}$ windows up to 100 kGy(Si).



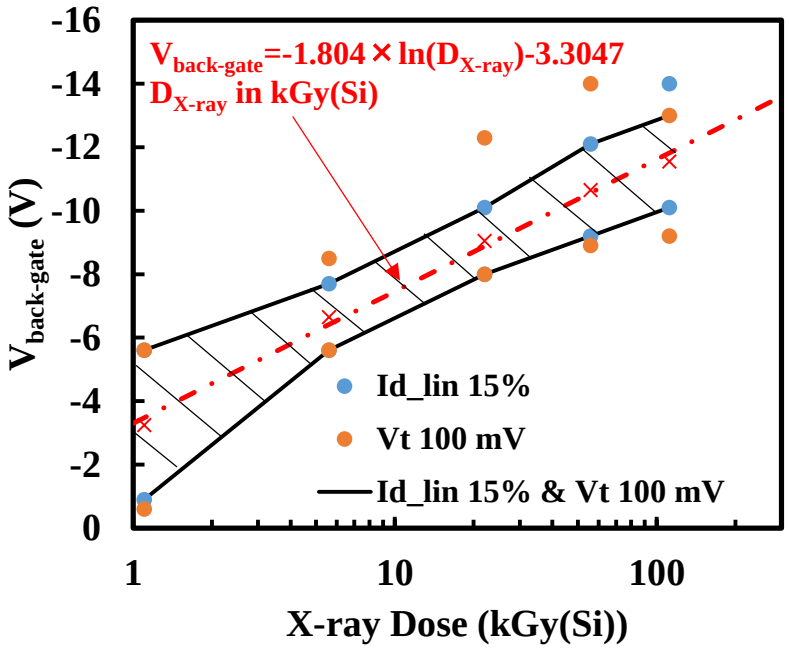
L=0.2 to 10 μm

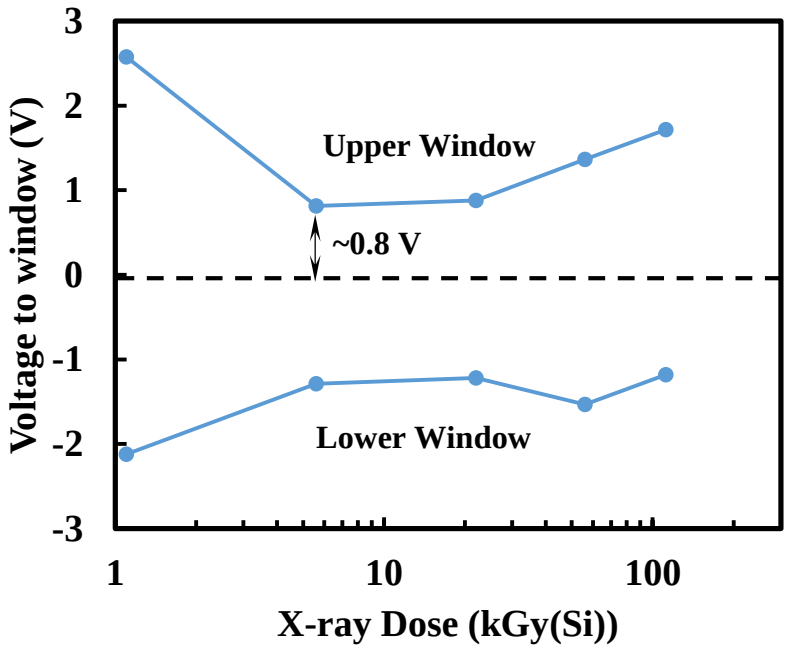


Back-Gate Bias Window for V_t & I_{ds} Correction

- If variations of 100 mV in Vt and 15% in I_{d_lin} can be allowable, there are $V_{back\text{-}gate}$ windows to correct both Nch & Pch with L=0.2-10 μm up to 100 kGy(Si) irradiation.
- Correction by $V_{back\text{-}gate}$ follows $V_{back\text{-}gate}$=-1.804×ln($D_{X\text{-}ray}$)-3.3047. $D_{X\text{-}ray}$ (kGy(Si))
- Minimum allowable tolerance of $V_{back\text{-}gate}$ is around 0.8 V.

Nch & Pch MOSFET
L=0.2 to 10 μm



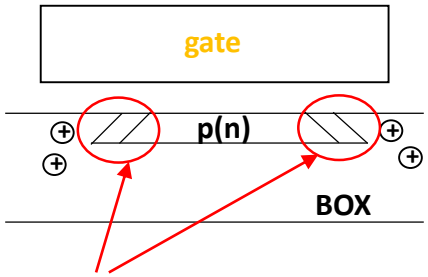


Summary

- Radiation hardness improvement by applying back-gate bias to compensate generated positive charge in BOX has been investigated.
- Back-gate bias can be applied through buried well (single SOI) and middle SOI (double SOI). Due to rough design rule of buried well and middle SOI, a given back-gate bias should cover wide range of gate length and N and Pch MOSFETs.
- Improvement of RIGLEM by high dose LDD can help to make wider back-gate bias windows.
- When allowable Vt and I_{d_lin} variations are 100 mV and 15%, respectively, existing of back-gate bias widow has been confirmed up to around 100 kGy(Si) X-ray irradiation.
- This method may one of solution candidates for radiation hardness improvement of TID weak FD-SOI MOSFETs.

Thank you for your kind attention !!

Back-up

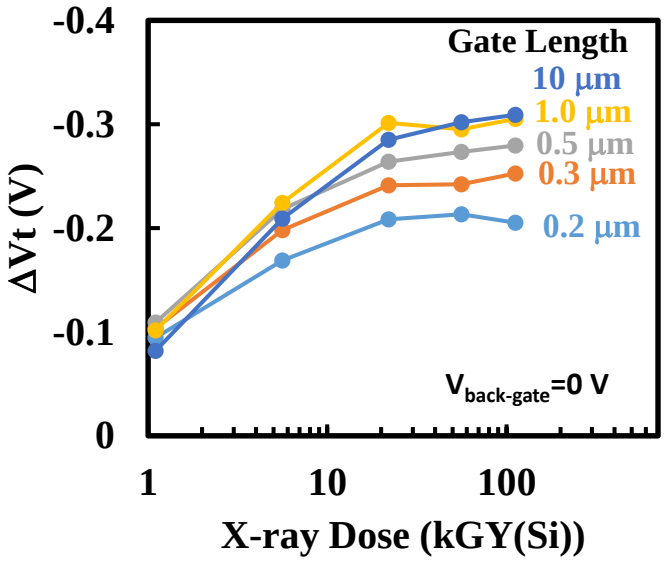


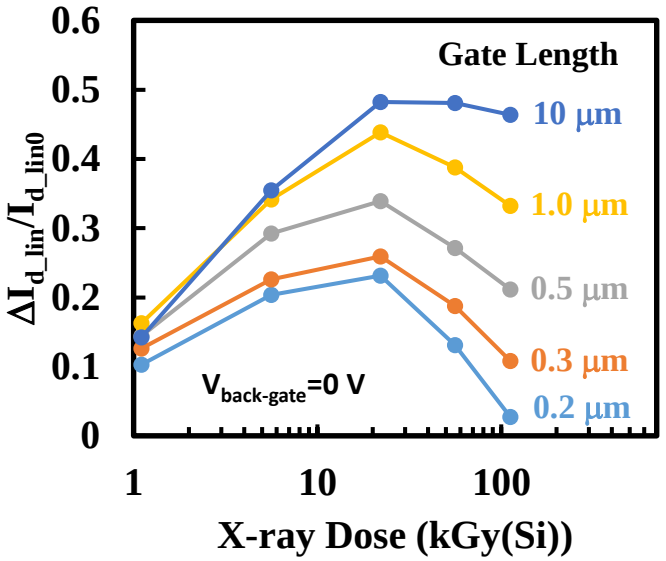
Higher doping region by channel stop implantation. Hard to turn-on by Vgs.
No RINCE and width dependence.

Nch MOSFET X-ray Irradiation Degradation

- **Drain current increase is caused by generated positive charge in BOX.**
- **Drain current decrease in higher dose region, which has gate length dependence (RIGLEM) , is caused by interface state generation at gate edge.**
- **To recover characteristics for wide range of gate length, REGLEM has to be minimized.**

ULP-LDD





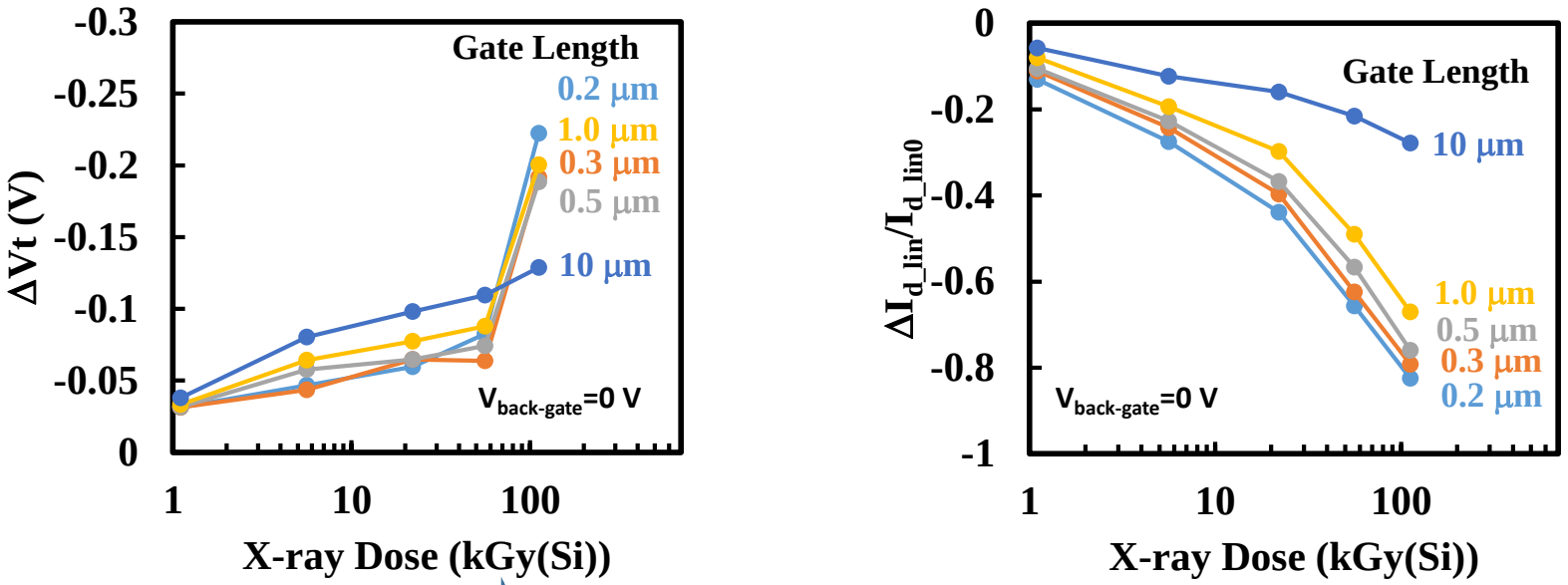
Improvement of gate length dependence may be achieved by applying higher LDD dose (RH-LDD) to cover gate edge region.

Presented in ETCMOS 2017
I. Kurachi et al., "Analysis of Radiation Induced Gate Length Modulation Mechanism in FD-SOI MOSFETs"

Pch MOSFET X-ray Irradiation Degradation

- **Relatively high drain current decrease as 80% is observed for L=0.2 μm.**
- **Drain current decrease is caused by generated positive charge in BOX and positive charge in sidewall spacer (RIGLEM).**
- **Effect due to positive charge in spacer must be minimized to reduce gate length dependence.**

ULP-LDD



Improvement of gate length dependence may be achieved by applying higher LDD dose (RH-LDD) to cover gate edge region.

I. Kurachi et al., IEEE Trans. Electron Devices, vol. 62, pp. 2371-2376, 2015.

Idea of automatic back gate bias generation circuit

Detection of charge in BOX

Back gate bias generation circuit

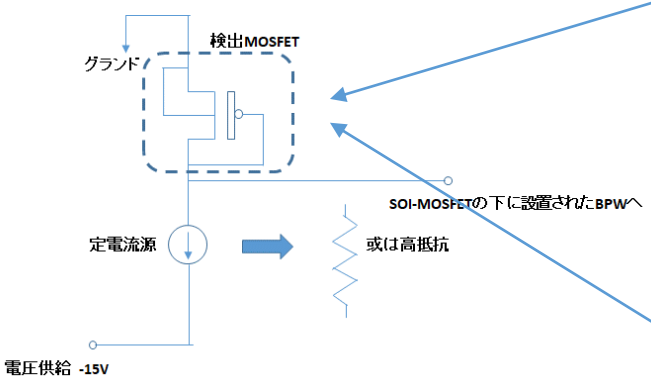
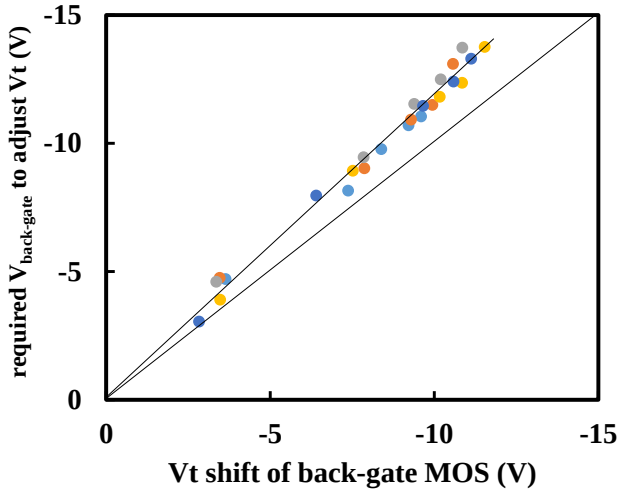


図-2 本発明の実施例1での補正電圧自動発生回路



Single SOI

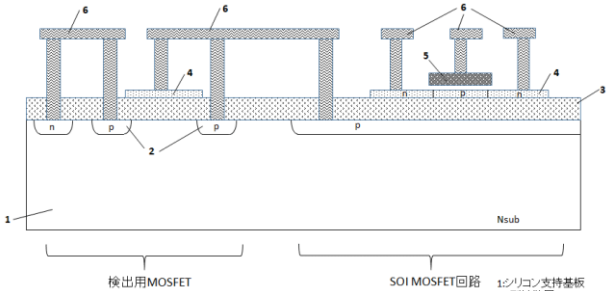


図-1 本発明の実施例1での検出用MOSFET構造

Double SOI

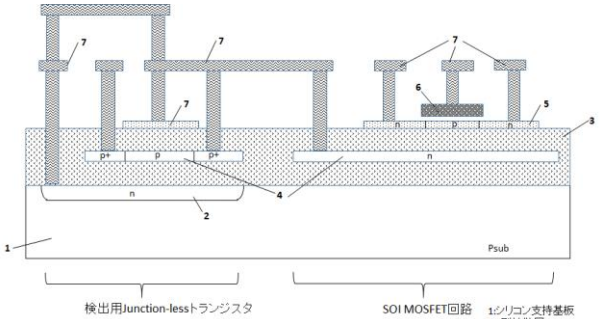


図-3 本発明の実施例2での検出用Junction-lessトランジスタ構造

Patent has been issued.