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Investigation of Radiation Hardness Improvement by Applying Back-gate Bias for FD-SOI MOSFETs

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Radiation hardness improvement of FD-SOI MOSFETs has been investigated in terms of positive charge compensation in buried oxide (BOX) by applying back-gate bias. In general, the radiation tolerance of SOI MOSFET is low in total ionizing dose (TID) because the relatively thick oxide, BOX, exists underneath the MOSFETs and the positive charge generated in the oxide by the irradiation. Then, increase of N-channel MOSFET or decrease of P-channel MOSFET drain current occur due to threshold voltage shift caused by field effect of the generated positive charge in BOX. There is possibility to compensate the charge by biasing the back-gate to negative. However, the compensation method is effective when the front-side MOSFET degradation is well controlled and the variation of generated positive charge in BOX is minimized between N and P channel and for wide range of gate length. With using radiation hardened lightly doped drain (RH-LDD) to suppress radiation induced gate length modulation (RIGLEM) and L=0.2 to 10 um MOSFETs, we found the back-gate bias windows to keep the linear drain current variation within 15% up to 100 kGy(Si) X-ray irradiation. This is evidence for high radiation hardness even for FD-SOI MOSFET in TID with the back-gate bias compensation. This back-gate compensation method is also suitable for double SOI technology which has the silicon shield electrode in the middle of BOX.

Primary author: Prof. KURACHI, Ikuo (HIgh Energy Accelerator Research Organization)

Co-authors: Mr KOBAYASHI, Kazuo (RIKEN SPring-8 Center); Mr OKIHARA, Masao (Lapis Semiconductor Co., Ltd.); Mr KASAI, Hiroki (Lapis Semiconductor Miyagi Co., Ltd.); HATSUI, Takaki (RIKEN); HARA, Kazuhiko (University of Tsukuba (JP)); MIYOSHI, Toshinobu (KEK); ARAI, Yasuo (High Energy Accelerator Research Organization (JP))

Presenter: Prof. KURACHI, Ikuo (HIgh Energy Accelerator Research Organization)

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