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Development of new high-speed readout system for SOI pixel detectors

Friday 15 December 2017 09:00 (20 minutes)

We are developing new high-speed readout system for Silicon-On-Insulator (SOI) Pixel Detectors. The SOI detector is a monolithic radiation imaging detector based on a 0.2um FD-SOI CMOS process. As before, we used Xilinx Virtex-4/5 FPGA readout board for SOI detector, and developed many facilities for this board. However, Virtex-4/5 FPGA is now obsoleted and does not have enough performance for recent experiments which require more than 1 kHz high-speed imaging with large number of pixels. Thus we started to develop new high-speed readout system using KC705. KC705 is the evaluation board which has Kintex-7, new generation FPGA. We develop new DAQ structure, compatible with previous environment, on this board and implement several functions for practical purpose. Although the achieved speed of the new system is still 100 Hz for 80k pixels, we are confident to reach readout speed of 1 kHz soon. The detail of new readout system will be shown in the presentation.

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